Hall Ticket No | | | | | | | | | | | Question Paper Code: AECC49

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal-500043, Hyderabad

B.Tech IV SEMESTER END EXAMINATIONS (REGULAR/SUPPLEMENTARY) - AUGUST 2023
Regulation: UG-20

DIGITAL DESIGN THROUGH VERILOG

Time: 3 Hours **(ELECTRONICS AND COMMUNICATION ENGINEERING)** **Max Marks: 70**

Answer ALL questions in Module I and II
Answer ONE out of two questions in Modules III, IV and V
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) Elucidate about white space characters and variables in Verilog HDL. Distinguish them with the help of suitable examples. [BL: Understand| CO: 1|Marks: 7]

   (b) Develop a simple Verilog code which explains the purpose of declaring ports in Verilog HDL. [BL: Apply| CO: 1|Marks: 7]

MODULE – II

2. (a) Summarize the following relevant to gate level modelling with necessary syntax and example.
   i) Gate delays
   ii) Array of instances [BL: Understand| CO: 2|Marks: 7]

   (b) Build a gate level description of a 2 bit circuit which compares their magnitudes with relevant logic diagram and Verilog HDL source code. [BL: Apply| CO: 2|Marks: 7]

MODULE – III

3. (a) What is behavioral modeling? Explain the concept of event construct in a module for Verilog HDL. [BL: Understand| CO: 3|Marks: 7]

   (b) Construct a model using the behavioral modeling style to describe the behavior of a JK flip- flop using an always statement. [BL: Apply| CO: 3|Marks: 7]

4. (a) Demonstrate the following statements with suitable examples.
   i) Blocking
   ii) Non – Blocking [BL: Understand| CO: 4|Marks: 7]

   (b) Develop a Verilog HDL code for n-bit shift register with an enable input using blocking assignments. [BL: Apply| CO: 4|Marks: 7]

MODULE – IV

5. (a) Discuss about the concept of basic switch primitives available in switch level modelling of verilog HDL. [BL: Understand| CO: 5|Marks: 7]

   (b) Explain the operation of left/right shifter briefly and also design the Verilog module for the same. [BL: Understand| CO: 5|Marks: 7]

6. (a) How strength and delays are instantiated in Verilog HDL? Explain the same in detail.
[BL: Understand| CO: 5|Marks: 7]

   (b) Illustrate the operation of complementary metal oxide semiconductor (CMOS) flip – flop and also design the Verilog module for the same with suitable diagram.
[BL: Understand| CO: 5|Marks: 7]

MODULE – V

7. (a) Outline the concepts of design environment and constraints while synthesizing Verilog code with suitable example. [BL: Understand| CO: 6|Marks: 7]

   (b) Describe about Moore detector in general and develop a test bench for Moore detector to control the delay. [BL: Understand| CO: 6|Marks: 7]

8. (a) Demonstrate the operation of a counter in general and also differentiate between asynchronous and synchronous counter with neat diagrams. [BL: Understand| CO: 6|Marks: 7]

   (b) Discuss about setup, hold, width and period checks used in Verilog. Write a Verilog module for D flip-flop using setup hold, width and period checks. [BL: Apply| CO: 6|Marks: 7]