Hall Ticket No | | | | | | | | | | | Question Paper Code: AECC44

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal-500043, Hyderabad

B.Tech VII SEMESTER END EXAMINATIONS (REGULAR) - DECEMBER 2023
Regulation: UG-20
VLSI DESIGN

Time: 3 Hours (ELECTRONICS AND COMMUNICATION ENGINEERING) **Max Marks: 70**

Answer ALL questions in Module I and II
Answer ONE out of two questions in Modules III, IV and V
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) Explain the following characteristics of MOS transistor:
   i) Transconductance g_m
   ii) Output conductance g_{ds}
   iii) Figure of merit ω_0 [BL: Understand| CO: 1|Marks: 7]

   (b) Compute the pull-up and pull-down ratio Z_{pu}/Z_{pd} for an nMOS inverter driven by another nMOS inverter. [BL: Apply| CO: 1|Marks: 7]

MODULE – II

2. (a) Discuss in detail about the scaling models and effect of scaling on any four parameters. [BL: Understand| CO: 2|Marks: 7]

   (b) Draw stick diagram of 2-input CMOS NOR gate and discuss in detail about lambda based layout design rules. [BL: Understand| CO: 2|Marks: 7]

MODULE – III

3. (a) Describe in detail the following
   i) Fringing field capacitance
   ii) Interlayer capacitance
   iii) Peripheral capacitance. [BL: Understand| CO: 3|Marks: 7]

   (b) Compute the resistivity of a substance which has resistance of 1000 Ω, if the length of the material is 4.0 cm and its cross-sectional area is 0.20 cm^2. [BL: Apply| CO: 3|Marks: 7]

4. (a) Why single phase dynamic circuits cannot be cascaded? How this problem is resolved in CMOS domino circuit? [BL: Understand| CO: 4|Marks: 7]

   (b) Explain the principal concept of clock skew? Justify why clocked CMOS is called as clock skew insensitive approach with necessary diagrams? [BL: Apply| CO: 4|Marks: 7]

MODULE – IV

5. (a) Summarize the 1-T dynamic RAM cell with necessary diagrams. Sketch data read-store and precharge phase using 1-T RAM cell. [BL: Understand| CO: 5|Marks: 7]

   (b) Draw a 4-bit x 4-bit NOR-based ROM array and explain its operation in detail [BL: Apply| CO: 5|Marks: 7]

6. (a) Illustrate with necessary diagrams the carry save adder. Justify why this adder is called as high speed adder. [BL: Analyze| CO: 5|Marks: 7]

   (b) Build a 4-bit x 4-bit barrel shifter. Why this shifter is not suitable for more than 4 bits? [BL: Understand| CO: 5|Marks: 7]

MODULE – V

7. (a) Demonstrate Xilinx XC 3000 CLB and explain in detail about CLB, IOB and programmable interconnect for FPGA. [BL: Understand| CO: 6|Marks: 7]

   (b) Implement the following Boolean expression using 3 input, 3 product terms and 2 outputs using PLA [BL: Apply| CO: 6|Marks: 7]

   F1= AC + BC

   F2= AC + AB'

8. (a) Explain about complex programmable logic devices (CPLDS) with necessary block diagram. Discuss whether CPLD's are volatile or non volatile? [BL: Understand| CO: 6|Marks: 7]

   (b) Categorize different approaches used for application specific integrated circuit (ASIC's). [BL: Understand| CO: 6|Marks: 7]