Hall Ticket No | | | | | | | | | | | Question Paper Code: AECC49

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal-500043, Hyderabad

B.Tech VII SEMESTER END EXAMINATIONS (REGULAR) - DECEMBER 2023
Regulation: UG-20

DIGITAL DESIGN THROUGH VERILOG

Time: 3 Hours **(ELECTRONICS AND COMMUNICATION ENGINEERING)** **Max Marks: 70**

Answer ALL questions in Module I and II
Answer ONE out of two questions in Modules III, IV and V
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) Discuss about continuous assignments and draw the characteristics of the assignment statement used in data flow modeling with a Verilog code. [BL: Understand| CO: 1|Marks: 7]

   (b) Design a full adder circuit using data flow modeling and write a test bench to verify the functionality of the full adder. [BL: Apply| CO: 1|Marks: 7]

MODULE – II

2. (a) List outgate delays. Explain the delays with neat sketches and instantiation syntax. [BL: Understand| CO: 2|Marks: 7]

   (b) Build an edge triggered JK flip flop with Asynchronous preset and clear as a UDP. [BL: Apply | CO: 2|Marks: 7]

MODULE – III

3. (a) Describe the delay based timing control models of behavioral modeling in detail. [BL: Understand| CO: 3|Marks: 7]

   (b) Write a Verilog program to design a 4-bit up/ down counter to perform upcount when selection bit is '1'and down count when the selection bit is '0'. [BL: Apply| CO: 3|Marks: 7]

4. (a) Differentiate between blocking and non blocking statements with necessary code example. [BL: Understand| CO: 4|Marks: 7]

   (b) Design an ALU to perform the following operations.
   i) Addition ii) Subtraction iii) Bit wise [BL: Apply| CO: 4|Marks: 7]

MODULE – IV

5. (a) Classify delays in CMOS switches. Give an example to instantiate a CMOS switch with different delays. [BL: Understand| CO: 5|Marks: 7]

   (b) Develop a CMOS D Flip flop and write a Verilog code using switch primitives. [BL: Apply| CO: 5|Marks: 7]

6. (a) Explain bi- directional switches with symbol and instantiation syntax in detail.
[BL: Understand| CO: 5|Marks: 7]

(b) Draw the circuit diagram for 2-input NAND gate. Write a Verilog code for the 2-input NAND gate using NMOS and PMOS constructs. [BL: Apply| CO: 5|Marks: 7]

MODULE – V

7. (a) Explain in detail about Assertion verification. Also give its benefits.
[BL: Understand| CO: 6|Marks: 7]

(b) Obtain a transition table and flow table for the asynchronous circuit with the function.
Y = x_1x_2+(x_1+x_2)y and z=y [BL: Apply| CO: 6|Marks: 7]

8. (a) What is race around condition? Classify race around condition types and explain with suitable example.
[BL: Understand| CO: 6|Marks: 7]

(b) Build a synchronous sequential machine for '110' sequence detector for which state diagram shown in Figure 1. Obtain state table and logic diagram. [BL: Apply| CO: 6|Marks: 7]

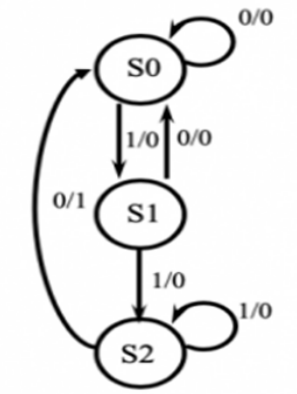

Figure 1

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