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Question Paper Code:ACSC07

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
(Dundigal-500043, Hyderabad)

B.Tech III SEMESTER END EXAMINATIONS (REGULAR) - FEBRUARY 2022
Regulation:UG-20

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours **(CSE|IT|AIML|DS|CS|CSIT)** **Max Marks: 70**

Answer ALL questions in Module I and II
Answer ONE out of two questions in Modules III, IV and V
NOTE: Provision is given to answer TWO questions from among one of the Modules III / IV / V
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) Demonstrate the architecture of a basic computer and explain what are the input and output operations in this architecture. **[7M]**
   (b) Describe about compiling process and assembly process with a neat flow diagram. **[7M]**

MODULE – II

2. (a) With a neat schematic explain the steps involved in fetch and decode phases using register transfer instructions. **[7M]**
   (b) Illustrate the basic requirements for input and output communication using a terminal unit such as keyboard and printer. **[7M]**

MODULE – III

3. (a) Explain the logical micro-operations which manipulates individual bits of word in register with examples. **[7M]**
   (b) Subtract single point precision floating point numbers A and B where A= 44900000 and B=42A00000H. **[7M]**
4. (a) Illustrate BCD adder which contains two four bit binary adders with the block diagram. **[7M]**
   (b) What do you mean by completeness of instruction set? Give the reasons to choose the instructions in each category. **[7M]**

MODULE – IV

5. (a) Briefly explain about block diagram of DMA controller. Identify the function of DMA I/O operation and also show the input/output processor. **[7M]**
   (b) What is virtual memory? Explain the relation between address space and memory space in a virtual memory system along with its memory table for mapping. **[7M]**.
6. (a) List the disadvantage of strobe method? Explain how handshake method solves the problem. **[7M]**
   (b) Explain direct memory access controller functionality with the block diagram. **[7M]**

MODULE – V

7. (a) Illustrate a processor with multiple functional units with a neat diagram. **[7M]**

   (b) What is instruction pipelining? What are the conflicts that occurred during instruction pipelining? Elaborate the major difficulties that cause the instruction pipeline to deviate from its normal operation. **[7M]**

8. (a) Write about multicomputers and multiprocessors and also write about the characteristics of multiprocessors. **[7M]**

   (b) Explain about inter process communication and synchronization in detail with neat sketch. **[7M]**

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