Hall Ticket No | | | | | | | | | | |

Question Paper Code:AECC03

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal-500043, Hyderabad

B.Tech III SEMESTER END EXAMINATIONS (REGULAR) - FEBRUARY 2022
Regulation:UG-20
DIGITAL SYSTEM DESIGN

Time: 3 Hours **(ECE)** **Max Marks: 70**

Answer ALL questions in Module I and II
Answer ONE out of two questions in Modules III, IV and V
NOTE: Provision is given to answer TWO questions from among one of the Modules III / IV / V
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) Perform the following subtraction using 2's complement.
   i) $(111)_2 - (100)_2 = (?)_2$
   ii) $(23)_{10} - (25)_{10} = (?)_2$ **[7M]**
   (b) Write short notes on binary number systems. Discuss 1's and 2's complement methods of subtraction and octal number system. **[7M]**

MODULE – II

2. (a) Explain half adder and half subtractor with the help of truth table, block diagram and logic diagram. **[7M]**
   (b) Design a single digit BCD adder using 4 bit parallel adder and external gates. Briefly explain the logic. **[7M]**

MODULE – III

3. (a) Explain the working of a SR latch using NOR gates with the help of logic diagram, truth table and write timing diagram. **[7M]**
   (b) Design a mod-6 counter whose counting sequence is 0→1→4→6→7→5→0 using positive edge triggered clocked JK flip-flops. Write state diagram, excitation table, K-map and logic diagram. **[7M]**
4. (a) Write and explain characteristic equation for the JK flip-flop with gate level block diagram. **[7M]**
   (b) Design a synchronous mod-6 counter using clocked T flip-flop for the following sequence 0→2→3→6→5→1→0 with the minimal combinational gating. **[7M]**

MODULE – IV

5. (a) Explain about various CMOS logic families. Describe the interfacing of CMOS with neat sketch. **[7M]**
   (b) Draw the circuit diagram of TTL NAND gate and explain its working with the help of a truth table. **[7M]**.

6. (a) Explain about TTL logic family. List the comparison between TTL with CMOS logic family. **[7M]**

   (b) Realize the following 2 switching functions with a 3-input, 3-output PROM.
   i) f_1(A, B, C) = AB + B'C
   ii) f_2(A, B, C) = (A + B' + C)(A' + B) **[7M]**

MODULE – V

7. (a) List and explain about libraries and packages in VHDL programming. List the advantages and disadvantages of VHDL. **[7M]**

   (b) Write dataflow VHDL code for binary to gray code conversion along with the truth table. **[7M]**

8. (a) Explain the different operators supported in VHDL and mention which operators are evaluated in order to their precedence. (i.e., highest to lowest) **[7M]**

   (b) Write dataflow code and behavioural code for half adder example in VHDL. **[7M]**

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