Hall Ticket No | | | | | | | | | | |

Question Paper Code:AECC07

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal-500043, Hyderabad

B.Tech III SEMESTER END EXAMINATIONS (REGULAR) - FEBRUARY 2022

Regulation:UG-20

ANALOG ELECTRONICS

Time: 3 Hours **(EEE)** **Max Marks: 70**

Answer ALL questions in Module I and II

Answer ONE out of two questions in Modules III, IV and V

NOTE: Provision is given to answer TWO questions from among one of the Modules III / IV / V

All Questions Carry Equal Marks

All parts of the question must be answered in one place only

MODULE – I

1. (a) Derive the expressions for current gain, voltage gain and input impedance of a CE amplifier. **[7M]**

   (b) A common emitter circuit has the following components R_1=27kΩ,R_2=27k Ω, R_e=5.6kΩ, R_L=47kΩ, Rs=600Ω. The transistor parameters are h_{ie}=1kΩ, h_{fe}=85 and h_{oe}=2μA/V. Determine A_i, R_i, A_v, R_o. **[7M]**

MODULE – II

2. (a) Explain the principle of CS amplifier with the help of circuit diagram. Derive the expressions for A_V, input impedance and output impedance. **[7M]**

   (b) A common source amplifier circuit with bypassed R_s has the following circuit parameters: R_d = 15K, R_S = 0.5K, R_g = 1M, r_d = 5K, g_m= 5mS and V_{DD} = 20 V. Determine A_V and R_O. **[7M]**

MODULE – III

3. (a) Draw the push-pull class-B power amplifier and explain its operation. Show that the maximum conversion efficiency is 78.5%. **[7M]**

   (b) Calculate the DC bias voltages, collector current voltage gain of each stage and the overall AC voltage gain for the BJT cascade amplifier circuit shown in Figure 1. **[7M]**

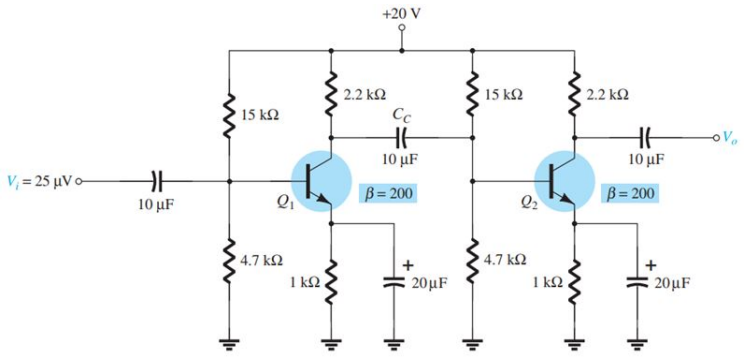

Figure 1

4. (a) Explain the classification of amplifiers with relevant sketches. **[7M]**

   (b) Calculate the efficiency of a transformer-coupled class A amplifier for a supply of 12 V and outputs of:

   i) V(p) = 12 V.

   ii) V(p) = 6 V.

   iii) V(p) = 2 V. **[7M]**

MODULE – IV

5. (a) Draw the circuit and explain the principle of operation of RC phase-shift oscillator. Derive the expression for the frequency of oscillations. **[7M]**

   (b) Identify the feedback topology and calculate the voltage gain with and without feedback for the circuit of Figure 2 with values of g_m = 5 mS, R_D = 5.1 kΩ, R_S = 1 kΩ, and R_F= 20 kΩ. **[7M]**

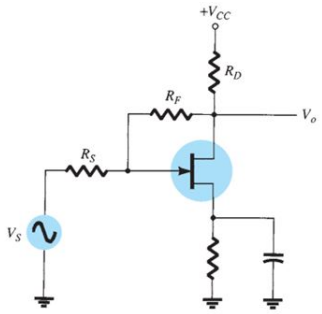

Figure 2

6. (a) Explain about Hartley oscillator. Illustrate the expression for the frequency of Hartley oscillators. **[7M]**

   (b) Determine the voltage gain, input, and output impedance with feedback for voltage-series feedback having A = -100, R_i = 10 kΩ and R_o = 20 kΩ for feedback of

   i) β=-0.1

   ii) β=-0.5. **[7M]**

MODULE – V

7. (a) Explain briefly about the following

   i) CMRR

   ii) Input offset voltage

   iii) Band width

   iv) Input bias current. **[7M]**

   (b) Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 1 KHz. If a sine wave of 1V peak at 1000 Hz is applied to this differentiator draw the output waveforms. **[7M]**

8. (a) Explain the operation of a square wave generator using op-amp with a neat circuit diagram and relevant waveforms. **[7M]**

   (b) Find R_1 and R_f in the lossy integrator so that the peak gain is 20dB and the gain is 3dB down from its peak when ω= 10,000 rad/sec. use a capacitance of 0.01micro farads. **[7M]**

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