



INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal-500043, Hyderabad

B.Tech III SEMESTER END EXAMINATIONS (REGULAR / SUPPLEMENTARY) - FEBRUARY 2023

Regulation:UG20

ELECTRONIC DEVICES AND CIRCUITS

Time: 3 Hours (ELECTRONICS AND COMMUNICATION ENGINEERING)

Max Marks: 70

Answer ALL questions in Module I and II

Answer ONE out of two questions in Modules III, IV and V

All Questions Carry Equal Marks

All parts of the question must be answered in one place only

MODULE – I

- (a) Summarize the following terms with respect to P-N junction diode
 - Transition capacitance
 - Diffusion capacitance.

[BL: Understand| CO: 1|Marks: 7]
- (b) Sketch the output V_o and determine the DC level of the output for the network of Figure 1. Also sketch, if the ideal diode is replaced by a silicon diode.

[BL: Apply| CO: 1|Marks: 7]

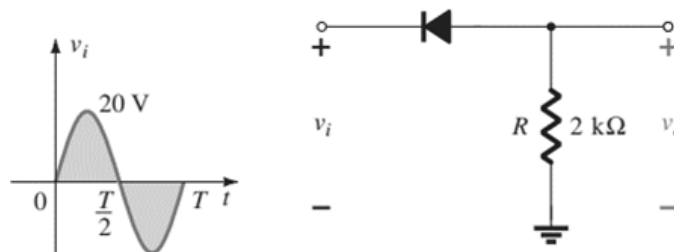


Figure 1

MODULE – II

- (a) Describe the working of NPN transistor in common base configuration and draw its input and output characteristics.

[BL: Understand| CO: 2|Marks: 7]
- (b) The reverse leakage current of the transistor when connected in CB configuration is $0.2 \mu\text{A}$ and it is $18 \mu\text{A}$ when the same transistor is connected in CE configuration. Calculate α_{dc} and β_{dc} of the transistor. (Assume $I_B = 30 \mu\text{A}$)

[BL: Apply| CO: 2|Marks: 7]

MODULE – III

- (a) What is operating point of the transistor? Explain the junction conditions required for the transistor operated in active, saturation and cut-off region.

[BL: Understand| CO: 3|Marks: 7]
- (b) Determine the following for the fixed-bias configuration of Figure 2
 - I_B and I_{CQ}
 - V_{CEQ}
 - V_B and V_C
 - V_{BC}

[BL: Apply| CO: 3|Marks: 7]

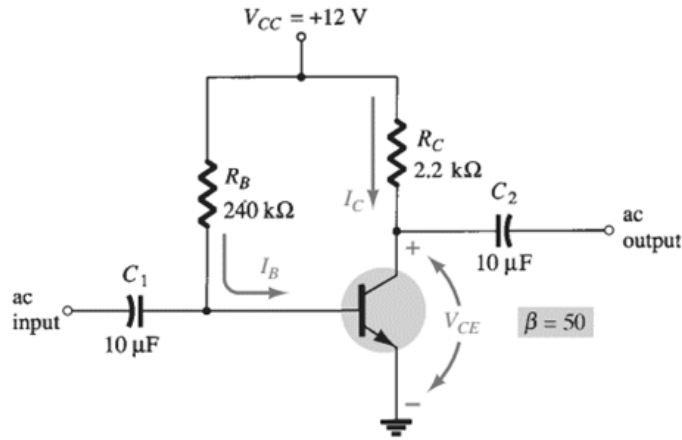


Figure 2

4. (a) Outline the circuit diagram of BJT emitter-bias configuration. What is the significance of emitter resistor used in this configuration? [BL: Understand| CO: 4|Marks: 7]
- (b) For the load line and the defined Q-point of Figure 3, determine the required values of V_{CC} , R_C and R_B for a fixed-bias configuration. [BL: Apply| CO: 4|Marks: 7]

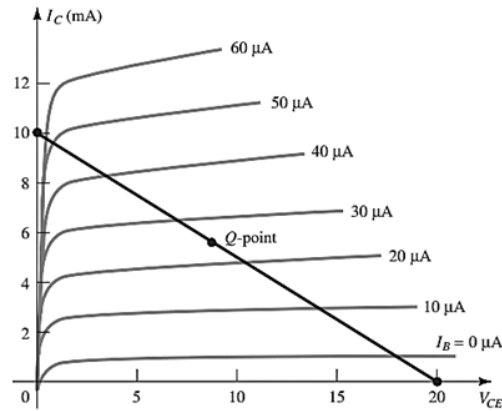


Figure 3

MODULE – IV

5. (a) With a neat drain and transfer characteristics, explain the significance of gate to source voltage in n-channel depletion-type FET. [BL: Understand| CO: 5|Marks: 7]
- (b) An N-channel JFET has $I_{DSS} = 8\text{mA}$ and $V_P = -5\text{V}$. Determine the minimum value of V_{DS} for pinch-off region and the drain current I_{DS} for $V_{GS} = -2\text{V}$ in the pinch-off region. [BL: Apply| CO: 5|Marks: 7]
6. (a) Explain the operation of fixed-bias configuration for the n-channel JFET with neat circuit diagram and relevant current and voltage equations. [BL: Understand| CO: 5|Marks: 7]
- (b) Determine the following parameters for the network shown in Figure 4, (Assume $I_D = 4\text{mA}$)
 i) V_{GSQ} ii) I_{DQ} iii) V_{DS} iv) V_s . [BL: Apply| CO: 5|Marks: 7]

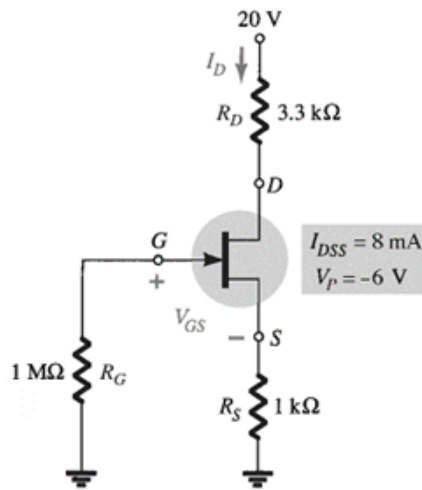


Figure 4

MODULE – V

7. (a) Illustrate the V-I characteristics of zener diode and analyse avalanche and Zener breakdown mechanisms. [BL: Understand| CO: 6|Marks: 7]
- (b) A Zener voltage regulator circuit is to maintain constant voltage at 60V, over a current range from 5 to 50mA. The input supply voltage is 200 V. find the value of resistance R to be connected in the circuit, for voltage regulation from load current $I_L = 0$ mA to I_L max, the maximum possible value of I_L . Show the value I_{Lmax} . [BL: Apply| CO: 6|Marks: 7]
8. (a) With a neat two-transistor analogy diagram, explain the regenerative action of silicon control rectifier. [BL: Understand| CO: 6|Marks: 7]
- (b) In common drain amplifier, let $R_s = 4$ kΩ, $R_G = 10$ MΩ, $\mu = 50$, and $r_d = 85$ kΩ. Solve the voltage gain A_V , input impedance Z_i and output impedance Z_O . [BL: Apply| CO: 4|Marks: 7]

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