Time: 3 Hours (Electronics and communication engineering) Max Marks: 70

## Answer ALL questions in Module I and II

Answer ONE out of two questions in Modules III, IV and V
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

## MODULE - I

1. (a) Differentiate between weighted and non-weighted codes. Explain the procedure to convert the expression $\mathrm{F}=\mathrm{a}+\mathrm{b}$ 'c in sum of min terms.
[BL: Understand| CO: 1|Marks: 7]
(b) Why the gray code is called as reflected binary code? Simplify the Boolean function F $(\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D})=\sum(0,1,2,6,8,9,10)$ using K-Map.
[BL: Apply| CO: 1|Marks: 7]

## MODULE - II

2. (a) Distinguish between serial adder and parallel adder. Construct a full adder circuit using logic gates. [BL: Understand| CO: 2|Marks: 7]
(b) Enumerate the procedure to design 4:1 multiplexer. Write the truth table and circuit diagram using logic gates.
[BL: Apply| CO: 2|Marks: 7]

## MODULE - III

3. (a) How do you build a latch using universal gates? Explain the working of pseudo random binary sequence generator.
[BL: Understand| CO: 3|Marks: 7]
(b) Outline the operation of 4-bit shift register in SISO mode. Design a 4 bit SISO shift register and give a sample input and output.
[BL: Apply| CO: 3|Marks: 7]
4. (a) Classify different types of latches. Describe the design procedure of synchronous finite state machine (FSM).
[BL: Understand| CO: 4|Marks: 7]
(b) Draw the characteristic table of gated D-Latch. Develop a 3 bit synchronous down counter using JK flip-flop.
[BL: Apply| CO: 4|Marks: 7]

## MODULE - IV

5. (a) Summarize the following terms
i) Noise margin
ii) Propagation delay
iii) Fan-in
iv) Fan-out
v) Time delay.
[BL: Understand| CO: 5|Marks: 7]
(b) Implement the following boolean functions using PROM
i) $F_{1}=\sum(1,2)$
ii) $F_{2}=\sum(0,1,3)$.
[BL: Apply| CO: 5|Marks: 7]
6. (a) Differentiate between TTL and CMOS logic families. Explain about complementary metal oxide semiconductor.
[BL: Understand| CO: 5|Marks: 7]
(b) Implement the following boolean functions using PAL
i) $F_{1}=\mathrm{AB}^{\prime}+\mathrm{AC}+\mathrm{A}^{\prime} \mathrm{BC}^{\prime}$
ii) $F_{2}=\mathrm{AC}+\mathrm{BC}$
[BL: Apply| CO: 5|Marks: 7]

## MODULE - V

7. (a) Compare behavioral and structural models. Discuss various datatypes in VHDL with examples.
[BL: Understand| CO: $6 \mid$ Marks: 7 ]
(b) List out the seven classes of VHDL operators according to their precedence. Write a VDHL code to design half adder and half substractor circuit.
[BL: Apply| CO: 6|Marks: 7]
8. (a) How to delete component in VHDL programming? Describe the design flow of VHDL with neat diagram.
[BL: Understand| CO: 6|Marks: 7]
(b) Write a VHDL code for positive edge triggered D flip flop with active high reset Asynchronous input using guarded block statement.
[BL: Apply| CO: 6|Marks: 7]

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