Hall Ticket No | | | | | | | | | | | Course Code: AECC08

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

B.Tech III SEMESTER END EXAMINATIONS (REGULAR / SUPPLEMENTARY) - FEBRUARY 2023

Regulation: UG20

ANALOG AND DIGITAL ELECTRONICS

Time: 3 Hours **Common to (CSE | CSE (AI&ML) | CSE (CS) | CSIT | IT)** **Max Marks: 70**

Answer ALL questions in Module I and II
Answer ONE out of two questions in Modules III, IV and V
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) With neat circuit diagram, explain V-I characteristics of PN junction diode under forward and reverse bias conditions. [BL: Understand| CO: 1|Marks: 7]

   (b) A full-wave rectifier uses two diodes, the internal resistance of each diode is at 20 Ω. The transformer RMS voltage from centre tap to each end of secondary is 50 V and load resistance is 980 Ω. Find

   i) The DC value of current

   ii) The RMS value of current.

   iii) Ripple factor

   iv) Efficiency [BL: Apply| CO: 1|Marks: 7]

MODULE – II

2. (a) Illustrate the input and output characteristics of an NPN transistor in CE configuration with a circuit diagram . [BL: Understand| CO: 2|Marks: 7]

   (b) The h-parameters of a transistor used in a CE circuit are $h_{ie} = 1k\Omega$, $h_{re} = 1\times10^{-4}$, $h_{fe} = 50$, and h_{oe} =100$\mu\mho$. The load resistor for the transistor is 1kΩ in the collector circuit. Determine the value of i) Input & output resistance ii) Current gain iii) Voltage gain. [BL: Apply| CO: 2|Marks: 7]

MODULE – III

3. (a) Tabulate any three weighted and one non weighted code values for the decimal numbers 1 to 9. [BL: Understand| CO: 3|Marks: 7]

   (b) Convert the following

   i) 11110010_2 to octal

   ii) $(010101)_2$ to decimal

   iii) $14B.032_H$ to decimal

   iv) 56.79_{10} to hexadecimal [BL: Apply| CO: 3|Marks: 7]

4. (a) Draw the truth table of logic gates. Build basic gates AND, NOT, OR using NAND and NOR gate. [BL: Understand| CO: 4|Marks: 7]

   (b) Simplify $(A+B)^{'}(A^{'}+B^{'})^{'}$. Implement $Y = (AB^{'} + A^{'}B)(C + D^{'})$ using only NAND gates. [BL: Apply| CO: 4|Marks: 7]

MODULE – IV

5. (a) Design a full subtractor circuit by using K-map method and draw the logic diagram. [BL: Apply| CO: 5|Marks: 7]

   (b) Simplify the Boolean function
   F (w,x,y,z)=$\sum$ (0,1,2,4,5,6,8,9,12,13,14) using K-Map. [BL: Apply| CO: 5|Marks: 7]

6. (a) What is multiplexer? Draw circuit diagram of 8:1 multiplexer and explain its working. [BL: Understand| CO: 5|Marks: 7]

   (b) Find the prime implicants for the following function
   $F(A, B, C, D) = \sum(0, 1, 2, 8, 10, 11, 14, 15)$ using tabular method. [BL: Apply| CO: 5|Marks: 7]

MODULE – V

7. (a) Draw the block diagram of a 4 bit universal shift register and explain its working with function table. [BL: Understand| CO: 6|Marks: 7]

   (b) Design a 4-bit ring counter using D- flip flops with relevant timing diagrams and explain in detail. [BL: Apply| CO: 6|Marks: 7]

8. (a) Demonstrate the working of clocked JK flipflop and RS flip-flop using NAND gates with suitable diagrams. [BL: Understand| CO: 6|Marks: 7]

   (b) Differentiate between combinational and sequential circuits. Design a 3 bit SISO shift register using D flip-flop. [BL: Apply| CO: 6|Marks: 7]

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