Hall Ticket No | | | | | | | | | | |

Question Paper Code: ACSC07

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal-500043, Hyderabad

B.Tech III SEMESTER END EXAMINATIONS (REGULAR/ SUPPLEMENTARY) - FEBRUARY 2024
Regulation: UG20

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours **(CSE | CSE (AI&ML) | CSE (DS) | CSE (CS) | CSIT | IT)** **Max Marks: 70**

Answer ALL questions in Module I and II
Answer ONE out of two questions in Modules III, IV and V
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) List and explain the process of components involved in the organization of a digital computer. [BL: Understand| CO: 1|Marks: 7]

   (b) Illustrate the following arithmetic expression using three and two address instructions.
   X= (A+B) * (C+D) [BL: Apply| CO: 1|Marks: 7]

MODULE – II

2. (a) Describe in detail about the list of operations involved in logic micro operations with its symbolic notations. [BL: Understand| CO: 2|Marks: 7]

   (b) Design a 4 bit arithmetic circuit by using 4x1 MUX and two select lines for the following operations.
   i) Addition
   ii) Subtraction
   iii) Increment and
   iv) Decrement.

   [BL: Apply| CO: 2|Marks: 7]

MODULE – III

3. (a) Draw flowchart and explain addition and subtraction of floating point numbers in detail. [BL: Understand| CO: 3|Marks: 7]

   (b) Find the suitable addressing mode type for the below instructions.
   i) MOV R #20
   ii) CMA
   iii) ADD X
   iv) ADD 10
   v) ADD AL,[0302]
   vi) Add R1, (R2)+
   vii) Add R1,-(R2) [BL: Apply| CO: 3|Marks: 7]

4. (a) List the phases involved in an instruction cycle. Explain how the control determines the suitable instruction type with a flow diagram? [BL: Understand| CO: 4|Marks: 7]

   (b) Convert the following pairs of decimal numbers to 5-bit 2's-complement numbers, and then perform addition and subtraction on each pair. Indicate whether or not overflow occurs for each case?

   i) 7 and 13

   ii) −12 and 9 [BL: Apply| CO: 4|Marks: 7]

MODULE – IV

5. (a) Compare paging and segmentation mechanisms for implementing the virtual memory. [BL: Understand| CO: 5|Marks: 7]

   (b) A digital computer has a memory unit of 64K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of 4 words.

   i) How many bits are there in the tag, index, block and word fields of the address format?

   ii) How many bits are there in each word of the cache, and how are they divided into functions? Include the valid bit.

   iii) How many blocks can the cache accommodate? [BL: Apply| CO: 5|Marks: 7].

6. (a) Illustrate the mapping process involved in transformation of data from main to cache memory. [BL: Understand| CO: 5|Marks: 7]

   (b) Draw an interface unit which communicates CPU with DMA through address and data buses with neat sketch [BL: Apply| CO: 5|Marks: 7]

MODULE – V

7. (a) Compare time shared common bus and multiport memory bus based on its interconnection structures with neat diagram [BL: Understand| CO: 6|Marks: 7]

   (b) Consider the four instructions in the following program. The first instruction starts from step 1 in the pipeline used. Specify what operations are performed in the four segments during step 4.?

   Load R1 <—- M [312]

   ADD R2 <—- R2 + R2 + M [313]

   INC R3 <—— R3 + 1

   STORE M [314] <— R3 [BL: Apply| CO: 6|Marks: 7]

8. (a) Explain how the instruction cycle in the CPU can be processed with a four segment pipeline with timing diagram? [BL: Understand| CO: 6|Marks: 7]

   (b) A nonpipeline system takes 50 ns to process a task. The same task can be processed in a 6 segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved [BL: Apply| CO: 6|Marks: 7]