Hall Ticket No | | | | | | | | | | |

Question Paper Code: AECC01

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal-500043, Hyderabad

B.Tech III SEMESTER END EXAMINATIONS (REGULAR/ SUPPLEMENTARY) - FEBRUARY 2024
Regulation: UG20
ELECTRONIC DEVICES AND CIRCUITS

Time: 3 Hours **(ELECTRONICS AND COMMUNICATION ENGINEERING)** **Max Marks: 70**

Answer ALL questions in Module I and II
Answer ONE out of two questions in Modules III, IV and V
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) Describe the concept of diffusion capacitance in a diode and relate the dynamic behavior of the diode when the applied voltage changes. [BL: Understand| CO: 1|Marks: 7]

   (b) An AC supply of 230 V is applied to a half-wave rectifier circuit shown in Figure 1 through a transformer of turns ratio 10 : 1. Find

   i) The output DC voltage

   ii) The peak inverse voltage.

   Assume the diode to be ideal. [BL: Apply| CO: 1|Marks: 7]

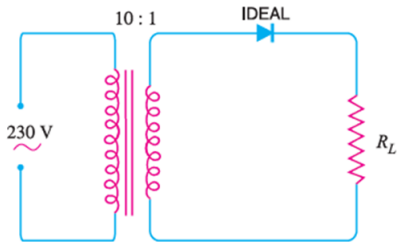

Figure 1

MODULE – II

2. (a) Summarize the performance characteristics of CB, CE, and CC configurations with the help of tabulation. [BL: Understand| CO: 2|Marks: 7]

   (b) A silicon transistor with $V_{BE} = 0.7$V, $\alpha = 0.98$ and collector cut-off current of 10μ A. Assume R_C=2KΩ, $V_{CC} = 12$V and $I_B = 10$µA. solve β, I_{CE0}, I_C, I_E and V_{CE}.

   [BL: Apply| CO: 2|Marks: 7]

MODULE – III

3. (a) Discuss the impact of temperature variations on the collector-to-base bias circuit. How does it maintain stability in different conditions? [BL: Understand| CO: 3|Marks: 7]

(b) Design a fixed-biased circuit using a silicon transistor as given in Figure 2 having β value of 100, V_{cc} is 10V and DC bias conditions are to be $V_{CE} = 5$ V and $I_C = 5$ mA.

[BL: Apply| CO: 3|Marks: 7]

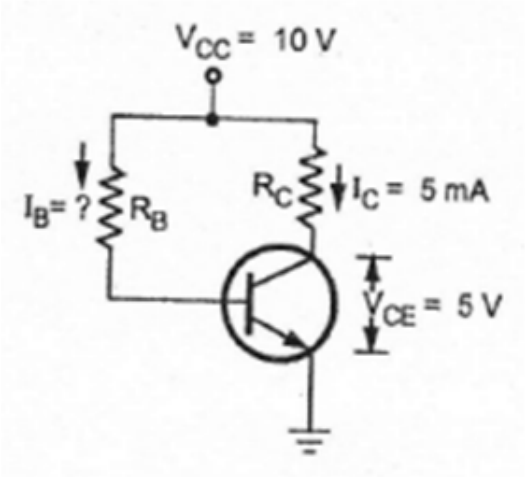

Figure 2

4. (a) Discuss the function of the emitter bypass capacitor in the low-frequency response of a common emitter amplifier. [BL: Understand| CO: 4|Marks: 7]

(b) The silicon transistor shown in Figure 3 has $\beta = 100$ is biased by base resistor method. Draw the DC load line and determine the operating point. What is the stability factor?

[BL: Apply| CO: 4|Marks: 7]

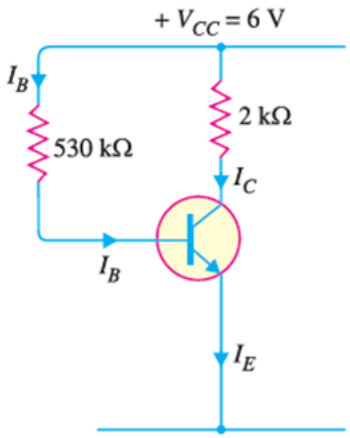

Figure 3

MODULE – IV

5. (a) Demonstrate the construction and principle of operation on n channel JFET with its characteristics. [BL: Understand| CO: 5|Marks: 7]

(b) For the JFET shown in the Figure 4, V_{GS} (off) = – 4V and $I_{DSS} = 12$ mA. Determine the minimum value of V_{DD} required to put the device in the constant-current region of operation.

[BL: Apply| CO: 5|Marks: 7].

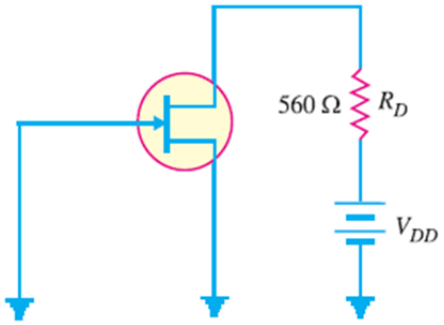

Figure 4

6. (a) Demonstrate the connection and configuration of an FET to function as a voltage variable resistor.
[BL: Understand| CO: 5|Marks: 7]

   (b) Determine the value of the drain current for the circuit shown in Figure 5
[BL: Apply| CO: 5|Marks: 7]

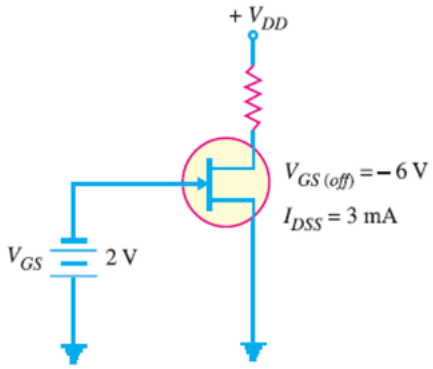

Figure 5

MODULE – V

7. (a) Design a self biasing network for a CS JFET amplifier circuit and derive the expression for gain and input resistance. [BL: Understand| CO: 6|Marks: 7]

   (b) A FET amplifier in the common-source configuration uses a load resistance of 500 kΩ. The ac drain resistance of the device is 100 kΩ and the transconductance is 0.8 mAV^{-1}. Calculate the voltage gain of the amplifier.
[BL: Apply| CO: 6|Marks: 7]

8. (a) Explain the significance of the Zener breakdown voltage in the contextof Zener diodes.
[BL: Understand| CO: 6|Marks: 7]

   (b) Determine the magnitude of I_D for a JFET with I_{DSS} = 8 mA and V_P = -4 V at the following DC bias points:
   i) V_{GS} = -0.5 V
   ii) V_{GS} = -1.5 V
   iii) V_{GS} = -2.5 V
[BL: Apply| CO: 6|Marks: 7]