Hall Ticket No | | | | | | | | | | |

Question Paper Code: AECC03

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal-500043, Hyderabad

B.Tech III SEMESTER END EXAMINATIONS (REGULAR/ SUPPLEMENTARY) - FEBRUARY 2024
Regulation: UG20

DIGITAL SYSTEM DESIGN

Time: 3 Hours **(ELECTRONICS AND COMMUNICATION ENGINEERING)** **Max Marks: 70**

Answer ALL questions in Module I and II
Answer ONE out of two questions in Modules III, IV and V
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) Outline the procedure of binary to gray and gray to binary code conversions. [BL: Understand| CO: 1|Marks: 7]

   (b) Simplify the Boolean function F(A, B, C, D) = $\sum$ (0, 2, 4, 5, 6, 7, 8, 10, 13, 15) using K-Map and realize logic diagram using NAND gate. [BL: Apply| CO: 1|Marks: 7]

MODULE – II

2. (a) Implement an 8-to-3 priority encoder. Describe the concept of priority encoding and discuss its applications. [BL: Understand| CO: 2|Marks: 7]

   (b) Draw a simple 4-bit ALU capable of performing addition, subtraction, AND, OR, and XOR operations. Discuss the control lines necessary for selecting different operations and optimizing for speed and area. [BL: Apply| CO: 2|Marks: 7]

MODULE – III

3. (a) Describe the working principle of an S-R flip-flop. What are the challenges associated with the SR flip-flop, and how can undesired states be avoided? [BL: Understand| CO: 3|Marks: 7]

   (b) Explain how data is loaded into the register and shifted out. Design a 4-bit serial-in, parallel-out shift register. [BL: Apply| CO: 3|Marks: 7]

4. (a) Summarize the concept of algorithmic state machines (ASMs) in digital design. How do ASMs aid in the design and description of complex sequential circuits? [BL: Understand| CO: 4|Marks: 7]

   (b) Design a 3-bit synchronous counter using T flip-flops. Discuss the advantages of synchronous counters in terms of speed and reliability. [BL: Apply| CO: 4|Marks: 7]

MODULE – IV

5. (a) Elaborate on the stages encompassing logic design, synthesis and the deployment of the configuration onto the FPGA hardware. [BL: Understand| CO: 5|Marks: 7]

   (b) Compare the characteristics of ECL and CMOS logic families, including speed, power consumption, and noise immunity. In what scenarios would you choose one over the other? [BL: Understand| CO: 5|Marks: 7].

6. (a) Discuss how you would apply tristate logic in the design of a digital system using TTL gates. [BL: Understand| CO: 5|Marks: 7]

   (b) Compare ASIC and PLD's. Implement the following function in PLA
   i) $F_1 = \sum$m(1,2,4,6); $F_2 = \sum$m(0,1,6,7); $F_3 = \sum$m(2,6)
   ii) $F_1 = \sum$m(3,5,8,9); $F_2 = \sum$m(2,3,5,8,); $F_3 = \sum$m(0,1) [BL: Apply| CO: 5|Marks: 7]

MODULE – V

7. (a) Describe the fundamental concepts of a finite state machine. How are states, transitions, and outputs defined in an FSM? [BL: Understand| CO: 6|Marks: 7]

   (b) Apply dataflow modeling in VHDL by presenting a scenario where logical operations and signal assignments are expressed using this modeling style. [BL: Apply| CO: 6|Marks: 7]

8. (a) What is meant by 'inertial' and 'transport' delays? Give an example of how each would be described in a VHDL model? [BL: Understand| CO: 6|Marks: 7]

   (b) Design a behavioral VHDL model of a positive edge triggered JK flipflop with reset. [BL: Apply| CO: 6|Marks: 7]