Hall Ticket No | | | | | | | | | | | Question Paper Code:AECC12

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal-500043, Hyderabad

B.Tech IV SEMESTER END EXAMINATIONS (REGULAR) - JULY 2022
Regulation:UG20
IC APPLICATIONS

Time: 3 Hours (ELECTRONICS AND COMMUNICATION ENGINEERING) **Max Marks: 70**

Answer ALL questions in Module I and II
Answer ONE out of two questions in Modules III, IV and V
(NOTE: Provision is given to answer TWO questions from among one of the Modules III / IV / V
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) Compare and contrast the DC and AC characteristics of an ideal op-amp with relevant expressions. [BL: Understand| CO: 1|Marks: 7]

   (b) Design the dual input balanced output differential amplifier to meet the following specifications and draw the circuit with designed values. $R_c = 2.2K\Omega, R_E = 4.7K\Omega, R_{in1} = R_{in2} = 50\Omega$, $+V_{cc} = +10V, -V_{EE} = -10V$ and the transistor is the CA 3086 with $\beta_{dc} = \beta_{ac} = 100$ and $V_{BE} = 0.715V$ typically. i) Determine the I_{cq} and VC_{Eq}
   ii) Determine voltage gain
   iii) Determine the input and output resistances [BL: Apply| CO: 1|Marks: 7]

MODULE – II

2. (a) Construct the circuit diagram of differentiator using op-amp and explain its operation with relevant wave forms [BL: Apply| CO: 2|Marks: 7]

   (b) Build an instrumentation amplifier to have a variable differential gain in the range 5-20dB. Use a 50 kilo-ohm potentiometer. [BL: Apply| CO: 2|Marks: 7]

MODULE – III

3. (a) With the help of schematic diagram of IC 555 timer, explain how it can be used as mono stable multivibrator and astable multivibrator. [BL: Understand| CO: 3|Marks: 7]

   (b) Model the 1KHz square wave form generator using IC 555 timer for duty cycle i) D=25% ii) D=50% and draw the waveforms. [BL: Apply| CO: 3|Marks: 7]

4. (a) Demonstrate the circuit diagram of first order high pass filter and its frequency response. Derive the expression for output voltage. [BL: Understand| CO: 4|Marks: 7]

   (b) Compute the free running frequency f_o, lock in range and capture range of PLL. Assume $R_T = 20k\Omega, C_T = 0.01\mu F$, $C = 1\mu F$ and supply voltage is ± 6v. [BL: Apply| CO: 4|Marks: 7]

MODULE – IV

5. (a) Draw the circuit of weighted resistor DAC and derive expression for output analog voltage V_0 [BL: Understand| CO: 5|Marks: 7]

   (b) Consider a 10 bit D/A converter having a reference voltage of 10 V. What is the binary digital input needed to get 4.5 V output? What outputs are obtained from the converter for the inputs of i) Binary 0010110101 ii) decimal 520? [BL: Apply| CO: 5|Marks: 7]

6. (a) Explain the working of a dual slope A/D converter. Enlist the advantages and disadvantages of dual slope ADC. [BL: Understand| CO: 5|Marks: 7]

   (b) Least significant bit of a 9-bit DAC is represented by 19.6 mv. If an input of 9 zero bits is represented by 0 volts.

   i) Find the output of the DAC for an input 10110 1101 and 01101 1011?

   ii) What is the full scale reading (FSR) of this DAC? [BL: Apply| CO: 5|Marks: 7]

MODULE – V

7. (a) Write short notes on Ring Counter and Johnson counter. Discuss the logic levels and noise margin with reference to TTL family. [BL: Understand| CO: 6|Marks: 7]

   (b) List the parameters which are used to compare logic families. Design a 4-bit bidirectional shift register with parallel load [BL: Apply| CO: 6|Marks: 7]

8. (a) What is the necessity of separate interfacing circuit to connect CMOS gate to TTL gate? Draw the interface circuit and explain the operation. [BL: Understand| CO: 6|Marks: 7]

   (b) Illustrate the CMOS transmission gate and realize a 2×1 MUX using this transmission gate. [BL: Apply| CO: 6|Marks: 7]