Hall Ticket No | | | | | | | | | | | Question Paper Code:AECC16

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal-500043, Hyderabad

B.Tech IV SEMESTER END EXAMINATIONS (REGULAR) - JULY 2022
Regulation:UG20
DIGITAL ELECTRONICS

Time: 3 Hours (ELECTRICAL AND ELECTRONICS ENGINEERING) Max Marks: 70

Answer ALL questions in Module I and II
Answer ONE out of two questions in Modules III, IV and V
(NOTE: Provision is given to answer TWO questions from among one of the Modules III / IV / V
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

MODULE – I

1. (a) Draw the circuit of two input CMOS NAND gate and explain the operation of it. [BL: Understand| CO: 1|Marks: 7]

   (b) For the logic expression Y=A$\overline{B}$ + $\overline{A}$ B, obtain the truth table. Realize this operation using basic gates and using NAND gates. [BL: Apply| CO: 1|Marks: 7]

MODULE – II

2. (a) Design half adder and half subtracter circuit using NAND gates. State the truth tables. [BL: Apply| CO: 2|Marks: 7]

   (b) Implement the following function F(A,B,C,D)=$\sum$m(0,1,3,4,8,9,15) using 8x1 MUX. [BL: Apply| CO: 2|Marks: 7]

MODULE – III

3. (a) Explain the operation of the clocked SR flip flop using NAND gates. Write the characteristic equation of SR flip flop. [BL: Understand| CO: 3|Marks: 7]

   (b) Design a synchronous counter that goes through states 0, 3, 5, 6, 0…..using T flip-flops and state the flow of sequence using excitation table. [BL: Apply| CO: 3|Marks: 7]

4. (a) List the advantages and disadvantages of Johnson counter. Explain the operation of 4 bit Johnson counter and 4 bit ring counter. [BL: Understand| CO: 4|Marks: 7]

   (b) Design a MOD-10 asynchronous up counter using T Flip Flop and explain with timing waveforms. [BL: Apply| CO: 4|Marks: 7]

MODULE – IV

5. (a) Explain the R-2R ladder digital to analog converters with suitable circuit diagrams. [BL: Understand| CO: 5|Marks: 7]

   (b) With the help of circuit diagram and functional table, explain the working of parallel comparator A/D converter. [BL: Understand | CO: 5|Marks: 7]

6. (a) What is need for data converters? Discuss the various specifications of digital to analog converter. [BL: Understand| CO: 5|Marks: 7]

(b) With a neat block diagram, explain in detail about successive approximation type analog to digital converter. [BL: Apply| CO: 5|Marks: 7]

MODULE – V

7. (a) Explain the operation of the charge coupled memory device with charge transfer plots and clock waveform. [BL: Understand| CO: 6|Marks: 7]

   (b) What is three state buffer? Obtain a 2048x8 memory using 256x8 memory chips. [BL: Apply| CO: 6|Marks: 7]

8. (a) Give the comparison between PAL and PLA. Explain PAL with the help of diagram. [BL: Understand| CO: 6|Marks: 7]

   (b) Implement the following Boolean functions with a PLA
   i) F1(A,B,C) = $\overline{A}$ BC + A$\overline{B}$ C + A$\overline{C}$
   ii) F2(A,B,C) = $\overline{A}$ $\overline{B}$ $\overline{C}$+ BC [BL: Apply| CO: 6|Marks: 7]

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