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INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal-500043, Hyderabad

B.Tech IV SEMESTER END EXAMINATIONS (REGULAR) - JULY 2022

Regulation:UG20

DIGITAL DESIGN THROUGH VERILOG

Time: 3 Hours (ELECTRONICS AND COMMUNICATION ENGINEERING) Max Marks: 70

Answer ALL questions in Module I and II

Answer ONE out of two questions in Modules III, IV and V

(NOTE: Provision is given to answer TWO questions from among one of the Modules III / IV / V

All Questions Carry Equal Marks

All parts of the question must be answered in one place only

MODULE – I

1. (a) Explain in detail about the unary, binary & ternary operators in verilog with examples.
[BL: Understand| CO: 1|Marks: 7]
- (b) Distinguish between tasks and functions. Design 2-bit comparator and write the dataflow verilog module.
[BL: Apply| CO: 1|Marks: 7]

MODULE – II

2. (a) Describe the following relevant to gate level modelling with necessary syntax and example.
i) Gate delays ii) Array of instances [BL: Understand| CO: 2|Marks: 7]
- (b) Give a gate level description of a 2-4 decoder circuit with relevant logic diagram and Verilog HDL source code.
[BL: Apply| CO: 2|Marks: 7]

MODULE – III

3. (a) Illustrate the while & for loop statements used in Verilog with syntax and example.
[BL: Understand| CO: 3|Marks: 7]
- (b) Write the behavioral model for 4 to 2-line priority encoder (highest priority to LSB) with valid bit output using case statement. Plot the simulated output.
[BL: Apply| CO: 3|Marks: 7]
4. (a) Compare the following and illustrate with example:
i) Initial with always block
ii) Blocking with non-blocking assignment statements. [BL: Understand| CO: 4|Marks: 7]
- (b) List the difference between a sequential block and parallel block with an example verilog code.
[BL: Understand| CO: 4|Marks: 7]

MODULE – IV

5. (a) Summarize the switch level primitives and give their instantiations. Draw the basic switch circuit and its Verilog HDL code. [BL: Understand| CO: 5|Marks: 7]
- (b) Design 2 to 1 line MUX using CMOS switches and write the transistor level Verilog code. [BL: Apply| CO: 5|Marks: 7]
6. (a) Explain about CMOS switch and Bi-directional gates related to switch level modelling in Verilog HDL. [BL: Understand| CO: 5|Marks: 7]
- (b) Give an example of 4 to 1 multiplexer built using UDPs. Write the switch level modeling for the following Boolean expression: $Y = [(A + B)C]'$. [BL: Apply| CO: 5|Marks: 7]

MODULE – V

7. (a) Explain the design environment and constraints while synthesizing verilog code with an example. [BL: Understand| CO: 6|Marks: 7]
- (b) Enumerate sequential circuit testing. Write a test bench for moore detector to control the delay. [BL: Apply| CO: 6|Marks: 7]
8. (a) Illustrate the synthesis of synchronous sequential machines with example. Differentiate between asynchronous and synchronous counter. [BL: Understand| CO: 6|Marks: 7]
- (b) Draw an asynchronous sequential machine chart to describe a state machine that detects a sequence of three logic 1s occurring at the input and that asserts a logic 1 at the output during the last state of the sequence. Write a two process Verilog HDL description to the state machine. [BL: Apply| CO: 6|Marks: 7]

