# INSTITUTE OF AERONAUTICAL ENGINEERING
### (Autonomous)
### Dundigal-500043, Hyderabad

**B.Tech VI SEMESTER END EXAMINATIONS (REGULAR) - JULY 2023**
**Regulation: UG-20**
## COMPUTER ARCHITECTURE

Time: 3 Hours        (COMMON TO ECE | EEE)        Max Marks: 70

**Answer ALL questions in Module I and II**
**Answer ONE out of two questions in Modules III, IV and V**
**All Questions Carry Equal Marks**
**All parts of the question must be answered in one place only**

## MODULE – I

1. (a) Outline the following instruction types of assembly languages

    i) Data transfer instructions

    ii) Data operational instructions

    iii) Program control instructions        [BL: Understand| CO: 1|Marks: 7]

    (b) Model a simple instruction set architecture to minimize the complexity by reducing the number of instructions and addressing modes available to the programmer [BL: Apply| CO: 1|Marks: 7]

## MODULE – II

2. (a) Describe the working principle of three-state bus buffers. How it controls the flow of data on the bus and handles the three different states?        [BL: Understand| CO: 2|Marks: 7]

    (b) Build the 4-bit arithmetic circuit for parallel adder to perform different types of arithmetic operations        [BL: Apply| CO: 2|Marks: 7]

## MODULE – III

3. (a) Explain the different types of memory-reference instructions in performing memory operations and draw the flowchart for memory-reference instructions. How do these instructions facilitate reading and writing data to and from memory?        [BL: Understand| CO: 3|Marks: 7]

    (b) Demonstrate the floating point arithmetic operations and draw the flowchart for addition/ subtraction of two floating-point binary numbers.        [BL: Apply| CO: 3|Marks: 7]

4. (a) Enlist the three major types of interrupts that cause a break in the normal execution of a program in a computer with suitable examples.        [BL: Understand| CO: 4|Marks: 7]

    (b) Design and implement the BCD add/subtraction circuit for performing addition/subtraction on BCD (Binary Coded Decimal) numbers.        [BL: Apply| CO: 4|Marks: 7]

## MODULE – IV

5. (a) Compare the isolated and memory-mapped I/O in computer systems to transfer the information between memory or I/O and the CPU.        [BL: Understand| CO: 5|Marks: 7]

(b) Employ the daisy-chaining priority method for establishing priority between serial connections of all the devices that request an interrupt. [BL: Apply| CO: 5|Marks: 7]

6. (a) Interpret the various modes of data transfer between the central computer and Input/Output devices. [BL: Understand| CO: 5|Marks: 7]

(b) Adapt direct memory access(DMA) controller for DMA transfer among the other components in a computer system. [BL: Apply| CO: 5|Marks: 7]

## MODULE – V

7. (a) Summarize the following auxiliary memory devices used in computer systems
   i) Magnetic disks
   ii) Magnetic tape [BL: Understand| CO: 6|Marks: 7]

(b) Demonstrate the mapping of virtual addresses to physical addresses in a computer system and sketch the memory table for mapping a virtual address. [BL: Apply| CO: 6|Marks: 7]

8. (a) How does associative mapping and set-associative mapping in cache memory allow data to be stored in any cache location without a predetermined mapping?
[BL: Understand| CO: 6|Marks: 7]

(b) Design a four-segment instruction pipeline to improve instruction execution efficiency and specify the each stages of the instruction execution process [BL: Apply| CO: 6|Marks: 7]

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