

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous) Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

DEFINITIONS AND TERMINOLOGY QUESTION BANK

Course Title	DIGITAL SYSTEM DESIGN					
Course Code	AECB07					
Programme	B.Tech	_		-		
Semester	III	ECE				
Course Type	Core					
Regulation	R18	R18				
	Theory			Practical		
Course Structure	Lectures	Tutorials	Credits	Practicals	Credits	
	3	1	4	-	-	
Chief Coordinator	Dr. V Vijay, Associate Professor					
Course Faculty	Dr. P Muna Dr. Lalit K	Dr. P Munaswamy, Professor Dr. Lalit Kumar Kaul, Professor				

OBJECTIVES:

Ι	Understand common forms of number representation in logic circuits.
II	Learn basic techniques for the design of digital circuits and fundamental concepts used in the design of digital systems.
III	Understand the concepts of combinational logic circuits and sequential circuits.
IV	Understand the Realization of Logic Gates Using Diodes & Transistors.

DEFINITIONS AND TERMINOLOGY QUESTION BANK

S.No	QUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code			
	MODULE-I								
1	Define POS form.	Canonical PoS form means Canonical Product of Sums form. In this form, each sum term contains all literals. So, these sum terms are nothing but the Max terms. Hence, canonical PoS form is also called as product of Max terms form.	Understand	CO 1	CLO 3	AECB07.03			
2	What is binary?	Binary (or base-2) a numeric system that only uses two digits — 0 and 1. Computers operate in binary, meaning they store data and perform calculations using only zeros and ones. A single binary digit can only represent True (1) or False (0) in Boolean logic.	Understand	CO 1	CLO 1	AECB07.01			
3	Define number system.	A number system is a collection of various symbols which are called digits. Different types of Number System.	Understand	CO 1	CLO 1	AECB07.01			
4	Define Gray code.	A Gray code is an encoding of numbers so	Understand	CO 1	CLO 1	AECB07.01			

S.No	QUESTION	ANSWER	Blooms Level	СО	CLO	CLO Code
-		that adjacent numbers have a single digit				
		differing by 1. The term Gray code is often				
		used to refer to a "reflected" code, or more				
		specifically still, the binary reflected Gray				
		code.				
5	Define Excess-3	Excess-3, also called XS3, is a non-weighted	Remember	CO 1	CLO 3	AECB07.03
	code.	code. is a self- complementary				
		binary-coded decimal (BCD) code and				
		numeral system. It is a self- complementing				
		code.				
6	What is self	Self-Complementing Codes (Excess 3, 84-2-	Remember	CO 1	CLO 1	AECB07.01
	complementing code?	1, $2*421$) Such codes have the property that				
		the 9's complement of a decimal number is				
		obtained directly by changing 1's to 0's and				
		0's to 1's				
7	Define codes.	In the coding, when numbers or letters are	Understand	CO 1	CLO 1	AECB07.01
		represented by a specific group of symbols, it				
		is said to be that number or letter is being				
		encoded. The group of symbols is called as				
		code. The digital data is represented, stored				
		and transmitted as group of bits. This group				
		of bits is also called as binary code.				
8	Define signed	Signed numbers contain both sign and	Understand	CO 1	CLO 1	AECB07.01
	numbers.	magnitude of the number. Generally, the sign				
		is placed in front of number. So, we have to				
		consider the positive sign for positive				
		numbers and negative sign for negative				
		numbers. Therefore, all numbers can be				
		treated as signed numbers if the				
		corresponding sign is assigned in front of the				
	****	number.		GO 1		
9	What is unsigned	Unsigned numbers contain only magnitude	Understand	COT	CLO I	AECB07.01
	number system?	of the number. They don't have any sign.			-	
	-	I hat means all unsigned binary numbers are			-	
		positive. As in decimal number system, the	_		0	
		placing of positive sign in front of the	1 million (
	~	number is optional for representing positive		- A.		
	0	numbers. Therefore, all positive numbers				
		numbers if positive sign is not assigned in		1		
		front of the number	/ /	1.1		
10	Define sign	The Most significant bit (MSP) is used for	Understand	CO 1	$CI \cap 1$	AECD07.01
10	magnitude form	representing sign of the number and the	Understand	COT	CLU I	ALCD07.01
	magintude form.	remaining hits represent the magnitude of the	1.01.1			
		number. So just include sign bit at the left				
		most side of unsigned binary number. This	100			
		representation is similar to the signed				
		decimal numbers representation				
11	What is hamming	Hamming code is useful for both detection	Remember	CO 1	CLO 1	AECB07.01
	code?	and correction of error present in the received	1.0.110.01	001	0201	1120207101
	code.	data. This code uses multiple parity bits and				
		we have to place these parity bits in the				
		positions of powers of 2. The minimum value				
		of 'k' for which the following relation is				
		correct (valid) is nothing but the required				
		number of parity bits.				
12	What is Duality	This theorem states that the dual of the	Remember	CO 1	CLO 2	AECB07.02
	theorem?	Boolean function is obtained by				
		interchanging the logical AND operator with				
		logical OR operator and zeros with ones. For				

S.No	OUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
	C C C C C C C C C C	every Boolean function, there will be a				
		corresponding Dual function				
13	What is 8/21 code?	The weights of this code are $8, 4, 2$ and 1	Remember	CO 1	CLO 1	AECB07.01
15	what is 0+21 code:	This code has all positive weights. So, it is a	Remember	001	CLO I	ALCD07.01
		positively weighted and This and is also				
		colled on notural RCD (Dinary Coded				
		Called as hatural BCD (Binary Coded				
1.4	XVI 4: 0401 1.0	Decimal) code.	D 1	CO 1		AECD07.01
14	what is 2421 code?	I his code has all positive weights. So, it is a	Remember	01	CLO I	AECB07.01
		positively weighted code. It is an unnatural				
		BCD code. Sum of weights of unnatural				
		BCD codes is equal to 9.1t is a sell-				
		complementing code. Self-complementing				
		codes provide the 9's complement of a				
		decimal number, just by interchanging 1's				
1.5		and 0 s in its equivalent 2421 representation.	XX 1 . 1	GO 1		
15	Define Binary	The binary number system is a numbering	Understand	COT	CLO I	AECB07.01
	Number.	system that represents numeric values using				
		two unique digits (0 and 1). Most computing				
		devices use binary numbering to represent				
		electronic circuit voltage state, (i.e., on/off				
1.5		switch), is the base-2 number system.			OT 0.1	
16	Define Decimal	A number is expressed in base 10 by using	Understand	CO 1	CLO 1	AECB07.01
	number system.	one of the first nine integers or 0 in each				
		place and letting each place value be a power				
		of 10.				
17	Define octal number	The octal numeral system, or oct for short, is	Understand	CO 1	CLO 1	AECB07.01
	system.	the base-8 number system, and uses the digits	-			
		0 to 7. Octal numerals can be made from				
		binary numerals				
18	Define Hexa decimal	The hexadecimal numeral system, also	Understand	CO 1	CLO 1	AECB07.01
	number system.	known as just hex, is a numeral system made				
		up of 16 symbols (base 16). The standard			1.00	
		numeral system is called decimal (base 10)				
		and uses ten symbols: 0,1,2,3,4,5,6,7,8,9.			_	
		Hexadecimal uses the decimal numbers and				
		includes six extra symbols.	1			
19	What is one's	The ones' complement of a binary number is	Remember	CO 1	CLO 1	AECB07.01
	compliment?	defined as the value obtained by inverting all		-		
		the bits in the binary representation of the	1	100		
		number.		1		
20	What is Two's	The 2's complement of a binary number is	Remember	CO 1	CLO 1	AECB07.01
	compliment?	obtained by adding one to the 1's				
		complement of signed binary number. So, 2's	- 0. V			
		complement of positive number gives a	0			
		negative number. Similarly, 2's complement				
		of negative number gives a positive number.	1900 - C			
21	What is binary coded	Binary coded decimal (BCD) is a system of	Understand	CO 1	CLO 1	AECB07.01
	decimal?	writing numerals that assigns a four-digit				
		binary code to each digit 0 through 9 in a				
		decimal (base-10) numeral. The four-bit				
		BCD code for any particular single base-10				
		digit is its representation in binary notation.				
22	Define Unit distance	An un weighted code that changes at only	Understand	CO 1	CLO 1	AECB07.01
	code.	one digit position when going from one				
		number to the next in a consecutive sequence				
		of numbers. Use of one of the many unit-				
		distance codes can minimize errors at symbol				
		transition points when converting analog				
		quantities into digital quantities.				

23 Define parity bit. the fact of Most significant bit (MSB) or on the right of Least significant bit (MSB) or on the ri	S.No	QUESTION	ANSWER	Blooms Level	СО	CLO	CLO Code
24 What is error The right of Less significant bit (MSB) or to inginal bit stream. There are two types of aparity codes, manely even parity code and odd parity code. based on the type of parity being chosen. Remember C0 1 CI 0.1 AFCB07.01 24 What is error To is used to detect the error(s) present in the preserviced dual divistream). These codes detect the error, if it is occurred during transmission of the data (bit stream). These codes detect the error, if it is occurred during transmission of the data (bit stream). These codes detect the error. If it is occurred during transmission of the data (bit stream). These codes detect the error. If it is occurred during transmission of the data (bit stream). These codes detect the error. If it is occurred during transmission of the data (bit stream). These codes detect the error. If it is occurred during transmission of the data (bit stream). These codes detect the error. If it is occurred during transmission of the data (bit stream). These codes detect the error. If it is occurred only two elements 1 and 0 by which all the mathematical operations in binary system. These are not holds by only two elements. C0 1 CL 0.2 AFCB07.02 226 Define sop form. Comparized Styp form means Canonical Sum of the min terms. Hence, error module terms form. Understand C0 1 CL 0.1 AECB07.01 227 What is Boolean Takes only two values - either true (1) or formal togic. Remember C0 1 CL 0.1 AECB07.01 28 What is Boolean	23	Define parity bit.	It is easy to include one parity bit either to	Understand	CO 1	CLO 1	AECB07.01
in the right of Least significant bit (LSB) of ord parity codes, namely even parity code and odd parity code sector the received data (bit stream). These codes contain some bits, which are included to the original bit stream. These codes contain some bits, which are included to the original data (bit stream). These codes contain some bits, which are included to the original data (bit stream). These codes contain some bits, which are included to the original data (bit stream). These codes code, Hamming code. CO 1 CLO 1 AECB07.01 25 Define Booleau algebra. Boolean algebra or switching algebra is system. These are codes protons of the received data (or parity or chements 1 and 0 by which all the mathematical operations in binary system. These are only by other or parity to chements 1 and 0 by which all the mathematical operations are commental soft form means Cannetical Sum terms form. Understand computer retworks CO 1 CLO 3 AECB07.02 26 Define sop form Canonical Song form means Cannetical Sum terms form. Understand computer retworks Understand computer retworks CO 1 CLO 3 AECB07.01 27 What is RORC? Canonical Song form is also called as sum of min terms form. Understand computer retworks Understand computer retworks CO 1 CLO 1 AECB07.01 28 What is Rogela Quintary (base-5 or pental) is a numeral variable? Remember CO 1 CLO 1 AECB07.01			the left of Most significant bit (MSB) or to				
24 What is error Detection? It is used to detect the error(2) present in the precived data (bit stream). These code date to the error if it is occurred during transmission of the original bit stream). These code date to the error, if it is occurred during transmission of the original bit stream). These code date to the error, if it is occurred during transmission of the original bit stream). These code date to the error, if it is occurred during transmission of the original bit stream). These codes detect the error, if it is occurred during transmission of the original data (bit stream). These codes detect the error, if it is occurred during transmission of the original bit stream. These codes detect the error is in stream). These codes detect the error by two demensions in bitary system. These are only two demensions are to be performed. Remember CO 1 CL 0.2 AECB07.02 25 Define Boolean algebra. Boolean algebra or switching algebra is a system. These are only two demensions are to be performed. Understand CO 1 CL 0.3 AECB07.02 26 Define sop form. Canonical Sop form means Canonical Sum trem serontal but the mate-ton designed to detect accidental changes to digital data in computer networks. Understand CO 1 CL 0.1 AECB07.01 27 What is Boolean varable? Take only two values either true (1) or formal loga. Remember CO 1 CL 0.1 AECB07.01 28 What is Boolean varable? Taket only two values either true (1) or formal loga. </td <td></td> <td></td> <td>the right of Least significant bit (LSB) of</td> <td></td> <td></td> <td></td> <td></td>			the right of Least significant bit (LSB) of				
and a diparity codes, namely even parity code and objarity code based on the type of parity heing chosen. CO CO CO 24 What is error It is used to detect the error(s) present in the received data (bit stream). These codes codes detect the error(s) minimated to the original data (bit stream). These codes detect the error(s) minimated to the original data (bit stream). These codes detect the error(s) minimated during transmission of the original data (bit stream). Example – Parity code; Hamming code. Remember CO CO CLO AECB07.01 25 Define Boolean algebra. Boolean algebra or switching algebra is a system of mathematical logic to perform different nuthematical operations in hiary system. These are only two elements 1 and 0 by which all the mathematical operations are not be performed. CO CLO AECB07.02 26 Define sop form. Canonical Sop form seans Canonical Sum or means Canonical Sum or min terms are onding but the min terms. Hence, canonical Sop form is also called as sum or min terms are noting wallser-either true (1) or fake (0). They are used a basic units of fake (0). They are used a basic units of falad tain canonical Sop form all begins or biginal data in canonical Sop form allow so to diginal data in canonical Sum of mail begins. CO CLO AECB07.01 27 What is Boolean devises - or penal) is a numeral subsite or minimal system. If these or penalo is a basic units of falak (0). They are used as basic units of falak (0). They are usetads basic units of falak (0). They are used as basic			original bit stream. There are two types of				
odd pairty code based on the type of pairty being chosen. odd pairty code based on the type of pairty being chosen. output the server of the type of pairty being chosen. output the server of the type of pairty being chosen. output the server of the type of pairty being chosen. CO 1 CL 0 1 AECB07.01 24 What is error original data (bit stream). These codes detect the error, if it is occurred during transmission of the original data (bit stream). Example – Parity code. Remember CO 1 CL 0 2 AECB07.02 25 Define Boolean algebra. Boolean algebra or switching algebra is a system of mathematical operations in binary system. These are only two elements 1 and 0 Understand CO 1 CL 0 2 AECB07.02 26 Define sop form. Cannical Sop form means Canonical Sum of Products form. In this form, each product terms are nothing but the min terms. Hence, canonical Sop form is also called as sum of min. Understand CO 1 CL 0 1 AECB07.01 27 What is Roplean Takes only twov values – either true (1) or fabe(0). They are used as busic units of formal logic. Remember CO 1 CL 0 1 AECB07.01 28 What is Roplean variable? Takes only twov values – either true (1) or fabe(0). They are used as busic units of formal logic. Remember CO 1 CL 0 1 AECB07.01 <td></td> <td></td> <td>parity codes, namely even parity code and</td> <td></td> <td></td> <td></td> <td></td>			parity codes, namely even parity code and				
being chosen. Remember CO CLO AECB07.01 24 What is error It is used to detect the error(s) present in the received data (bit stream). These codes codes codes date (bit stream). These codes detect the error, if it is occurred during transmission of the original data (bit stream). Example – Parity code. Hamming code. Remember CO 1 CLO 2 AECB07.02 25 Define Boolean agebra codes date (bit stream). Example – Parity code. Hamming code. Remember CO 1 CLO 2 AECB07.02 26 Define Boolean agebra codes date (bit stream). Example – Parity code. Hamming code. Remember CO 1 CLO 2 AECB07.02 27 Define sop form. Cannotcal Sop form neams Cannotcal Sum of Podata's form in this form, each product term contains all literals. So, these product term contains all literals. So these product term contains all literals. So these product term contains all literals. So, these product term contains all literals. So, these pro			odd parity code based on the type of parity				
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Detection? received data (bit stream). These codes original data (bit stream). These codes detect the original data (bit stream). Example – Parity Remember CO 1 CL 0.2 AECB07.02 25 Define Boolean algebra. Boolean algebro or switching algebra is a system of mathematical logic to perform different mathematical logic to perform by which all the mathematical stam of Products form. Remember CO 1 CL 0.2 AECB07.02 26 Define Sop form. Canonical Sop form means Canonical Sum of Products form. Understand CO 1 CL 0.3 AECB07.03 26 Define sop form. Canonical Sop form is also called as sum of min Understand CO 1 CL 0.4 AECB07.03 27 What is CRC? a single-burst-error-detecting cyclic code and non-secure hash function designed to detect accidental changes to digital data in compater networks CO 1 CL 0.1 AECB07.01 28 What is Booleum variable? Takes only two values - cither true (1) or formal logic. Remember CO 1 CL 0.1 AECB07.01 29 What is Logic Composed of graphic symbols for logic gates. CO 1 CL 0.1 AECB07.01 20 What is Logic Composed of graphic symbols for logic gates.	24	What is error	It is used to detect the error(s) present in the	Remember	CO 1	CLO 1	AECB07.01
Image: Contain some ones, which are included to the original bit stream. These code detect the error, if it is occurred during transmission of the original data (bit stream). Example – Parity code.RememberCO 1CLO 2AECB07.0225Define Boolean algebra.Boolean algebra or switching algebra is a system of mathematical operations in binary system. These care only two clements 1 and 0 by which all the mathematical operations are to be performed.RememberCO 1CLO 2AECB07.0226Define sop form.Canonical Sop form means Canonical Sum of Products form. In this form, each product terms are nothing but the min terms. Hence, canonical Sop form is also called as sum of mone server hash function designed to detect a compare to be performed.UnderstandCO 1CLO 1AECB07.0127What is CRC?a single-burst-error-detecting cyclic code and non-secure hash function designed to detect accidential changes to digital data in computer networksUnderstandCO 1CLO 1AECB07.0128What is Boolean values - either true (1) or false (0). They are used as basic units of formal logic.RememberCO 1CLO 1AECB07.0130What is Logic culture networksContinger and the inhibrary. Sinary 10UnderstandCO 1CLO 1AECB07.0131What does 10 mean filter as 10.10 in binary. binary 10UnderstandCO 1CLO 2AECB07.0231What is base 4Quater any is the base-4 numeral system. 1RememberCO 1CLO 2AECB07.0233What is SoP and POSThe econy is also to represent any disple to represent any disple to represent any disple tor resting of the cano		Detection?	received data (bit stream). These codes				
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1 unit unit <t< td=""><td></td><td></td><td>the</td><td></td><td></td><td></td><td></td></t<>			the				
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25 Define Boolean algebra. Boolean algebra or switching algebra is a system of mathematical logic to perform different mathematical operations in binary system. These are only two elements 1 and 0 by which all the mathematical operations are to be performed. CO 1 CLO 2 ABCB07.02 26 Define sop form. Canonical Sop form means Canonical Sum of Products form. In this form, each product terms are nothing but the min terms. Hence, canonical Sop form is also called as sum of min_ terms form. Understand CO 1 CLO 3 AECB07.03 27 What is CRC? a single-burst-error-detecting cyclic code and non-secure hash function designed to detect arcidental changes to digital data in computer networks Understand CO 1 CLO 1 AECB07.01 28 What is Boolean variable? Takes only two values – either true (1) or false (0). They are used as basic units of formal logic. Remember gates. CO 1 CLO 1 AECB07.01 29 What is Logic diagram? Quinary (base-5 or pental) is a numeral gates. Understand CO 1 CLO 1 AECB07.01 30 What is base 4 Quinary (base-5 or pental) is a numeral wises the digits 0, 1, 2 and 3 to represent any the base of the number system. Understand CO 1 CLO 2 AECB07.02 31 What is SoP and POS and Maxterms? A minterm is a Bololean expression resulting in 1 for the outpu			code. Hamming code.				
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map: squares each representing a different combination of the variables of a Boolean function. Imap: Imap: 37 What are the Minimizes boolean expressions without the Remember CO 1 CLO 3 AECB07.03	30	what is Karnaugh	a unagram consisting of a rectangular array of	Keinember	01	CLU 3	AECB07.03
37 What are the Minimizes boolean expressions without the Remember CO 1 CLO 3 AECB07.03		map :	squares each representing a different combination of the variables of a Roolean				
37 What are the Minimizes boolean expressions without the Remember CO 1 CLO 3 AECB07.03			function.				
	37	What are the	Minimizes boolean expressions without the	Remember	CO 1	CLO 3	AECB07.03

S.No	OUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
0110	advantages of K	need using various boolean theorems &	Dioonis Level	00	020	020 0000
	Man?	computations Minimizes number of Logical				
	Mup.	gates used				
38	Why is Gray code	Gray code sequence only changes one binary	Understand	CO 1	CLO 3	AECB07.03
50	used in K man?	bit as we go from one number to the next in	Onderstand	001	CLO J	ALCD07.05
	used in K map:	the sequence, unlike binery. That means that				
		discont calls will only your by one bit on				
		Declean veriable. This is what we need to				
		boolean variable. This is what we need to				
		that we may view commonality				
20	Without the design of	that we may view commonanty.	TT. I. action 1	CO 1	CLO 2	AECD07.02
39	what is dont care	a dont-care term for a function is an input-	Understand	01	CLO 3	AECB07.03
	condition?	sequence (a series of bits) for which the				
10	XX 71 1	function output does not matter	D 1	00.1	CT O O	
40	Why do we use gray	used to facilitate error correction in digital	Remember	COT	CLO 3	AECB07.03
	code?	communications such as digital terrestrial				
		television and some cable TV systems.				
		MODULE-II				
1	What is parallel	A parallel adder is an arithmetic	Understand	CO 2	CLO 4	AECB07.04
	adder?	combinational logic circuit that is used to add				
		more than one bit of data simultaneously.				
2	Define 5-variable k-	The number of cells in 5 variable K-map is	Remember	CO 2	CLO 4	AECB07.04
	map.	thirty-two, since the number of variables is 5.				
		The following figure shows 5 variable K-				
		Map, here is only one possibility of grouping				
		32 adjacent min terms. There are two				
		possibilities of grouping 16 adjacent min	1000			
		terms, i.e., grouping of min terms from m0 to				
		m15 and m16 to m31.				
3	Define 4-variable k-	The number of cells in 4 variables K-map is	Remember	CO 2	CLO ₄	AECB07.04
U	man	sixteen since the number of variables is four	110111011	001	020.	1120207101
	imp.	There is only one possibility of grouping 16			-	
		adjacent min terms			-	
4	Define 3-variable k-	The number of cells in 3 variable K-man is	Remember	CO 2	CLO ₄	AECB07.04
•	man	eight since the number of variables is three	Remember	002	CLO I	THEEDOT.OT
	iimp.	The following figure shows 3 variable K-				
		Map There is only one possibility of				
		grouping 8 adjacent min terms				
5	Define Hazards	A dynamic hazard is the possibility of an	Understand	CO_2	CLO 4	AECB07.04
5	Define Hazards.	output changing more than once as a result of	Onderstand	002	CLO 4	ALCD07.04
		a single input change				
6	What is static hazard?	static hazard takes place when change in an	Understand	CO 2	CLOA	AECB07.04
0	mat is static flazalu?	input causes the output to change	onderstallu	002		ALCD07.04
		momentarily before stabilizing to its correct				
7	What is dynamic	A dynamic bazard is the possibility of an	Understand	CO 2	CIO4	AECB07.04
/	hazard?	A dynamic hazard is the possibility of an	Understand	02	CLO 4	ALCD07.04
	nazaru :	as a result of a single input change. Dynamic				
		hazards often occur in larger logic circuits				
		where there are different routes to the output				
		(from the input)				
0	What is calact line?	A multiplayor (or muy) is a device that	Understand	CO^{2}		
0	w hat is select line?	A multiplexer (of mux) is a device that	Understand	02	CLU4	AECD07.04
		selects one of several analog of digital input				
		signals and forwards the selected input into a single line. A multipleyer of 2 minputs has a				
		single line. A multiplexer of 2 n inputs has n				
		select lines, which are used to select which				
0	Define data silente	Input line to send to the output.	I Indonetica 4	CO 2		AECD07.04
9	Define data selector.	Data Selector take one data input and a	Understand	002	CLU 4	AECB07.04
		number of selection inputs, and they have				
1		several outputs. They forward the data input				

S.No	QUESTION	ANSWER	Blooms Level	СО	CLO	CLO Code
		to one of the outputs depending on the values				
		of the selection inputs.				
10	Define decoder.	A decoder is a circuit that changes a code	Understand	CO 2	CLO 4	AECB07.04
		into a set of signals. It is called a decoder				
		because it does the reverse of encoding, but				
		we will begin our study of encoders and				
		decoders with decoders because they are				
		simpler to design.				
11	Define an encoder.	The n output lines generate the binary code	Understand	CO 2	CLO 4	AECB07.04
		for the possible 2n input lines. Let us take an				
		example of an octal-to-binary encoder.				
12	Define priority	Binary Encoders generally have a number of	Understand	CO 2	CLO ₄	AECB07 04
	encoder.	inputs that must be mutually exclusive, i.e.	Chathatana	001	020.	1120201101
		only one of the inputs can be active at any		1 A		
		one time. The encoder then produces a binary				
		code on the output pins, which changes in				
		response to the input that has been activated				
13	What is Enable?	Enable pin in multiplexers de multiplexer	Understand	CO_2	CLO 4	AECB07.04
15	What is Enable.	decoder and encoder ensures the functioning	Onderstand	002	CLO I	Theorem
		of the hardware i.e. "enables" the function of				
		the logic circuit				
14	Define k man	Karnaugh introduced a method for	Understand	CO_2	CIO4	AECB07.04
14	Define K-map.	simplification of Boolean functions in an	Understand	02	CLO 4	ALCD07.04
		simplification of Boolean functions in an				
		Karnaugh man mathod or K man mathod. It				
		Kamaugh map method of K-map method. It				
		is a graphical method, which consists of 2 ¹¹				
		cells for 'n' variables. The adjacent cells are				
		differed only in single bit position.				
15	Define Prime	Each grouping will give either a literal or one	Remember	CO 2	CLO 4	AECB07.04
	implicant and	product term. It is known as prime implicant.				
	Essential prime	The prime implicant is said to be essential				
	implicant.	prime implicant, if at least single '1' is not			-	
	C	covered with any other groupings but only			-	
	1	that grouping covers.				
16	What is don't care	If outputs are not defined for some	Understand	CO 2	CLO 4	AECB07.04
	condition?	combination of inputs, then those output	Statement of the			
		values will be represented with don't care		A		
	C	symbol 'x'. That means, we can consider				
		them as either '0' or '1'.		1		
17	Define tabular	Quine-McClukey tabular method is a tabular	Understand	CO 2	CLO 5	AECB07.05
	method.	method based on the concept of prime	2.2	C		
		implicants. We know that prime implicant is	- N.			
		a product (or sum) term, which can't be	. 0. *			
		further reduced by combining with any other				
		product (or sum) terms of the given Boolean	100 C			
		function.				
18	What is universal	NAND & NOR gates are called as universal	Understand	CO 2	CLO 5	AECB07.05
	gate?	gates. Because we can implement any				
		Boolean function, which is in sum of				
		products form by using NAND gates alone.				
		Similarly, we can implement any Boolean				
		function, which is in product of sums form				
		by using NOR gates alone.				
19	Define logic gates?	The basic digital electronic circuit that has	Understand	CO 2	CLO 5	AECB07.05
		one or more inputs and single output is				
		known as Logic gate. Hence, the Logic gates				
		are the building blocks of any digital system.				
		We can classify these Logic gates into the				
		following three categories.				

S.No	QUESTION	ANSWER	Blooms Level	СО	CLO	CLO Code
20	Define combinational	Combinational circuits consist of Logic	Understand	CO 2	CLO 5	AECB07.05
	circuit.	gates. These circuits operate with binary				
		values. The output(s) of combinational				
		circuit depends on the combination of present				
		inputs.				
21	Define half adder.	Half adder is a combinational circuit, which	Understand	CO 2	CL0 5	AECB07.05
		performs the addition of two binary numbers				
		A and B are of single bit. It produces two				
		outputs sum, S & carry, C.				
22	What is binary adder?	The most basic arithmetic operation is	Understand	CO 2	CLO 5	AECB07.05
		addition. The circuit, which performs the				
		addition of two binary numbers, is known as				
		Binary adder.				
23	Define full adder.	Full adder is a combinational circuit, which	Understand	CO 2	CLO 5	AECB07.05
		performs the addition of three				
		bits A, B and Cin. Where, A & B are the two				
		parallel significant bits and Cin is the carry				
		bit, which is generated from previous stage.				
24	Define multiplexer.	Multiplexer is a combinational circuit that	Understand	CO 2	CLO 5	AECB07.05
		has maximum of 2^n data inputs 'n' selection				
		lines and single output line. One of these data				
		inputs will be connected to the output based				
		on the values of selection lines				
25	Define Demultiplexer	De-Multiplexer is a combinational circuit	Understand	CO_2	CLO 5	AECB07.05
23	Denne Dennartipiexer	that performs the reverse operation of	Onderstand	602	CLO J	Theorem 1
		Multiplexer It has single input 'n' selection				
		lines and maximum of 2 outputs. The input				
		will be connected to one of these outputs				
26	Define comperator	Digital Comparator A magnitude digital	Understand	CO 2	CLO 5	AECD07.05
20	Denne comparator.	comparator is a combinational circuit that	Understand	02	CLO 5	AECD07.05
		compares two digital or binary numbers			-	
	C	(consider A and B) and determines their			-	
	-	relative magnitudes in order to find out			-	
		whether one number is equal less than or			0	
		greater than the other digital number				
27	What is code	Codes and code converters Coding is the	Remember	CO 2	CLO 5	AECB07.05
	converter?	process of translating the input information	Remember	002	0105	Theorem
		which can be understandable by the machine				
		or a particular device. Coding can be used for	×			
		security purpose to protect the information	1.1			
		from steeling or interrupting.	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~			
28	What is parallel	A parallel adder is an arithmetic	Understand	CO 2	CLO 5	AECB07.05
	adder?	combinational logic circuit that is used to add	1.			
		more than one bit of data simultaneously.	lane -			
29	What is one-to-one	each input code word produces a different	Understand	CO 2	CLO 5	AECB07.05
	mapping?	output code word				
30	What is binary	has an n-bit binary input code and a 1-out-of-	Understand	CO 2	CLO 5	AECB07.05
	decoder?	2n output code				
31	What is binary	If the device's output code has fewer bits	Remember	CO ₂	CLO 6	AECB07.06
	encoder?	than the input code, the device is usually				
		called an encoder				
32	What is multiplexer?	a digital switch—it connects data from one	Understand	CO 2	CLO 6	AECB07.06
		of n sources to its output				
33	What is comparator?	A circuit that compares two binary words	Understand	CO2	CLO 6	AECB07.06
		and indicates whether they are equal is called				
		a comparator				

S.No	QUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
34	What is ALU?	arithmetic logic unit (ALU) is a digital	Understand	CO 2	CLO 6	AECB07.06
		circuit used to perform arithmetic and logic				
		operations				
35	What is Barrel	A barrel shifter is a digital circuit that can	Remember	CO 2	CLO 6	AECB07.06
	shifter?	shift a data word by a specified number of				
		bits without the use of any sequential logic,				
		only pure combinational logic				
36	What is meant by	BCD adder A 4-bit binary adder that is	Understand	CO 2	CLO 6	AECB07.06
	BCD adder?	capable of adding two 4-bit words having a				
		BCD (binary-coded decimal) format				
37	Where is BCD used?	Binary-coded Decimal or BCD is a way of	Understand	CO 2	CLO 6	AECB07.06
		representing a decimal number as a string of				
		bits suitable for use in electronic systems.		a a	CT 0 1	
38	What is a 4 bit	a combinational circuit which is used to add	Remember	CO 2	CLO 6	AECB07.06
- 20	parallel adder?	two N-bit binary numbers	XX 1 . 1	00.0	CT O (
39	What is a in binary	A binary code represents text, computer	Understand	CO 2	CLO 6	AECB07.06
	code?	processor instructions, or any other data				
40	W/1	using a two-symbol system.	The desired of the	CO 2	CLO (AECD07.06
40	what is fast adder?	A carry-lookanead adder (CLA) of fast adder	Understand	02	CLU 6	AECB07.06
1	What is a counter?	Counts those pulses which are driven by a	Remember	CO 3		AECB07.7
1	what is a counter?	clock	Kemember	05	CLO /	ALCD07.7
2	What are the	(i) Asynchronous and Synchronous counters	Understand	<u>CO</u> 3	CLO7	AFCB077
2	categories Counters?	(i) Single and multi mode counters (iii)	Onderstand	05	CLO /	ALCD07.7
	eurogonies counters.	Modulus counters.				
3	What is a multimode	If the same counter circuit can be operated in	Remember	CO 3	CLO 7	AECB07.7
C	counter?	both the UP and DOWN modes, it is called a		000	020 /	111020111
		multimode counters.				
4	What is a	Each flip flop is triggered by the previous	Understand	CO 3	CLO 7	AECB07.7
	asynchronous	flip flop.				
	counters?				-	
5	What is a Ripple	A ripple counter is an asynchronous counter	Remember	CO 3	CLO 7	AECB07.7
	Counter?	where only the first flip-flop is clocked by an			-	
		external clock				
6	Where the ripple	It can also be used for Frequency divider,	Understand	CO 3	CLO 7	AECB07.7
	counter is used	time measurement, frequency measurement,		A		
	explain?	distance measurement and also for				
		generating square waveforms.		100		
7	What is the difference	In a synchronous counter however, the	Remember	CO 3	CLO 7	AECB07.7
	between ripple	external event is used to produce a pulse that	2.5	0		
	counter and	is synchronised with the internal clock.	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~			
0	What is the main	Disaduantagos of Asymphetics Country	Undonstand	CO^{2}	CLO 7	AECD077
ð	disadvantage of	An extra "re-synchronizing" output flip flop	Understand	003	CLU /	AECDU/./
	asynchronous	may be required	la contra c			
	counters?	may be required.				
9	What is a Johnson	A Johnson counter is a modified ring	Remember	CO 3	CLO 7	AECB07.7
	counter?	counter, where the inverted output from the				
		last flip flop is connected to the input to the				
		first. The register cycles through a sequence				
		of bit-patterns.				
10	What is a ring	A ring counter is a type of counter composed	Understand	CO 3	CLO 8	AECB07.8
	counter?	of flip-flops connected into a shift register,				
		with the output of the last flip-flop fed to the				
		input of the first, making a "circular" or				
		"ring" structure.				
11	What is the purpose	When a bit is input on the right, all the bits	Remember	CO 3	CLO 8	AECB07.8
1	of a shift register?	move one place to the left, and the leftmost				

S.No	QUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
		bit disappears. Shift registers are commonly				
		used in converters that translate parallel data				
		to serial data, or vice-versa. Shift registers				
		can also function as delay circuits and digital				
		pulse extenders.				
12	What are universal	A Universal shift register is a register which	Understand	CO 3	CLO 8	AECB07.8
	shift registers?	has both the right shift and left				
		shift with parallel load capabilities. Universal				
		shift registers are used as memory elements				
		in computers.				
13	What is the difference	Both shift registers and counters are made of	Remember	CO 3	CLO 8	AECB07.8
	between register and	flip-flops. A shift register is simply a chain				
	shift register?	of FFs where the O output of one FF				
	Sinte register (connects to the D input of the next A shift				
		register will transfer data from one FF to the				
		next on each clock event				
14	What is bidirectional	A bidirectional shift register is one in which	Understand	CO 3	CLO 8	AECB07.8
11	shift register?	the data can beshifted either left or right. It	Chacistana	005	010 0	Theorem
	shirt register.	can be implemented by using gatelogic that				
		enables the				
		transfer of a data bit from one stage to				
		thenext stage to the right or to the left				
		depending on the level of acontrol line				
15	What is a dynamic	A dynamic shift register circuit comprises an	Remember	CO 3	CLOS	AECB07.8
15	shift register?	input terminal and an output terminal. The	Kememoer	05	CLU 0	ALCD07.8
	shift register?	logic circuit is made operative by an output				
		signal of the signal follower circuit and				
		produces an inverter function at the output				
		terminal in response to an output signal of				
		the second transfer gate circuit				
16	Define Sequential	Sequential circuit has memory so output can	Understand	CO 3	CLOQ	AECB07.9
10	circuits	very based on input. This type of circuits	Understand	05	CLO 9	ALCD07.9
	circuits.	uses previous input, output, clock and a			-	
	C	memory element			100 C	
17	Define flip flop	A flip flop is a circuit that has two stable	Remember	CO 3	CLOQ	AECB07.0
17	Define hip-hop.	states and can be used to store state	Remember	005	CLO)	ALCD07.7
	6	information. The circuit can be made to	and the second s		100 C	
		change state by signals applied to one or				
	C	more control inputs and will have one or two				
		outputs. It is the basic storage element in				
		sequential logic flip flop has a clock signal	×			
18	Define latch.	The output of the latch depends on its input	Understand	CO 3	CLO 9	AECB07 9
10	Denne laten.	It continuously checks its inputs and changes	Chaeistana	005	010)	ПШевоно
		its output correspondingly. It is not	1.50			
		depending on clock	1.			
19	What is ik flip-flop?	The IK Flip Flop is basically a gated RS flip	Remember	CO 3	CLO 9	AECB07 9
17	what is jk inp nop.	flop with the addition of the clock input	Remember	005	CLO)	THEEDOT.
		circuitry When both the inputs S and R are				
		equal to logic "1" the invalid condition takes				
		place. Thus to prevent this invalid condition				
		a clock circuit is introduced				
20	What is master slave	Master slave IK FF is a cascade of two S-R	Remember	CO 3	CLO9	AECB07.9
20	ik flin- flon?	FF with feedback from the output of second	Kennennoer	005		
	Jr mh- mh;	to input of first Master is a positive level				
		triggered But due to the presence of the				
		inverter in the clock line, the slave will				
		respond to the negative level Master clave				
		flip flop is designed using two soperate flip				
		flops				
		nops.				

S.No	QUESTION	ANSWER	Blooms Level	СО	CLO	CLO Code
21	Define T flip-flop.	The T or "toggle" flip-flop changes its output	Understand	CO 3	CLO 9	AECB07.9
		on each clock edge, giving an output which				
		is half the frequency of the signal to the T				
- 22	W7 . 1 10	input	TT 1 . 1	<u> </u>	CT 0 10	A E C D 07 10
22	What is clock?	A clock signal is a particular type of signal	Understand	CO 3	CLO 10	AECB07.10
22	What is manager as 119	that oscillates between a high and a low state	Understand	CO 2	CLO 10	AECD07.10
23	what is memory cen?	stores one bit of binary information and it	Understand	05	CLO 10	AECD07.10
		must be set to store a logic 1 (high voltage				
		level) and reset to store a logic 0 (low				
		voltage level). Its value is maintained/stored				
		until it is changed by the set/reset process.				
24	What is Binary cell?	An elementary unit of computer storage that	Understand	CO 3	CLO 10	AECB07.10
		can have one or the other of two stable states	6			
		and can thus store one bit of information.				
25	Define clock skew.	Clock skew is a phenomenon in synchronous	Understand	CO 3	CLO 10	AECB07.10
		digital circuit systems in which the same				
		sourced clock signal arrives at different				
		instantaneous difference between the				
		readings of any two clocks is called their				
		skew.				
26	What is sequential	It has inputs and outputs that can each take	Understand	CO 3	CLO 10	AECB07.10
	machine?	on any value from a finite set and are of				
		interest only at certain instants of time, and				
		in which the output depends on previous				
		inputs as well as the concurrent input.				
27	What is register?	A collection of two or more D flip-flops with	Remember	CO 3	CLO 11	AECB07.11
20	XX 71	a common clock input is called a register		GO 3	CT 0 11	AEGD07.11
28	What is divide-by-m	A counter with m states is called a modulo-m	Understand	CO 3	CLO II	AECB07.11
20	What is Shift	Counter or, sometimes, a divide-by-m counter	Domomhor	CO 3	CLO 11	AECD07.11
29	What is Simi- Register?	a sint register is an n-bit register with a	Kemember	05		AECD07.11
	Register :	bit position at each tick of the clock			100 C	
30	What is ROM?	ROM is a type of memory that normally can	Remember	CO 3	CLO 11	AECB07.11
	1	only be read, as opposed to RAM which can	· · · · ·		~	
	- C-	be both read and written			100	
31	What is PROM?	This is a type of ROM that can be	Understand	CO 3	CLO 11	AECB07.11
		programmed using special equipment; it can		100		
		be written to, but only once.			ax a 40	
32	What is EPROM?	An EPROM is a ROM that can be erased and	Remember	CO 3	CLO 10	AECB07.10
22	What is EEDDOM9	Flootricelly Freechle Dreemerschle DOM	Understand	CO 2	CLO 10	AECD07 10
27 27	What is DRAM?	Dynamic random access memory	Remember	CO 3	CLO 10	AECD07.10
34	What is Synchronous	An asynchronous DRAM chin has nower	Understand	<u>CO3</u>	CLOID	AECB07.10
55	DRAM?	connections, some number of address inputs	Understallu	05		ALCD0/.7
		(typically 12), and a few (typically one or				
		four) bidirectional data lines.				
36	What is Synchronous	An asynchronous DRAM chip has power	Understand	CO 3	CLO 9	AECB07.9
	DRAM?	connections, some number of address inputs				
		(typically 12), and a few (typically one or				
		four) bidirectional data lines.				
37	What is called latch?	A latch is an electronic logic circuit that has	Remember	CO 3	CLO 9	AECB07.9
		two inputs and one output. One of the inputs				
		RESET input. I atch circuits can be either				
		active-high or active-low				
38	What are the different	there are four types of latches and flin flons:	Remember	CO 3	CLO 8	AECB07 8
	types of latches?	SR, D, JK and T.				

S.No	OUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
39	What is master slave	This circuit is a master-slave D flip-flop. A D	Understand	CO 3	CLO 7	AECB07.7
	FF?	flip flop takes only a single input, the D				
		(data) input. The master-slave configuration				
		has the advantage of being edge-triggered,				
		making it easier to use in larger circuits,				
		since the inputs to a flip-flop often depend on				
		the state of its output.				
40	What is toggling in	In the case of JK flip flop (master slave)	Remember	CO 3	CLO 10	AECB07.10
	JK flip flop?	when your input is $J=K=1$, then flip flop is to				
	1 1	be called in toggle state				
		MODULE-IV				
1	What is Transition	The amount of time that the output of a logic	Remember	CO 4	CLO 12	AECB07.12
	Time?	circuit takes to change from one state to				
		another is called the Transition Time.	_			
2	What is Rise time?	Time interval when waveform is changing	Remember	CO 4	CLO 12	AECB07.12
		from a logic low to a logic high level.				
3	What is Fall time?	Time interval when waveform is changing	Understand	CO 4	CLO 12	AECB07.12
		from a logic high to a logic low level.				
4	What are Rise time	ON transistor resistance and Load	Remember	CO 4	CLO 12	AECB07.12
	and Transition Time	capacitance				
	depending					
	parameters?					
5	How Stray	Output circuits' transistors internal wiring	Remember	CO 4	CLO 12	AECB07.12
	Capacitance occurs?	and packing have capacitance in the range.				
6	What is Propagation	The amount of time that it takes for a change	Remember	CO 4	CLO 12	AECB07.12
	Delay?	at the input of a device to produce a change				
		at the output of the same	-			
7	What is t _{pLH} ?	propagation delay when the output changes	Understand	CO 4	CLO 12	AECB07.12
		from LOW to HIGH				
8	What is t _{pHL} ?	Propagation delay when the output changes	Remember	CO 4	CLO 12	AECB07.12
		from HIGH to LOW				
9	What is Dynamic	Power consumed during transition is called	Remember	CO 4	CLO 12	AECB07.12
	Power Dissipation?	Dynamic Power Dissipation			1.00	
10	What is P _T ?	Circuit internal power	Remember	CO 4	CLO 12	AECB07.12
11	What is C_{PD} ?	power dissipation capacitance	Understand	CO 4	CLO 12	AECB07.12
12	What is C _L ?	capacitive load on the output	Remember	CO 4	CLO 12	AECB07.12
13	What is Load power?	Load power (PL) during charging and	Remember	CO 4	CLO 12	AECB07.12
		discharging current flows through transition.				
14	What are basic	The basic building blocks in CMOS logic	Remember	CO 4	CLO 12	AECB07.12
	building blocks in	circuits are MOS transistors NMOS and	1 1			
	CMOS logic circuits?	PMOS	1	C		
15	What is Leakage	The resistance between the gate and the other	Understand	CO 4	CLO 12	AECB07.12
	current?	terminals of the device is extremely high,	1.50			
		well over a mega ohm. The small amount of	1			
		current that flows across this resistance is	100			
		very small, typically less than one				
1.0		microampere, and is called a leakage current.		<u> </u>	01.0.12	
16	what is AOI gate?	AND UK INVERT gate	Kemember	<u>CO 4</u>	CLO 13	AECB07.13
17	what is OAI gate?	UK AND INVERT gate	Understand	<u>CO 4</u>	CLO 13	AECB07.13
18	what are	Logic Levels, Noise Margin, Fan out, Speed,	Kemember	CO 4	CLO 13	AECB07.13
	Characteristics of	Power Consumption, Effect of Loading,				
	Electrical Behavior of	Unused Inputs, Electrostatic Discharge, Open				
10	CMUS?	Drain Outputs, Three State Outputs.	TT. J (1	<u> </u>	OL 0. 12	AECDOZ 12
19	what is V _{OHmin} ?	I ne minimum Output voltage produced in	Understand	CO 4	CLO 13	AECB07.13
- 20	What is V 9	the High sate	Demonstra	<u> </u>	$CI \cap 12$	AECD07.12
20	what is V_{IHmin} ?	i ne minimum input Voltage guaranteed to	Kemember	CO 4	CLU 13	AECB07.13
21	What is V 9	The merimum Input Valtage account of the	Undonstand	CO 4	CL 0 12	AECD07.12
21	what is V _{ILmax} ?	he maximum input voltage guaranteed to	Understand	CU 4	CLU 13	AECB0/.13
		be recognized as a Low				

S.No	QUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
22	What is V _{OLmax} ?	The maximum Output voltage produced in the High sate	Remember	CO 4	CLO 13	AECB07.13
23	What is Fan-out?	The no. of inputs that the gate can drive without exceeding its worst – case loading specifications	Remember	CO 4	CLO 13	AECB07.13
24	What is TTL?	Transistor-Transistor Logic	Understand	CO 4	CLO 13	AECB07.13
25	What is ECL?	emitter-coupled logic	Remember	CO 4	CLO 13	AECB07.13
26	What are n-channel MOS (NMOS) transistor terminals?	gate, source, and drain	Understand	CO 4	CLO 13	AECB07.13
27	What is gate to source voltage (Vgs) in an NMOS transistor?	is normally zero or positive	Remember	CO 4	CLO 13	AECB07.13
28	How to form CMOS logic?	NMOS and PMOS transistors are used together in a complementary way to form CMOS logic	Remember	CO 4	CLO 13	AECB07.13
29	What is fan-in?	The number of inputs that a gate can have in a particular logic family is called the logic family's fan-in	Remember	CO 4	CLO 13	AECB07.13
30	What is DC Noise Margin?	It is a measure of how much noise it takes to corrupt a worst-case output voltage into a value that may not be recognized properly by an input	Understand	CO 4	CLO 13	AECB07.13
31	What is ESD?	ESD is the sudden and momentary unwanted electric currents that flows between two objects and that may cause damage to electronic equipment	Understand	CO 4	CLO 14	AECB07.14
32	What is Bipolar logic?	Bipolar logic families use semiconductor diodes and bipolar junction transistors as the basic building blocks of logic circuits	Understand	CO 4	CLO 14	AECB07.14
33	What is Diode?	A semiconductor diode is fabricated from two types of semiconductor material, called p-type and n-type that are brought into contact with each other	Remember	CO 4	CLO 14	AECB07.14
34	What is Bipolar Junction Transistors?	A bipolar junction transistor is a three- terminal device (Base, Emitter and Collector) that, in most logic circuits, acts like a current-controlled switch	Remember	CO 4	CLO 14	AECB07.14
35	What is CML?	current-mode logic	Understand	CO 4	CLO 14	AECB07.14
36	What is on resistance of MOSFET?	the total resistance between the drain and source in a Metal Oxide Field Effect Transistor	Understand	CO 4	CLO 14	AECB07.14
37	What is Schottky- clamped transistors?	By placing a Schottky diode between the base and collector of each transistor that might saturate. The resulting transistors, which do not saturate, are called Schottky- clamped transistors.	Remember	CO 4	CLO 14	AECB07.14
38	What is noise margin in MOSFET?	the amount of noise that a CMOS circuit could withstand without compromising the operation of circuit.	Remember	CO 4	CLO 14	AECB07.14
39	What is Programmable logic device?	an electronic component used to build reconfigurable digital circuits	Understand	CO 4	CLO 14	AECB07.14
40	What is programmable logic array (PLA)?	a kind of programmable logic device used to implement combinational logic circuits	Understand	CO 4	CLO 14	AECB07.14
	MODULE-V					
1	What is acronym of VHDL?	Very High Speed Integrated Circuits Hardware Description Language	Remember	CO 5	CLO 15	AECB07.15

S.No	QUESTION	ANSWER	Blooms Level	СО	CLO	CLO Code
2	What are VHDL	Designs may be decomposed hierarchically.	Understand	CO 5	CLO 15	AECB07.15
	features?	The logical operation and timing behavior of				
		a design can be simulated.				
3	What is design flow	VHDL-based design process	Remember	CO 5	CLO 15	AECB07.15
	in VHDL?					
4	What is Compiler?	A VHDL compiler analyzes your code for	Understand	CO 5	CLO 15	AECB07.15
		syntax errors and also checks your code for				
		compatibility with other modules on which it				
		relies				
5	What is Simulator?	VHDL simulator allows you to define and	Remember	CO 5	CLO 15	AECB07.15
		apply inputs to your design, and to observe				
		its outputs, without ever having to build the				
		physical circuit		2 0.5	ax a 4 a	
6	What are types of	Functional Verification and Timing	Remember	CO 5	CLO 15	AECB07.15
	verification?	Verification		<i></i>	GY 0 1 7	
7	What are steps in	Synthesis, Fitting/Place + Route, Timing	Understand	CO 5	CLO 15	AECB07.15
	back-end?	Verification	D 1	<u> </u>	CI O 15	AECD07.15
8	What is Synthesis?	converting the VHDL description into a set	Remember	05	CLO 15	AECB07.15
		of primitives or components that can be				
0	What is Place and	assembled in the target technology	Domomhor	<u>CO 5</u>	$CI \cap 15$	AECD07.15
9	Pouto?	assigning equations to available AND-OK	Remember	05	CLO 15	AECD07.15
10	What is final stan in	timing verification	Understand	<u>CO 5</u>	CLO 15	AECB07.15
10	fitted circuit?	timing vermeation	Onderstand	05	CLO 15	ALCD07.15
11	What is entity?	declaration of a module's inputs and outputs	Remember	<u>CO 5</u>	CLO 16	AFCB07.16
12	What is architecture?	detailed description of the module's internal	Understand	CO 5	CLO 16	AFCB07.16
12	what is dreinteeture.	structure or behavior	Onderstand	05	CLO IO	ALCD07.10
13	What is entity	to define its external interface signals or	Understand	CO 5	CLO 16	AECB07 16
10	declaration?	ports in its port declaration part	Chacistana	005	010 10	THEODOWING
14	How comments	with two hyphens ()	Remember	CO 5	CLO 16	AECB07.16
	begins in VHDL?	JI TO C				
15	What is entity	to define its external interface signals or	Understand	CO 5	CLO 16	AECB07.16
	declaration?	ports in its port declaration part				
16	What is entity-name?	A user-selected identifier to name the entity	Remember	CO 5	CLO 16	AECB07.16
17	What are signal-	A comma-separated list of one or more user-	Understand	CO 5	CLO 16	AECB07.16
	names?	selected identifiers to name external-interface				
	2	signals				
18	What is "IN" in	The signal is an input to the entity	Remember	CO 5	CLO 16	AECB07.16
	VHDL?			100		
19	What is "OUT" in	The signal is an output of the entity	Remember	CO 5	CLO 16	AECB07.16
	VHDL?		1	C		
20	What is "BUFFER"	The signal is an output of the entity, and its	Understand	CO 5	CLO 16	AECB07.16
	in VHDL?	value can also be read inside the entity's	101			
01		architecture		00.5	01.0.15	AEGD07.17
21	What is "INOUT" in	The signal can be used as an input or an	Understand	CO 5	CLO 17	AECB07.17
	VHDL?	output of the entity	TT. J · ·	<u> </u>	CL 0.17	AECDOR 17
22	what is "signal-type"	A built-in or user-defined signal type	Understand	005	CLO I7	AECB07.17
22	IN VHDL?	and have the sector 0 or 1.1	The density of 1	CO 5	$CI \cap 17$	AECD07.17
23	What is bit in	can have the value 0 and 1	Understand	05	CL0 17	AECB07.17
24	What is "bit waster"	is a vactor of hit values	Understand	CO 5	$CI \cap 17$	AECD07 17
24	in VHDL stores?	is a vector of oil values	Understand	005		AECDU/.1/
25	What is "hoolean" in	can have the value TRUE and EALSE	Understand	CO 5	CL 0 17	AECB07.17
23	VHDI stores?		Understand	05		ALCD0/.1/
26	What is "time" in	to indicate time	Remember	CO 5	CL O 17	AFCR07 17
20	VHDL?		Remember	005		/1LCD0/.1/
27	What are VHDL	Bit, character, severity level bit vector	Remember	CO 5	CLO 17	AECB07 17
	predefined types?	integer, string, Boolean, real, time	i contenio or	200	02011	
	I JI					
		•				

S.No	QUESTION	ANSWER	Blooms Level	СО	CLO	CLO Code
28	What is "abs" in VHDL?	absolute value	Understand	CO 5	CLO 17	AECB07.17
29	What is "rem" in VHDL?	modulo remainder	Remember	CO 5	CLO 17	AECB07.17
30	What is "Mod" in VHDL?	modulo division	Remember	CO 5	CLO 16	AECB07.16
31	What is "**" in VHDL?	exponentiation	Understand	CO 5	CLO 16	AECB07.16
32	What is an array in VHDL?	an ordered set of elements of the same type, where each element is selected by an <i>array</i> <i>index</i>	Remember	CO 5	CLO 16	AECB07.16
33	What is "string" in VHDL?	a sequence of ISO characters enclosed in double quotes	Remember	CO 5	CLO 16	AECB07.16
34	What is library in VHDL?	a place where the VHDL compiler stores information about a particular design project, including intermediate files that are used in the analysis, simulation, and synthesis of the design	Understand	CO 5	CLO 16	AECB07.16
35	What is package in VHDL?	a file containing definitions of objects that can be used in other programs	Remember	CO 5	CLO 15	AECB07.15
36	What is structural description or structural design in VHDL?	it defines the precise interconnection structure of signals and entities that realize the entity	Remember	CO 5	CLO 15	AECB07.15
37	What is Dataflow Modeling in VHDL?	Behavioral modeling can be done with sequential statements using the process construct or with concurrent statements	Understand	CO 5	CLO 15	AECB07.15
38	What is Null statement in VHDL?	The null statement states that no action will occur	Remember	CO 5	CLO 15	AECB07.15
39	What is wait statement in VHDL?	The wait statement will halt a process until an event occurs	Remember	CO 5	CLO 15	AECB07.15
40	What is Next and Exit Statement in VHDL?	The next statement skips execution to the next iteration of a loop statement and proceeds with the next iteration.	Understand	CO 5	CLO 15	AECB07.15

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4