HallTicketNo | | | | | | | | | | | Question Paper Code:CAEC516

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

MODEL QUESTION PAPER

B.TechIII Semester End Examinations,November - 2018

Regulations: IARE-R16

DIGITAL IC APPLICATIONS USING VHDL

(Common to ECE)

Time: 3 hours **Max. Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1	a)	Design a 2 input XOR gate circuit using AOI and OAI logic family with required truth table and explanation.	[7M]
	b)	Design a 2 input TTL NAND gate circuit with totem pole output logic with the necessary functiona table and description.	[7M]
2	a)	Explain the operation of steady state and dynamic electrical behavior of CMOS logic with the needed description.	[7M]
	b)	Design a 2 input NOR gate using bipolar logic and compare the performance with respect to CMOS logic.	[7M]

UNIT – II

3	a)	With suitable diagrams, explain the working flow of VLSI design and mention each block significance in designing aspect.	[7M]
	b)	Design a 3 input XOR gate using structural level modelling in very high speed hardware description language .	[7M]
4	a)	Explain the libraries and packages used in very high speed integrated circuit hardware description language.	[7M]
	b)	Explain the data flow design elements , simulation and synthesis in very high speed hardware description language.	[7M]

UNIT – III

5	a)	Design a 16:4 encoder using 4:2 encoder and write the VHDL code using component instantiation technique.	[7M]
	b)	Implement 1 bit ALU with required block diagrams and write VHDL code using structural modeling.	[7M]
6	a)	Design a 4 x 4 multiplier using full adders and synthesis the multiplier design using VHDL with any programing style of VHDL.	[7M]

	b)	Implement a 4 bit magnitude comparator using logic gates and write the VHDL program for 4 bit magnitude comparator.	[7M]

UNIT – IV

7	a)	Design a 4 bit shift register using D dlip flop and write the code for D flip flop with reset in VHDL .	[7M]
	b)	Explain the operation of programmable logic devives and write the VHDL code full adder using PLA.	[7M]
8	a)	Implement a 4 bit synchronous counter and write the VHDL code for synchronous counter using for loop.	[7M]
	b)	Explain the timing diagram of D flip flop and write the VHDL code for D flip flop using data flow modeling.	[7M]

UNIT – V

9	a)	Explain the internal structure of SRAM decoding and its applications applications with relevant block diagrams and timing waveforms.	[7M]
	b)	Explain the working principle of DRAM structure and read and write operations of DRAM with the help of timing diagram.	[7M]
10	a)	Explain the architecture of Cypress CY6116 and it components by giving its neat working block diagrams.	[7M]
	b)	Draw and analyse read and write operations of SRAM structure with the help of timing diagram.	[7M]

INSTITUTE OF AERONAUTICAL ENGINEERING

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I. COURSE OBJECTIVES

The course should enable the students to:

S.No	Description
I	Familiarization of Digital Logic families.
II	Design of combinational circuits using digital ICs.
III	Design of sequential circuits using digital ICs.
IV	Strategy of digital circuits using VHDL Programming
V	Acquire Knowledge of memories like SRAM, DRAM memory construction, operation and timing diagrams.

II. COURSE LEARNING OUTCOMES

Students who complete the course will have demonstrated the ability to do the following

S. No	Description
CAEC516.01	Understand logic families of CMOS, TTL and ECL
CAEC516.02	Construct the circuits of CMOS basic gates like inverter, NAND, NOR, AOI and OAI logic with functionality verification.
CAEC516.03	Construct the circuits of TTL logic family by understanding NAND, NOR gates with functionality verification.
CAEC516.04	Identify the need of interfacing CMOS logic family with TTL logic family and interfacing TTL with CMOS logic.
CAEC516.05	Understand the Static and dynamic electrical behavior of CMOS circuits.
CAEC516.06	Understand the different design methods in VHDL.
CAEC516.07	Acquire the basic constucts in VHDL programming.
CAEC516.08	Understand the terms simulation and synthesis in the area of VLSI.
CAEC516.09	Familarization of basic combinational circuits viz decoders, encoders, multiplexers, demultiplexers, parity circuits.
CAEC516.10	Familarization of basic arithmetic circuits for addition, subtraction and multiplication.
CAEC516.11	Distinguish between combinatorial and sequential circuits.
CAEC516.12	Design sequential circuits like latches, flip-flops.
CAEC516.13	Design sequential circuits like shift registers and counters.
CAEC516.14	Understand synchronous design methodology
CAEC516.15	Learns impediments to synchronous design
CAEC516.16	Understand internal structure of SRAM and decoding mechanism
CAEC516.17	Understand timing diagrams of SRAM for read and write operations
CAEC516.18	Understand internal structure of DRAM
CAEC516.19	Understand timing diagrams of DRAM for read and write operations

MAPPING OF SEMESTER END EXAMINATION TO COURSE LEARNING OUTCOMES

SEE Question No.		Course learning Outcomes		Blooms Taxonomy Level
1	a	CAEC516.02	Construct the circuits of CMOS basic gates like inverter, NAND, NOR, AOI and OAI logic with functionality verification.	Understand
	b	CAEC516.03	Construct the circuits of TTL logic family by understanding NAND, NOR gates with functionality verification.	Understand
2	a	CAEC516.05	Understand the Static and dynamic electrical behavior of CMOS circuits.	Remember
	b	CAEC516.01	Understand logic families of CMOS, TTL and ECL	Understand
3	a	CAEC516.06	Understand the different design methods in VHDL.	Understand
	b	CAEC516.07	Acquire the basic constucts in VHDL programming.	Understand
4	a	CAEC516.07	Acquire the basic constucts in VHDL programming.	Remember
	b	CAEC516.07	Acquire the basic constucts in VHDL programming.	Understand
5	a	CAEC516.09	Familarization of basic combinational circuits viz decoders, encoders, multiplexers, demultiplexers, parity circuits.	Remember
	b	CAEC516.10	Familarization of basic arithmetic circuits for addition, subtraction and multiplication.	Remember
6	a	CAEC516.09	Familarization of basic combinational circuits viz decoders, encoders, multiplexers, demultiplexers, parity circuits.	Understand
	b	CAEC516.13	Design sequential circuits like shift registers and counters.	Remember
7	a	CAEC516.13	Design sequential circuits like shift registers and counters.	Remember
	b	CAEC516.14	Understand synchronous design methodology.	Understand
8	a	CAEC516.12	Design sequential circuits like shift registers and counters.	Remember
	b	CAEC516.12	Design sequential circuits like latches, flip-flops.	Understand
9	a	CAEC516.16	Understand internal structure of SRAM and decoding mechanism.	Understand
	b	CAEC516.19	Understand timing diagrams of DRAM for read and write operations.	Remember
10	a	CAEC516.19	Understand timing diagrams of DRAM for read and write operations.	Understand
	b	CAEC516.16	Understand internal structure of SRAM and decoding mechanism.	Understand

Signature of Course Coordinator **HOD, ECE**