# INSTITUTE OF AERONAUTICAL ENGINEERING

**(Autonomous)**

Dundigal, Hyderabad - 500 043

## COMPUTER SCIENCEAND ENGINEERING

### DEFINITIONS AND TERMINOLOGY

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| **Course Title** | **MICROPROCESSORS AND INTERFACING** | | | | |
| **Course Code** | AEC021 | | | | |
| **Programme** | B.Tech | | | | |
| **Semester** | V | CSE | | | |
| **Course Type** | Core | | | | |
| **Regulation** | IARE - R16 | | | | |
| **Course Structure** | **Theory** | | | **Practical** | |
| | **Lectures** | **Tutorials** | **Credits** | **Laboratory** | **Credits** |
| | 3 | 1 | 4 | 3 | 2 |
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**OBJECTIVES:**

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| I | To help students to consider in depth the terminology and nomenclature used in the syllabus. |
| II | To focus on the meaning of new words / terminology/nomenclature |

## DEFINITIONS AND TERMINOLOGY QUESTION BANK

| S No | QUESTION | ANSWER | BLOOMS TAXONOMY LEVEL | CO | CLO | CLO Code |
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| **UNIT – I<br>OVERVIEW OF 8086 MICROPROCESSOR** | | | | | | |
| 1. | Define a microprocessor? | A processor on a single integrated circuit.<br>In the world of personal computers, the terms microprocessor and CPU are used interchangeably | Remember | CO 1 | CLO 1 | AEC021.01 |
| 2. | What is a clock speed? | The clock speed determines how many instructions per second the processor can execute | Understand | CO 1 | CLO 1 | AEC021.01 |
| 3. | What is a RISC processor? | RISC stands for Reduced Instruction Set Computer. It is designed to reduce the execution time by simplifying the instruction set of the computer. | Remember | CO 1 | CLO 1 | AEC021.01 |

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| 4. | What is an Input device? | A device that allows input of information to a computer. | Remember | CO 1 | CLO 1 | AEC021.01 |
| 5. | What is an Interface? | Interfacing a microprocessor is to connect it with various peripherals to perform various data operations and controlling of the devices. | Remember | CO 1 | CLO 1 | AEC021.01 |
| 6. | What is a CISC processor? | CISC stands for Complex Instruction Set Computer. It is designed to minimize the number of instructions per program, ignoring the number of cycles per instruction. | Remember | CO 1 | CLO 1 | AEC021.01 |
| 7. | What is a coprocessor? | A coprocessor is a specially designed microprocessor, which can handle its particular function many times faster than the ordinary microprocessor. | Remember | CO 1 | CLO 1 | AEC021.01 |
| 8. | What are the features of processor? | The main internal hardware of processor consists, external memory, registers, control unit, and ALU.<br>Registers are processor components that hold information and address. To execute a program, the system copies it from the external device into the internal memory.<br>The processor executes the program instructions. | Understand | CO 1 | CLO 1 | AEC021.01 |
| 9. | Explain the fundamental unit in computer or processor storage? | The fundamental unit of computer storage is a bit; it could be ON (1) or OFF (0).<br>A group of 9 related bits makes a byte, out of which eight bits are used for information and the final one is used for parity. According to the rule of parity, the number of bits that are ON (1) in each byte should always be odd.<br>The parity bit is used to make the number of bits in a byte odd. If the parity is even, the system assumes that there had been a parity error (though rare), which might have been caused due to hardware fault or electrical disturbance. | Understand | CO 1 | CLO 1 | AEC021.01 |
| 10. | Define addressing modes? | The term addressing modes refers to the way in which the operand of an instruction is specified. | Understand | CO 1 | CLO 4 | AEC021.04 |
| 11. | Define ALU? | An arithmetic logic unit (ALU) is a digital circuit used to perform arithmetic and logic operations. | Understand | CO 1 | CLO 2 | AEC021.02 |
| 12. | What is the speed of a microprocessor? | Time required executing a basic instruction | Understand | CO 1 | CLO 2 | AEC021.02 |
| 13. | What is an ISR? | ISR (Interrupt Service Routine)is a short program to instruct the | Understand | CO 1 | CLO 4 | AEC021.04 |

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| | | microprocessor on how to handle the interrupt. | | | | |
| 14. | Define Assembler? | Assembler converts instructions written in low-level symbolic code into machine code. | Remember | CO 1 | CLO 5 | AEC021.05 |
| 15. | What is Architecture? | Architecture is the study of internal logic circuitry. | Understand | CO 1 | CLO 2 | AEC021.02 |
| 16. | What is a Control Unit? | Provides necessary timing and control signals to all the operation of the microprocessor and microprocessor system | Understand | CO 1 | CLO 1 | AEC021.01 |
| 17. | What is a Register? | The Registers are a mini-storage area for data used by the Arithmetic Logic Unit (ALU) to complete the tasks the Control Unit has requested. | Remember | CO 1 | CLO 3 | AEC021.03 |
| 18. | What is a pre-fetch unit? | The pre-fetch Unit decides when to order data and instructions from the Instruction Cache or the computer's main memory based on commands or the task at hand. | Understand | CO 1 | CLO 2 | AEC021.02 |
| 19. | What is a decode unit? | The Decode Unit decodes or translates complex machine language instructions into a simple format understood by the Arithmetic Logic Unit (ALU) and the Registers. This makes processing more efficient. | Understand | CO 1 | CLO 1 | AEC021.01 |
| 20. | What is a flag register? | Flag Register shows the status of the microprocessor before/after an operation. | Understand | CO 1 | CLO 3 | AEC021.03 |
| 21. | What is a carry flag? | Carry Flags set if there is a carry or borrow from arithmetic operation | Understand | CO 1 | CLO 3 | AEC021.03 |
| 22. | What is a program counter? | Program Counter (PC) is a register that is used to control the sequencing of the execution of instructions. This register always holds the address of the next instruction | Understand | CO 1 | CLO 2 | AEC021.02 |
| 23. | What is a stack? | Stack is an area of memory identified by the programmer for temporary storage of information. | Remember | CO 1 | CLO 2 | AEC021.02 |
| 24. | What is an address bus? | Address bus carries the address, which is a unique binary pattern used to identify a memory location or an I/O port. | Understand | CO 1 | CLO 2 | AEC021.02 |
| 25. | What are the hardware interrupts of 8086? | The interrupts of 8086 are INTR and NMI. The INTR is general maskable interrupt and NMI is non-maskable interrupt. | Understand | CO 1 | CLO 4 | AEC021.04 |
| 26. | What is a segment register? | The segment registers stores segment base address of the memory segment. | Understand | CO 1 | CLO 2 | AEC021.02 |

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| 27. | What is a ready signal | This is the acknowledgment from the slow devices (or) memory that they have completed the data transfer. | Understand | CO 1 | CLO 2 | AEC021.02 |
| 28. | What is ALE? | ALE -Address Latch Enable: This signal indicates the availability of the valid address on the address / data lines. | Remember | CO 1 | CLO 2 | AEC021.02 |
| 29. | What is DEN signal? | DEN signal indicates the availability of valid data over the address / data lines. | Understand | CO 1 | CLO 2 | AEC021.02 |
| 30. | What is a numeric processor? | The numeric processor 8087 is a coprocessor which has been designed to work under the control of the processor 8086 and offer it additional numeric processing capabilities. | Remember | CO 1 | CLO 5 | AEC021.05 |
| 31. | Define bit. | Bit is the smallest unit of memory storage. | Remember | CO 1 | CLO 2 | AEC021.02 |
| 32. | What is Von Neumann Architecture? | Data and instructions stored in a single memory unit. | Remember | CO 1 | CLO 2 | AEC021.02 |
| 33. | What is Harvard Architecture | Data and instructions stored in a separate memory units. | Remember | CO 1 | CLO 2 | AEC021.02 |
| 34. | What is machine instruction? | Machine instruction is binary code for processing by hardware. | Understand | CO 1 | CLO 4 | AEC021.04 |
| 35. | What is direct addressing mode? | In Direct Addressing Mode, the address of the data is specified as the Operand in the instruction. Using Direct Addressing Mode, we can access any register or on-chip variable. This includes general purpose RAM, SFRs, I/O Ports, Control registers. Example:MOVA,47H | Remember | CO 1 | CLO 4 | AEC021.04 |
| 36. | What is assembler directives? | Assembler directives directs the assembler to do something. As the name says, it directs the assembler to do a task. | Understand | CO 1 | CLO 5 | AEC021.05 |
| 37. | Define byte (DB) directive? | Define Byte [DB] directive defines the byte type variable. | Understand | CO 1 | CLO 5 | AEC021.05 |
| 38. | Define word (DW) directive? | Define Word [DW] directive defines items that are one word (two bytes) in length. | Understand | CO 1 | CLO 5 | AEC021.05 |
| 39. | Define quad word (DQ) directive? | Define Quad word [DQ] directive is used to tell the assembler to declare variable 4 words in length or to reserve 4 words of storage in memory. | Understand | CO 1 | CLO 5 | AEC021.05 |
| 40. | What is ten bytes (DT) directive? | Define Ten bytes [DT] is used to define the data items that are 10 bytes long. | Understand | CO 1 | CLO 5 | AEC021.05 |
| 41. | What is versatility? | The microprocessors are versatile as the same chip can be used in a number of applications by configuring the software program. | Understand | CO 1 | CLO 1 | AEC021.01 |

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| 42. | What is equ directive?? | This EQU directive is used to give a name to some value or to a symbol.<br>Each time the assembler finds the name in the program, it will replace the name with the value or symbol you given to that name. | Understand | CO 1 | CLO 5 | AEC021.05 |
| 43. | What is even directive?? | EVEN directive instructs the assembler to increment the location of the counter to the next even address if it is not already in the even address. | Understand | CO 1 | CLO 5 | AEC021.05 |
| 44. | What is group directive? | The GROUP directive is used to group the logical segments named after the directive into one logical group segment. | Understand | CO 1 | CLO 5 | AEC021.05 |
| 45. | What is PROC directive? | The PROC directive is used to identify the start of a procedure. The term near or far is used to specify the type of the procedure. | Understand | CO 1 | CLO 5 | AEC021.05 |
| 46. | What is OFFSET directive? | Offset directive is used to determine the offset or displacement of a named data item or procedure from the start of the segment which contains it. | Remember | CO 1 | CLO 9 | AEC021.09 |
| 47. | What is ORG directive? | The ORG directive allows setting a desired value at any point in the program. | Understand | CO 1 | CLO 9 | AEC021.09 |
| 48. | What is PROC directive? | PROC directive is used to identify the start of a procedure. | Understand | CO 1 | CLO 9 | AEC021.09 |
| 49. | What is SEGMENT directive? | SEGMENT directive is used to indicate the start of a logical segment | Understand | CO 1 | CLO 9 | AEC021.09 |
| 50. | What is Assume directive? | The ASSUME directive is used to tell the assembler that the name of the<br>logical segment should be used for a specified segment. | Understand | CO 1 | CLO 5 | AEC021.05 |
| **UNIT – II<br>PIN DIAGRAM OF 8086 AND AEESMBLY LANGUAGE PROGRAMMING** | | | | | | |
| 1. | What are the modes in which<br>8086 can operate? | The 8086 can operate in two modes and they are minimum (or uniprocessor) mode and maximum (or multiprocessor) mode. | Remember | CO 2 | CLO 7 | AEC021.07 |
| 2. | What is an Instruction format? | The assembler processes an Instruction it converts the instruction from its mnemonics form to standard machine language format called the "Instruction format". | Remember | CO 2 | CLO 8 | AEC021.08 |
| 3. | What is a system bus? | System bus is used for communication path between Microprocessor and peripherals. System bus is a group of wires used to carry the information bits. | Understand | CO 2 | CLO 8 | AEC021.08 |

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| 4. | Define Program? | Program is a set of instruction used to perform a task. | Remember | CO 2 | CLO 8 | AEC021.08 |
| 5. | Define Instruction? | Instruction is a command to the microprocessor to perform a task. | Remember | CO 2 | CLO 8 | AEC021.08 |
| 6. | Define Mnemonics? | Mnemonics is an abbreviation for each binary instruction word | Understand | CO 2 | CLO 8 | AEC021.08 |
| 7. | What is machine cycle? | A machine cycle consists of the steps that a computer's processor executes whenever it receives a machine language instruction. The cycle consists of three standard steps: fetch decode and execute. | Understand | CO 2 | CLO 8 | AEC021.08 |
| 8. | What are DAA and DAS Instructions? | **Decimal Adjust after BCD Addition:** When two BCD numbers are added, the DAA is used after ADD or ADC instruction to get correct answer in BCD.<br>**Decimal Adjust after BCD Subtraction:** When two BCD numbers are added, the DAS is used after SUB or SBB instruction to get correct answer in BCD. | Remember | CO 2 | CLO 8 | AEC021.08 |
| 9. | What is pipelining? | A technique used in advanced microprocessors where the microprocessor begins executing a second instruction before the first has been completed | Remember | CO 2 | CLO 8 | AEC021.08 |
| 10. | Which Interrupt Has The Highest Priority? | TRAP has the highest priority. | Remember | CO 2 | CLO 8 | AEC021.08 |
| 11. | Explain few Assembly Controls? | JMP Jump; Intel 80×86; unconditional jump (near [relative displacement from PC] or far; direct or indirect [based on contents of general purpose register, memory location, or indexed])<br>Jump Conditionally; Intel 80×86; conditional jump (near [relative displacement from PC] or far;<br>direct or indirect [based on contents of general purpose register, memory location, or indexed]) based on a tested condition: JA/JNBE, JAE/JNB,<br>JB/JNAE, JBE/JNA, JC, JE/JZ, JNC, JNE/JNZ, JNP/JPO, JP/JPE, JG/JNLE, JGE/JNL, JL/JNGE, JLE/JNG, JNO, JNS, JO, JS | Understand | CO 2 | CLO 9 | AEC021.09 |

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| 12. | Write about Assembly Condition Codes? | Condition codes are the list of possible conditions that can be tested during conditional instructions.<br>Typical conditional instructions include: conditional branches, conditional jumps, and conditional subroutine calls.<br>Some processors have a few additional data related conditional instructions, and some processors make every instruction conditional. Not all condition codes available for a processor will be implemented for every conditional instruction. | Understand | CO 2 | CLO 9 | AEC021.09 |
| 13. | Write about Data Movement? | Data movement instructions move data from one location to another. The source and destination locations are determined by the addressing | Remember | CO 2 | CLO 8 | AEC021.08 |
| 14. | What is the function of JA or JNBE and JE/JZ Instructions | • Jump if above, not below, or equal i.e. when CF and ZF = 0<br>• Jump if zero or equal i.e. when ZF = 1 | Remember | CO 2 | CLO 8 | AEC021.08 |
| 15. | What is the function of CALL and RET Instructions | • Calls a procedure whose address is given in the instruction and saves their return address to the stack.<br>• Returns program execution from a procedure (subroutine) to the next instruction or main program. | Understand | CO 2 | CLO 8 | AEC021.08 |
| 16. | What is the function of MOVS/MOVSB/MOVSW and CMPS/CMPSB/CMPSW Instructions | • Moves 8-bit or 16-bit data from the memory location(s) addressed by SI register to the memory location addressed by DI register.<br>• Compares the content of memory location addressed by DI register with the content of memory location addressed by SI register. | Remember | CO 2 | CLO 8 | AEC021.08 |
| 17. | What is Assembly Numbers? | Numerical data is generally represented in binary system. Arithmetic instructions operate on binary data. When numbers are displayed on screen or entered from keyboard, they are in ASCII form. | Understand | CO 2 | CLO 9 | AEC021.09 |
| 18. | Write about Assembly Arithmetic Instructions? | The processor instruction set provides the instructions ADD, SUB, MUL, DIV, INC, and DEC to perform arithmetic operations which tests according to the need of the program. | Understand | CO 2 | CLO 8 | AEC021.08 |

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| 19. | Write about Assembly Logical Instructions? | The processor instruction set provides the instructions AND, OR, XOR, TEST, and NOT Boolean logic, which tests, sets, and clears the bits according to the need of the program. | Understand | CO 2 | CLO 8 | AEC021.08 |
| 20. | What is Assembly Conditions? | Conditional execution in assembly language is accomplished by several looping and branching instructions. These instructions can change the flow of control in a program. Conditional execution is observed in two scenarios - Unconditional jump Conditional jump | Understand | CO 2 | CLO 8 | AEC021.08 |
| 21. | What is Assembly Strings? | We have already used variable length strings in our previous examples. The variable length strings can have as many characters as required. | Understand | CO 2 | CLO 9 | AEC021.09 |
| 22. | What is Assembly Procedures? | Procedures or subroutines are very important in assembly language, as the assembly language programs tend to be big in size. Procedures are recognized by a name. | Understand | CO 2 | CLO 9 | AEC021.09 |
| 23. | What is Assembly Recursion? | A recursive procedure is one that calls itself. There are kind of recursion: direct and indirect. In direct recursion, the procedure calls itself and in indirect recursion, the first procedure calls a second process, which in turn calls the first procedure. | Remember | CO 2 | CLO 9 | AEC021.09 |
| 24. | What Is mean by Cross- compiler? | A program runs on one machine and executes on another is called as cross- compiler Programs which compile on One Machine and Execute on Another machine is called cross compiler. | Remember | CO 2 | CLO 9 | AEC021.09 |
| 25. | What is Assembly Language Programming? | Assembly language programming is a low-level programming language for a computer or other programmable devicespecific to a particular computer architecture in contrast to most high-level programming languages, which are generally portable across multiple systems. assembly language is converted into executable system codethrough a utility application called an assembler like NASM, MASM, etc. | Understand | CO 2 | CLO 9 | AEC021.09 |

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| 26. | What are the advantages of Assembly Language Programming? | Advantages of using assembly language are –<br>- It requires less memory and execution time;<br>- It allows hardware-specific complex<br>- It is suitable for time-critical jobs;<br>- It is most suitable for writing interrupt provider routines and different memory resident programs. | Remember | CO 2 | CLO 9 | AEC021.09 |
| 27. | Give an example of Hexa decimal conversion to binary? | Hexadecimal number considered is (FAD8)H its equal binary form is - (1111 1010 1101 1000)B | Understand | CO 2 | CLO 9 | AEC021.09 |
| 28. | What is interrupt? | An interrupt is a signal sent to the processor that interrupts the current process. It may be generated by a hardware device or a software program. | Remember | CO 2 | CLO 9 | AEC021.9 |
| 29. | What Is Non-maskable Interrupts? | An interrupt which can be never be turned off (i.e., disabled) is known as Non-Maskable interrupt. | Remember | CO 2 | CLO 9 | AEC021.09 |
| 30. | What is PTR directive? | PTR operator is used to assign a specific type of a variable or to a label. | Remember | CO 2 | CLO 9 | AEC021.09 |
| 31. | What is PUBLIC directive? | The PUBLIC directive is used to instruct the assembler that a specified name or label will be accessed from other modules. | Understand | CO 2 | CLO 9 | AEC021.09 |
| 32. | What is INT21H? | INT 21H is used to call DOS Function. | Understand | CO 2 | CLO 9 | AEC021.09 |
| 33. | Define assembler? | Assembler converts instructions written in low-level symbolic code into machine code. | Understand | CO 2 | CLO 9 | AEC021.09 |
| 34. | What is base register? | BX is known as the base register, as it may be used in indexed addressing. | Understand | CO 2 | CLO 9 | AEC021.09 |
| 35. | What is count register? | CX is known as the count register. CX registers store the loop count in iterative operations. | Understand | CO 2 | CLO 8 | AEC021.08 |
| 36. | What is an instruction pointer? | Instruction Pointer (IP) stores the offset address of the next instruction to be done. | Understand | CO 2 | CLO 8 | AEC021.08 |
| 37. | What is END directive? | The END directive marks the end of an assembly language program | Understand | CO 2 | CLO 8 | AEC021.08 |
| 38. | What is ENDP directive? | ENDP (End Procedure) used to indicate the end of a procedure. | Understand | CO 2 | CLO 8 | AEC021.08 |
| 39. | What is ENDS directive? | ENDS-End of Segment directive marks the end of a logical segment. | Understand | CO 2 | CLO 8 | AEC021.08 |
| 40. | What Happens When Hlt Instruction is Executed in Processor? | The Micro Processor enters into Halt-State and the buses are tri-stated. | Understand | CO 2 | CLO 8 | AEC021.08 |

| UNIT – III<br>8255 PROGRAMMABLE PERIPHERAL INTERFACE (PPI) | | | | | | |
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| 1. | What are the features of 8255A? | The prominent features of 8255A are as follows −<br>- It consists of 3 8-bit IO ports i.e. PA, PB, and PC to enhance the flexibility of 8225. Address/data bus must be externally demux.<br>- It is TTL compatible.<br>- It has improved DC driving capability. | Remember | CO 3 | CLO 10 | AEC021.10 |
| 2. | What is the necessity of 8259A? | In a system, microprocessor may need to perform the following tasks in an efficient way using interrupt:<br>- Read ASCII characters from a keyboard on an interrupt basis.<br>- Count interrupts from a timer to produce a real time clock of seconds, minutes and hours.<br>- Communicate with an A/D converter.<br>- Communicate with a display or printer.<br>- Detect several emergency signals like power failure etc on an interrupt basis. | Remember | CO 3 | CLO 13 | AEC021.13 |
| 3. | What is the function of 8259A? | The Programmable Interrupt Controller (PIC) functions as an overall manager in an interrupt-driven system environment.<br>It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced and issues an interrupt to the CPU based on this<br>determination. | Remember | CO 3 | CLO 13 | AEC021.13 |
| 4. | What are the different types of command words used in 8259A? | The command words of 8259A are classified in two groups,<br>1.Initialization command words (ICWs)<br>2.Operation command words (OCWs) | Understand | CO 3 | CLO 13 | AEC021.13 |
| 5. | What are the types operating modes of 8259A? | (a)Fully Nested Mode<br>(b)End of Interrupt (EOI)<br>(c)Automatic Rotation<br>(d)Automatic EOI Mode<br>(e)Specific Rotation<br>(f)Special Mask Mode | Understand | CO 3 | CLO 13 | AEC021.13 |

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| | | (g)Edge and level Triggered Mode<br>(h)Reading 8259 Status<br>(i)Poll command<br>(j)Special Fully Nested Mode<br>(k)Buffered mode<br>(l)Cascade mode | | | | |
| 6. | What are the internal devices of a typical DAC? | The internal devices of a DAC are R/2R resistive network, an internallatch and current to voltage converting amplifier. | Understand | CO 3 | CLO 11 | AEC021.11 |
| 7. | What is settling or conversion time in DAC? | The time taken by the DAC to convert a given digital data tocorresponding analog signal is called conversion time. | Understand | CO 3 | CLO 11 | AEC021.11 |
| 8. | What are the different types of ADC? | The different types of ADC are successive approximation ADC, counter type ADC flash type ADC, integrator converters and voltage-to-frequency converters. | Understand | CO 3 | CLO 11 | AEC021.11 |
| 9. | What is interrupt? | An interrupt is a signal sent to the processor that interrupts the current process. It may be generated by a hardware device or a software program. | Remember | CO 3 | CLO 12 | AEC021.12 |
| 10. | What are Maskable/Non-Maskable Interrupt? | An interrupt that can be disabled by writing some instruction is known as Maskable Interrupt otherwise it is called Non-Maskable Interrupt. | Remember | CO 3 | CLO 12 | AEC021.12 |
| 11. | What Is Non-maskable Interrupts? | An interrupt which can be never be turned off (i.e., disabled) is known as Non-Maskable interrupt. | Remember | CO 3 | CLO 12 | AEC021.12 |
| 12. | What is ISR? | ISR Stands for "Interrupt Service Routine." An ISR (also called an interrupt handler) is a software process invoked by an interrupt request from a hardware device. It handles the request and sends it to the CPU, interrupting the active process. When the ISR is complete, the process is resumed. | Remember | CO 3 | CLO 12 | AEC021.12 |
| 13. | What is IRQ? | IRQ Stands for "Interrupt Request." PCs use interrupt requests to manage various hardware operations. Devices such as sound cards, modems, and keyboards can all send interrupt requests to the processor. | Remember | CO 3 | CLO 12 | AEC021.12 |
| 14. | What are the hardware interrupts of 8086? | The interrupts of 8086 are INTR and NMI. The INTR is general maskable interrupt and NMI is non-maskable interrupt. | Understand | CO 3 | CLO 12 | AEC021.12 |
| 15. | Which Interrupt Has The Highest Priority? | TRAP has the highest priority. | Remember | CO 3 | CLO 12 | AEC021.12 |

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| 16. | What is a programmable peripheral device? | If the functions performed by a peripheral device can be altered or changed by a program instruction then the peripheral device is called programmable device. Usually the programmable devices will have control registers. The device can be programmed by sending control word in the prescribed format to the control register. | Understand | CO 3 | CLO 10 | AEC021.10 |
| 17. | What is the need for a Port? | The I/O devices are generally slow devices and their timing characteristics do not match with processor timings. Hence the I/O devices are connected to system bus through the ports. | Understand | CO 3 | CLO 10 | AEC021.10 |
| 18. | Write about handshake port? | In handshake port, signals are exchanged between I/O device and port or between port andprocessor for checking or informing various condition of the device. | Understand | CO 3 | CLO 10 | AEC021.10 |
| 19. | What are the internal devices of 8255? | The internal devices of 8255 are port-A, port-B, port-C and Control register. The ports can be programmed for either input or output function in different operating modes. | Understand | CO 3 | CLO 10 | AEC021.10 |
| 20. | What are the operating modes of port -A 8255? | The port-A of 8255 can be programmed to work in anyone of the following operating modes asinput or output port.<br>Mode-0: Simple 1/0 port. Mode-l : Handshake 1/0 port<br>Mode-2 : Bidirectional 1/0 port | Understand | CO 3 | CLO 10 | AEC021.10 |
| 21. | What are the functions performed by port-C of 8255? | 1. The port-C pins are used for handshake signals.<br>2. Port-C can be used as an 8-bit parallel 1/0 port in mode-0.<br>3. It can be used as two numbers of 4-bit parallel port in mode-0.<br>4. The individual pins of port-C can be set or reset for various control applications. | Understand | CO 3 | CLO 10 | AEC021.10 |

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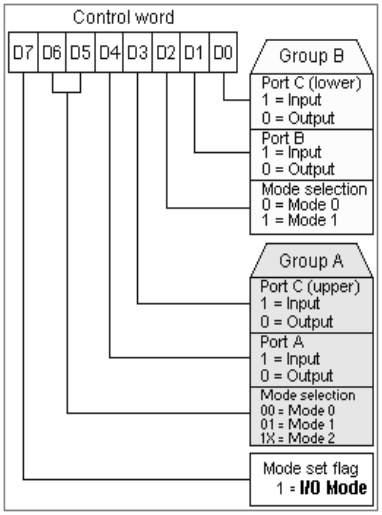
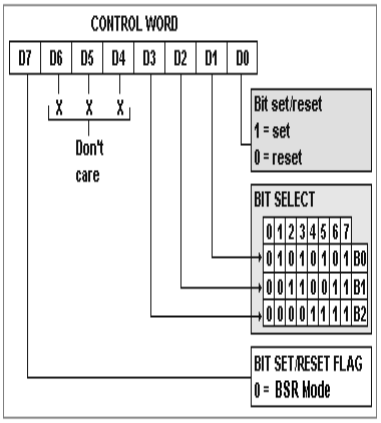
| 22. | Draw the control word format for I/O mode. |  | Understand | CO 3 | CLO 10 | AEC021.10 |
| 23. | Draw the control word format for BSR (Bit Set Reset) Mode. |  | Understand | CO 3 | CLO 10 | AEC021.10 |
| 24. | What are the different scan modes of 8279? | The different scan modes of 8279 are Decoded scan and Encoded scan. In decoded scan mode, the output of scan lines will be similar to a 2-to-4 decoder.<br>In encoded scan mode, the output of scan lines will be binary count, and so an external decodershould be used to convert the binary count to decoded output. | Understand | CO 3 | CLO 11 | AEC021.11 |
| 25. | What is de bouncing? | When a key is pressed, it bounces after a short time. If a key code is generated immediately aftersensing a key actuation, then the processor will generate the same keycode a number of times.(A key typically bounces for 10 to 20 msec). Hence the processor has to wait for the keybounces to settle before reading the keycode. This process is called keyboard de bouncing. | Understand | CO 3 | CLO 11 | AEC021.11 |
| 26. | What is the difference in programming the 8279 for encoded scan and decoded | If the 8279 is programmed for decoded scan then the output of scan lines will be decoded outputand if it is programmed for, encoded scan then the output of scan lines will be binary count. | Remember | CO 3 | CLO 13 | AEC021.13 |

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| | scan? | Inencoded mode, an external decoder should be used to decode the scan lines. | | | | |
| 27. | What is scanning in keyboard and what is scan time? | The process of sending a zero to each row of a keyboard matrix and reading the columns for keyactuation is called scanning. The scan time is the time taken by the processor to scan all therows one by one starting from first row and coming back to the first row again. | Remember | CO 3 | CLO 11 | AEC021.11 |
| 28. | What are the tasks involved in keyboard interface? | The tasks involved in keyboard interfacing are sensing a key actuation, de bouncing the key and generating key codes (Decoding the key). These tasks are performed by software if the keyboardis interfaced through ports and they are performed by hardware if the keyboard is interfacedthrough 8279. | Remember | CO 3 | CLO 11 | AEC021.11 |
| 29. | What is meant by 2-key lockout and N-key rollover? | 2-Key Lockout: When two keys are pressed simultaneously, one key pressed first will berecognized and code will be generated.<br>N-Key Rollover: When a key is pressed continuously, the same key will be recognized several times, after each de bounce. | Understand | CO 3 | CLO 11 | AEC021.11 |
| 30. | Write about Memory interfacing in 8086 microprocessor? | If any instruction is executed then we require microprocessor to access the memory in order to read the instruction codes and the stored data in the memory. So, to read from the memory and write in registers this memory and microprocessor need some signals. There are some key factors that are required in interfacing process to match with the memory requirements and microprocessor signals. So, the interfacing circuit must be designed in such a way that it should match with the memory signal requirements and the signals of the microprocessor. | Understand | CO 3 | CLO 11 | AEC021.11 |
| 31. | What is I/O Interfacing in 8086 microprocessor? | IO interfacing is the communication between various devices like keyboard, mouse, printer, etc. It is a set of registers where CPU communicates and controls the I/O device with the help of reading and writing registers. | Understand | CO 3 | CLO 11 | AEC021.11 |

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| | | These registers are connected to the CPU using buses. So, in order to interface between keyboard and other devices with the microprocessor latches and buffers are used. This type of interfacing is known as I/O interfacing. | | | | |
| 32. | What is programmable keyboard? | It is a specially designed type of programmable keyboard/display controller launched by Intel which helps in interfacing the keyboard with the CPU. It identifies any type of key that has been pressed with the help of scanning.<br>It then sends the response of the pressed key to the CPU and vice-a-versa. | Understand | CO 3 | CLO 11 | AEC021.11 |
| 33. | How Many Ways the Keyboard are Interfaced with the CPU? | The Keyboard can be interfaced in two modes that is either in the interrupt or the polled mode.<br>In the Interrupt mode, whenever any key is pressed then the request is sent by the processor, otherwise the CPU will continue to follow with its main task. In the Polled mode, the CPU periodically reads an internal flag of 8279 and checks whether any key is pressed or not with any pressure exerted by the key. | Understand | CO 3 | CLO 11 | AEC021.11 |
| 34. | How Does 8279 Keyboard Work? | The keyboard which acts as an input device contains maximum of 64 keys. With the help of keyboard the user can perform various types of tasks.<br>Certain specific key-codes are used where text is entered as an input with the keyboard. | Understand | CO 3 | CLO 11 | AEC021.11 |
| 35. | What is 8257 DMA controller? | 8257 DMA stands for 4-channel Direct Memory Access. It is specially designed by Intel for data transfer at the highest speed.<br>With the use of a DMA controller, the device sends requests to the CPU to hold its data, sequential memory address and control bus, which helps the device to transfer data directly to/from the memory.<br>The DMA data transfer is initiated only after receiving HLDA signal from the CPU. | Understand | CO 3 | CLO 11 | AEC021.11 |

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| 36. | How DMA Operations are Performed? | Primarily, when any device requires to send data between the device and the memory, the device need to send DMA request (DRQ) to DMA controller. The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA signal.<br>Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU leaves the control over bus and acknowledges the HOLD<br>request through HLDA signal. | Understand | CO 3 | CLO 11 | AEC021.11 |
| 37. | What are the features of 8257? | The prominent features of 8257 –<br>• It has four channels which can be exhibited over four I/O devices.<br>• Each channel has 16-bit address and 14-bit counter.<br>• Data transfer of each channel can be taken up to 64kb. Each channel can be programmed independently.<br>• Each channel can perform certain specific actions i.e., read transfer, write transfer and verify transfer operations. | Understand | CO 3 | CLO 13 | AEC021.13 |
| 38. | What is Programmable Peripheral Interface? | The 8255A is generally seen as 8-bit bidirectional data buffer, which is specially designed to transfer the data with the execution of input output instructions requested by the CPU. It has the ability to use with almost any microprocessor.<br>It consists of three 8-bit bidirectional I/O ports (24 I/O lines) which can be<br>configured with their different functional characteristics, each possessing unique features to upgrade the flexibility of 8255. | Understand | CO 3 | CLO 10 | AEC021.10 |
| 39. | What are the different Ports of 8255A? | 8255A consists of three ports, i.e., PORT A, PORT B, and PORT C.<br>Port A contains one 8-bit output latch/buffer and one 8-bit input buffer possessing both pull-up and pull-down devices present in Port A.<br>Port B is similar to PORT A.<br>Port C can be split into two parts, i.e. PORT C lower (PC0-PC3) and PORT C upper (PC7-PC4) with the help of control word. | Understand | CO 3 | CLO 10 | AEC021.10 |

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| | | These three ports are further classified into two groups, i.e. Group A includes PORT A and upper PORT C. Group B includes PORT B and lower PORT C. These two groups can be programmed in three different modes, i.e. the first mode is named as mode 0, the second mode is named as Mode 1 and the third mode is named as Mode 2. | | | | |
| 40. | What are the Operating Modes in 8255A? | Mode 0 − In this mode, Port A and B is used as two 8-bit ports and Port C as two 4-bit ports. Mode 1 − In this mode, Port A and B are used as 8-bit I/O ports. They can be configured as either input or output ports. Mode 2 − In this mode, Port A can be configured as the bidirectional port and Port B can be available in Mode 0 or Mode 1. | Understand | CO 3 | CLO 10 | AEC021.10 |
| **UNIT – IV SERIAL DATA TRANSFER SCHEMES** | | | | | | |
| 1. | What are the Ways of Communication − Microprocessor with the Outside World? | There are two ways of communication in which the microprocessor can connect with the outside world. Serial Communication Interface Parallel Communication interface | Understand | CO 4 | CLO 14 | AEC021.14 |
| 2. | What are the different types of methods used for data transmission? | The data transmission between two points involves unidirectional or bi- directional transmission of meaningful digital data through a medium. There are basically there modes of data transmission (a)Simplex (b)Duplex (c)Half Duplex | Understand | CO 4 | CLO 14 | AEC021.14 |
| 3. | What is the use of modem control unit in 8251? | The modem control unit handles the modem handshake signals to coordinate the communication between the modem and the USART. | Remember | CO 4 | CLO 15 | AEC021.15 |
| 4. | What are the various Programmed data transfer methods? | i) Synchronous data transfer ii) Asynchronous data transfer iii)Interrupt driven data transfer | Understand | CO 4 | CLO 14 | AEC021.14 |
| 5. | What is the use of 8251 chip? | Intel's 8251A is a universal synchronous asynchronous receiver and transmitter compatible with Intel's Processors. | Understand | CO 4 | CLO 15 | AEC021.15 |

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| 6. | What is baud rate? | The baud rate is the rate at which the serial data is transmitted (expressed as bits per second).<br>Baud rate is also defined as l/(Tb - time period for a symbol). In some systems, one data bit maybe represented through one symbol. Then, on such<br>occasions, the baud rate and bits/sec aresame. | Understand | CO 4 | CLO 14 | AEC021.14 |
| 7. | What are the different types of errors that can occur in asynchronous serial communication? | 1. Framing Error<br>2. Over run Error<br>3. Parity Error | Understand | CO 4 | CLO 14 | AEC021.14 |
| 8. | What is the significance of C/D signal in 8251? | This pin is used to select either Control register for configuring or Data bus buffer for read /write operations. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 9. | What is USART? What are the functions performed by INTEL 8251A? | The device which can be programmed to perform Synchronous or Asynchronous serial communication is called USART (Universal Synchronous Asynchronous Receiver Transmitter).<br>The INTEL 8251A is an example of USART.<br>The INTEL 825lA is used for serial data transmission or reception either asynchronously or synchronously. The 8251A can be used to interface<br>MODEM for serial communication through telephone lines. | Remember | CO 4 | CLO 15 | AEC021.15 |
| 10. | What are the control words of 8251A and what are its functions? | The control words of 8251A are Mode word and Command word. The mode word informs 8251about the baud rate, character length, parity and stop bits. The command word can be send toenable the data transmission and reception. | Remember | CO 4 | CLO 15 | AEC021.15 |
| 11. | What are the functions performed by INTEL 8251A? | The INTEL 825lA is used for converting parallel data to serial or vice versa. The data transmission or reception can be either asynchronously or synchronously. The 8251A can be used to interface MODEM and establish serial communication through MODEM over telephone lines. | Understand | CO 4 | CLO 15 | AEC021.15 |

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| 12. | What is RS-232C Standard? | The RS232C is a serial bus consisting of a maximum of 25 signals, which are standardized by EIA (Electronic Industry Association). The first 9 signals are sufficient for most of the serial data transmission. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 13. | What is the voltage level used in RS232C standard? | The voltage levels are<br>Logic LOW (0) : –3V to –15V<br>Logic HIGH (1) : +3V to +15V<br>Commonly used voltage levels are +12V (logic HIGH) and –12V (logic LOW). | Understand | CO 4 | CLO 15 | AEC021.15 |
| 14. | What are the various programmed data transfer methods? | i. Synchronous data transfer<br>ii. Asynchronous data transfer<br>iii. Interrupt driven data transfer | Understand | CO 4 | CLO 14 | AEC021.14 |
| 15. | Define USART? | 8251A is a USART (Universal Synchronous Asynchronous Receiver Transmitter) for serial data communication. Programmable peripheral designed for synchronous/asynchronous serial data communication, packaged in a 28-pin DIP. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 16. | What is status word register? | Checks the ready status of the peripheral. Status word register provides the information concerning register status and transmission errors. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 17. | Define program status word? | The Program Status Word or PSW is a collection of data 8 bytes (or 64 bits) long, maintained by the operating system. It keeps track of the current state<br>of the system. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 18. | What is RS 232? | An RS-232 serial port was once a standard feature of a computer, used for connections to modems, printers, mice, data storage, uninterruptible power supplies, and other peripheral devices. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 19. | Define USB system? | A Universal Serial Bus (USB) is a common interface that enables communication between devices and a host controller such as a personal computer (PC). | Understand | CO 4 | CLO 16 | AEC021.16 |
| 20. | What is USB cable? | USB cables are designed to ensure correct connections by having different connectors on host and devices, it is possible to connect; two hosts or two devices together.USB requires a shielded cable containing 4 wires. | Understand | CO 4 | CLO 16 | AEC021.16 |

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| 21. | Define USB host? | The USB host communicates with the devices using a USB host controller. The host is responsible for detecting and enumerating devices, managing bus access, performing error checking, providing and managing power, and exchanging data with the devices. | Understand | CO 4 | CLO 16 | AEC021.16 |
| 22. | What are control transfers? | Control transfers are used to configure and retrieve information about the device capabilities. | Remember | CO 4 | CLO 15 | AEC021.15 |
| 23. | What is Control Register? | This is a 16-bit register for a control word consists of two independent bytes; the first byte is called Mode Instruction (Word) and the second byte is called the Command Instruction (Word). This register can be accessed as an output port when the pin is high. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 24. | What is data bus buffer? | This is a tri state bidirectional buffer used to interface the 8255 to system data bus. Data is transmitted or received by the buffer on execution of input or output instruction by the CPU. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 25. | What is Strobe control? | Strobe control method of data transfer uses a single control signal for each transfer. The strobe may be activated by either the source unit or the www.eazynotes.com destination unit. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 26. | What is Status Register? | This input register checks the ready status of a peripheral. This register is addressed as an input port when the c/đ pin is high. It has the same port address as the control register. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 27. | What is Token packet? | The bit packet that commands the device either to receive data or transmit data in transmission of USB asynchronous communication is Token packet. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 28. | What is Data bus buffer? | Data bus buffer helps in interfacing the internal data bus of 8251 to the system data bus. The data transmission is possible between 8251 and CPU by the data bus buffer block. | Remember | CO 4 | CLO 15 | AEC021.15 |
| 29. | Define Modem. | Modem is a device converts analog signals to digital signals and vice-versa and helps the computers to communicate over telephone lines or cable wires. | Understand | CO 4 | CLO 15 | AEC021.15 |

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| 30. | What is Transmit buffer**?** | **Transmit buffer** is used for parallel to serial converter that receives a parallel byte for conversion into serial signal and further transmission onto the common channel. | Understand | CO 4 | CLO 16 | AEC021.16 |
| 31. | What is Receiver Buffer? | The receiver buffer accepts serial data on the RxD line, coverts this serial data to parallel formats, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to CPU. | Understand | CO 4 | CLO 16 | AEC021.16 |
| 32. | What does USB stand for? | USB stands for Universal Serial Bus, and it represents an industry standard for cables, connectors and communications protocols, used for the connection, communication, and power supply between various computing devices. | Understand | CO 4 | CLO 16 | AEC021.16 |
| 33. | What is Asynchronous Data Transfer? | The mode in which the bits of data are not synchronized by a clock pulse. Clock pulse is a signal used for synchronization of operation in an electronic system. | Understand | CO 4 | CLO 14 | AEC021.14 |
| 34. | What is Synchronous Data Transfer? | The mode in which the bits of data are synchronized by a clock pulse. | Understand | CO 4 | CLO 14 | AEC021.14 |
| 35. | What are the functional types used in control words of 8251a? | The control words of 8251A are divided into two functional types. 1.Mode Instruction control word 2.Command Instruction control word | Understand | CO 4 | CLO 15 | AEC021.15 |
| 36. | What is RS232? | RS232 is a standard protocol used for serial communication, it is used for connecting computer and its peripheral devices to allow serial data exchange between them. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 37. | What is Handshaking? | Handshaking is the process which is used to transfer the signal from DTE to DCE to make the connection before the actual transfer of data. The messaging between transmitter & receiver can be done by handshaking. | Remember | CO 4 | CLO 14 | AEC021.14 |
| 38. | What are the control words of 8251A and what are its functions? | The control words of 8251A are Mode word and Command word. The mode word informs 8251about the baud rate, character length, parity and stop bits. The command word can be send to enable the data transmission and reception | Understand | CO 4 | CLO 15 | AEC021.15 |

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| 39. | What is RS 232C interface? | RS-232C is a long-established standard ("C" is the current version) that describes the physical interface and protocol for relatively low-speed serial data communication between computers and related devices. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 40. | Define Parity error. | A parity error occurs when the parity of the number of one-bits disagrees with that specified by the parity bit. Use of a parity bit is optional, so this error will only occur if parity-checking has been enabled. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 41. | Define Overrun error. | An "overrun error" occurs when the receiver cannot process the character that just came in before the next one arrives. If the CPU or DMA controller does not service the UART quickly enough and the buffer becomes full, an Overrun Error will occur, and incoming characters will be lost. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 42. | What is Read/Write control logic? | It is a control block for overall device. It controls the overall working by selecting the operation to be done. | Remember | CO 4 | CLO 15 | AEC021.15 |
| 43. | Why is USART used? | USART Serial Data Communication in AVR Microcontroller.<br>The USART stands for universal synchronous and asynchronous receiver and transmitter. It is a serial communication of two protocols. This protocol is used for transmitting and receiving the data bit by bit with respect to clock pulses on a single wire. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 44. | What is RS232 Protocol? | In RS232, 'RS' stands for Recommended Standard. It defines the serial communication using DTE and DCE signals. Here, DTE refers to Data Terminal Equipment and DCE refers to the Data Communication Equipment. | Understand | CO 4 | CLO 15 | AEC021.15 |
| 45. | What is UBRR (USART Baud Rate Register)? | This register is 16BIT wide so **UBRRH **is the High Byte and **UBRRL **is Low byte. But as we are using C language it is directly available as UBRR and compiler manages the 16BIT access. This register is used by the USART to generate the data transmission at specified speed (say 9600Bps) | Understand | CO 4 | CLO 16 | AEC021.16 |

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| 46. | What is Software Handshaking? | Software Handshaking in RS232 involves two special characters for starting and stopping the communication. These characters are X-ON and X-OFF (Transmitter On and Transmitter OFF). | Understand | CO 4 | CLO 16 | AEC021.16 |
| 47. | Define slew rate. | The change of input voltage determines the rate at which the RS232 driver responds. This is often termed as slew rate. | Understand | CO 4 | CLO 16 | AEC021.16 |
| 48. | What is Hardware Handshaking? | The flow control of data transmission and reception is done using hardware handshaking. | Remember | CO 4 | CLO 16 | AEC021.16 |
| 49. | Define Data bits. | Data bits are a measurement of the actual data bits in a transmission. | Understand | CO 4 | CLO 16 | AEC021.16 |
| 50. | What is UDR: USART Data Register? | UDR: USART Data Register contains the received data or the transmitted data. | Understand | CO 4 | CLO 16 | AEC021.16 |
| 51. | What is USB Host Controller? | A USB Host Controller is the hardware either on the computer motherboard or PCI card. It provides an interface for transferring streams of data between the host computer and the USB devices. The host computer may have one or multiple USB host controllers with different types of interface. | Understand | CO 4 | CLO 16 | AEC021.16 |
| 52. | What is Software Handshaking? | Software Handshaking in RS232 involves two special characters for starting and stopping the communication. These characters are X-ON and X-OFF (Transmitter On and Transmitter OFF). | Understand | CO 4 | CLO 16 | AEC021.16 |
| 53. | What is USB Host Controller Interface? | A Host Controller Interface (HCI) is a register level interface which allows host controller hardware to communicate with the operating system of a host computer. | Understand | CO 4 | CLO 16 | AEC021.16 |
| UNIT-V<br>**ADVANCED MICROPROCESSORS** | | | | | | |
| 1. | What is Intel 80286? | The Intel 80286 was a 16-bit microprocessor chip introduced in 1982. The 80286 chip contained a 24-bit address bus, capable of accessing up to 16 MB (megabytes) of RAM (random access memory) and multitasking, the OS. | Understand | CO 5 | CLO17 | AEC021.17 |
| 2. | Define segment descriptor? | Segment descriptors are a part of the segmentation unit, used for translating a logical address to a linear address. | Understand | CO 5 | CLO17 | AEC021.17 |

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| 3. | Define machine status word? | The machine status word consists of four flags used for the LMSW and SMSW instructions which are available in the instruction set of 80286 to write and read the MSW in real address mode. | Remember | CO 5 | CLO17 | AEC021.17 |
| 4. | What is protected virtual address mode? | When the 80286 is reset, it always starts its execution in real address mode, where in it performs the initialization of the IP, peripheral, enables interrupts, sets up descriptor tables and then it prepares for entering the protected virtual address mode. | Understand | CO 5 | CLO17 | AEC021.17 |
| 5. | Define swapping? | The procedure of fetching the chosen program segments or data from the secondary storage into the physical memory is swapping | Remember | CO 5 | CLO17 | AEC021.17 |
| 6. | Define unswapping? | The procedure of storing back the partial results or data back on to the secondary storage is called unswapping. | Remember | CO 5 | CLO17 | AEC021.17 |
| 7. | Define descriptor? | The segments or pages have been associated with a data structure known as a descriptor. The descriptor contains information on the page, and also carry relevant information regarding a segment, and its access rights. | Remember | CO 5 | CLO18 | AEC021.18 |
| 8. | What is page table cache? | The storage of 32 recently accessed page table entries to optimize the time, is known as page table cache. | Understand | CO 5 | CLO17 | AEC021.17 |
| 9. | What are gate descriptors? | The descriptors that are used for subroutines and interrupt service routines are gate descriptors. | Understand | CO 5 | CLO18 | AEC021.18 |
| 10. | What is system segment descriptor? | The 80286 has system segment descriptor, that is used for special system data segments, and control transfer operations. | Understand | CO 5 | CLO19 | AEC021.19 |
| 11. | What is interrupt gate and trap gate? | The gate that is used to specify a corresponding service routine is interrupt gate and trap gate. | Understand | CO 5 | CLO18 | AEC021.18 |
| 12. | What is task gate? | The gate that is used to switch from one task to another is task gate. | Understand | CO 5 | CLO17 | AEC021.17 |
| 13. | What is call gate? | The word count field is only used by a call gate descriptor, to indicate the number of bytes to be transferred from the stack of the calling routine to the stack of the called routine. | Understand | CO 5 | CLO17 | AEC021.17 |
| 14. | Define cache memory. | The memory that maintains the most frequently required data for execution, in a high speed | Remember | CO 5 | CLO18 | AEC021.18 |

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| | | memory is called cache memory. | | | | |
| 15. | What is local and global descriptor? | A descriptor table is an array of 8 KB descriptor. This means there may 8 KB descriptors are in a descriptor table. A Global Descriptor table contains | Understand | CO 5 | CLO18 | AEC021.18 |
| 16. | Define Interrupt Descriptor Table? | Interrupt descriptor table is used to store task gates, interrupt gates and trap gates. The IDT has a 24 bit base address and 16 bit limit register in the CPU. | Understand | CO 5 | CLO17 | AEC021.17 |
| 17. | What is privilege? | The privilege mechanism controls the access to descriptors and hence to the corresponding segments of the task. | Understand | CO 5 | CLO17 | AEC021.17 |
| 18. | Define descriptor cache? | To allow for fast accesses to segmented memory, the 80286 processor keeps a copy of each segment descriptor in a special descriptor cache. This saves the processor from accessing the GDT for every memory access made. | Understand | CO 5 | CLO17 | AEC021.18 |
| 19. | What is GDT? | The Global Descriptor Table or GDT is a data structure used by Intel x86- family processors starting with the 80286 in order to define the characteristics of the various memory areas used during program execution, including the base address, the size and access privileges like execute- ability and write-ability. | Understand | CO 5 | CLO17 | AEC021.17 |
| 20. | What is LDT? | There is also a Local Descriptor Table (LDT). While the LDT contains memory segments which are private to a specific program, the GDT contains global segments. | Understand | CO 5 | CLO17 | AEC021.17 |
| 21. | What is LLDT? | The instruction that loads a selector which refers to a local descriptor table, containing the base address and limit for LDT is LLDT | Understand | CO 5 | CLO17 | AEC021.17 |
| 22. | What happens when 80286 is reset? | When 80286 is reset, it always starts its execution in real addressing mode. | Understand | CO 5 | CLO17 | AEC021.17 |
| 23. | What is context switching? | This context switch may be initiated at fixed time intervals (pre-emptive multitasking),or the running program may be coded to signal to the supervisory software when it can be interrupted in multitasking. | Remember | CO 5 | CLO17 | AEC021.17 |

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| 24. | Which unit that is used for handling data, and calculates offset address? | The execution unit has eight general purpose and eight special purpose registers, which are either used for handling the data or calculating the offset addresses. | Understand | CO 5 | CLO19 | AEC021.19 |
| 25. | What is instruction pipelining? | The process of fetching the instructions in advance and storing in the queue is called instruction pipelining. | Remember | CO 5 | CLO18 | AEC021.18 |
| 26. | What is the advantage of pages in paging? | The advantage of paging scheme is that the complete segment of a task need not be in the physical memory at any time. Only a few pages of the segments, which are required currently for the execution, need to be available in the physical memory. | Understand | CO 5 | CLO17 | AEC021.17 |
| 27. | What is page table cache? | The storage of 32 recently accessed page table entries to optimize the time, is known as page table cache. | Understand | CO 5 | CLO17 | AEC021.17 |
| 28. | Which test register(s) that is provided by 80386 for page caching? | Two test registers are provided by 80386 for page caching, namely test control and test status registers. | Remember | CO 5 | CLO18 | AEC021.18 |
| 29. | Which flag bits that indicate the privilege level of current IO operations | The IOPL flag bits indicate the privilege level of current IO operations. | Remember | CO 5 | CLO17 | AEC021.17 |
| 30. | Define integer data type? | The representation of 8-bit or 16-bit signed binary operands using 2's complement is integer data type. | Understand | CO 5 | CLO17 | AEC021.17 |
| 31. | What is LGDT? | The LGDT (load global descriptor table register) loads 6 bytes from a memory block, pointed to by the effective address of the operand, into global descriptor table register. | Remember | CO 5 | CLO17 | AEC021.17 |
| 32. | Define virtual memory. | To the user, there exists a very large logical memory space, which is actually not available called virtual memory. This does not exist physically in a system. It is however, possible to map a large virtual memory space onto the real physical memory. | Understand | CO 5 | CLO17 | AEC021.17 |
| 33. | What are the features of 80286? | • The 80286 microprocessor is an advanced version of the 8086 microprocessor that is designed for multi user and multitasking environments<br>• The 80286 addresses 16 M Byte of physical memory and 1G Bytes of virtual memory by using its memory-management | Understand | CO 5 | CLO17 | AEC021.17 |

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| | | system | | | | |
| 34. | What are the features of 80386? | • The 80386 also includes 32-bit extended registers and a 32-bit address and data bus.<br>• The 80386 is operated in the pipelined mode, it sends the address of the next instruction or memory data to the memory system prior to completing the execution of the current instruction | Remember | CO 5 | CLO18 | AEC021.18 |
| 35. | What are the features of 80486? | • The 80486 microprocessor is an improved version of the 80386 microprocessor that contains an 8K-byte cache and an 80387 arithmetic co processor;<br>• A new feature found in the 80486 in the BIST (builtin self-test) that tests the microprocessor, coprocessor, and cache at reset time | Remember | CO 5 | CLO19 | AEC021.19 |
| 36. | Define multitasking? | Multitasking refers to the simultaneously performance of multiple tasks and processes by hardware, software or any computing appliance. It enables the performance of more than one computer process at the same time with minimal lag in overall performance and without affecting the operations of each task. | Understand | CO 5 | CLO17 | AEC021.17 |
| 37. | List out the Register organization of 80286? | The 80286 CPU contains almost the same set of registers, as in 8086, viz.<br>(a) Eight 16-bit general purpose registers<br>(b) Four 16-bit segment registers<br>(c) Status and control register<br>(d) Instruction pointer. | Remember | CO 5 | CLO17 | AEC021.17 |
| 38. | Give the Signal Descriptions of 80386 | • $CLK_2$ :The input pin provides the basic system clock timing for the operation of 80386.<br>• $D_0 - D_{31}$:These 32 lines act as bidirectional data bus during different access cycles.<br>• $A_{31} - A_2$: These are upper 30 bit of the 32- bit address bus.<br>• $BE_0$ to $BE_3$: The 32- bit data bus supported by 80386 and the memory system of 80386 can be viewed as a 4- byte wide memory access mechanism. The 4 byte enable lines $BE_0$ to $BE_3$, may be used for enabling these | Remember | CO 5 | CLO18 | AEC021.18 |

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| | | 4 blanks. Using these 4 enable signal lines, the CPU may transfer 1 byte / 2 / 3 / 4 byte of data simultaneously. | | | | |
| 39. | List out Register Organization of 80386? | • The 80386 has eight 32 - bit general purpose registers which may be used as either 8 bit or 16 bit registers.<br>• A 32 - bit register known as an extended register, is represented by the register name with prefix E.<br>• Example : A 32 bit register corresponding to AX is EAX, similarly BX is EBX etc.<br>• The 16 bit registers BP, SP, SI and DI in 8086 are now available with their extended size of 32 bit and are names as EBP,ESP,ESI and EDI.<br>• AX represents the lower 16 bit of the 32 bit register EAX.<br>• BP, SP, SI, DI represents the lower 16 bit of their 32 bit counterparts, and can be used as independent 16 bit registers. | Understand | CO 5 | CLO18 | AEC021.18 |

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