INSTITUTE OF AERONAUTICAL ENGINEERING

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ELECTRONICS AND COMMUNICATION ENGINEERING

DEFINITIONS AND TERMINOLOGY QUESTION BANK

Course Name	:	VLSI DESIGN
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OBJECTIVES:

I	Have skills to use concepts of MOS devices for the fabrication of integrated chips (IC's).
II	Familiarize CMOS layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
III	Demonstrate the ability to design static CMOS combinational and sequential logic at the transistor level, including mask layout.
IV	Focus in selecting appropriate building blocks of data path for given system.

DEFINITIONS AND TERMINOLOGY QUESTION BANK

S.No	QUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
UNIT-I						
1	What is depletion mode?	In this MOSFET device is normally ON at zero gate–source voltage.	Understand	CO 1	CLO 1	AEC017.01
2	What is enhancement mode?	These devices are off at zero gate–source voltage, NMOS can be turned on by pulling the gate voltage higher than the source voltage, PMOS can be turned on by pulling the gate voltage lower than the source voltage.	Understand	CO 1	CLO 1	AEC017.01
3	What are the applications of MOSFET?	All digital and Analog circuits	Understand	CO 1	CLO 1	AEC017.01
4	How MOSFET is better than BJT?	MOSFETs are better in terms of power consumption. As the supply voltage is less in MOSFETs when compared to BJTs, power consumption is also very less.	Understand	CO 1	CLO 1	AEC017.01

S.No	QUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
5	What is pinch off?	Pinch off voltage is the drain to source voltage after which the drain to source current becomes almost constant and MOSFET enters into saturation region and is defined only when gate to source voltage is zero.	Understand	CO 1	CLO 1	AEC017.01
6	What is latch up?	Latch up is defined as the generation of a low-impedance path in CMOS between the power supply (VDD) and the ground (GND) due to the interaction of parasitic PNP and NPN bipolar junction transistors (BJTs).	Understand	CO 1	CLO 2	AEC017.02
7	What is body effect?	Body effect refers to the change in the transistor threshold voltage (VT) resulting from a voltage difference between the transistor source and body.	Remember	CO 1	CLO 2	AEC017.02
8	What is triode region?	The triode region is the operating region where the inversion region exists and current flows, but this region has begun to taper near the source.	Remember	CO 1	CLO 1	AEC017.01
9	What do u mean by cut-off region?	It is a region in which transistor remains OFF and needed some threshold voltage to operate or to move	Remember	CO 1	CLO 1	AEC017.01
10	What is linear region in MOS transistor?	There "linear" can mean "roughly linear current with applied voltage", which also means the MOSFET is acting like a resistor as opposed to more like a current source.	Understand	CO 1	CLO 1	AEC017.01
11	Define sub-threshold voltage	The supply voltage which is less than threshold voltage is called sub-threshold voltage	Understand	CO 1	CLO 2	AEC017.02
12	Define sub-threshold region	The region of operation of a MOSFET below its threshold voltage is called sub threshold region. It is also known as weak inversion region	Understand	CO 1	CLO 2	AEC017.02
13	Define super threshold region	The region of operation of a MOSFET above its threshold voltage is called super threshold region. It is also known as strong inversion region	Understand	CO 1	CLO 2	AEC017.02
14	List out Short channel effects of MOSFET	1 Threshold voltage roll off 2 Sub-threshold current 3 Drain induced barrier lowering (DIBL) 4 Hot carrier effect 5 Impact Ionization	Understand	CO 1	CLO 3	AEC017.03

S.No	QUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
		6 Velocity saturation 7 Gate Induced Drain Leakage (GIDL)				
15	Define threshold voltage?	The voltage at which the conduction starts is called threshold voltage.	Understand	CO 1	CLO 2	AEC017.02
16	What is Drain induced barrier lowering	Drain-induced barrier lowering (DIBL) is a short-channel effect in MOSFETs referring originally to a reduction of threshold voltage of the transistor at higher drain voltages.	Understand	CO 1	CLO 3	AEC017.03
17	What is GIDL	Gate-induced drain leakage, GIDL is induced by band-to-band tunneling effect in strong accumulation mode and generated in the gate-to-drain overlap region.	Understand	CO 1	CLO 3	AEC017.03
18	What is Hot carrier effect	Hot carrier injection in MOSFETs occurs when a carrier from Si channel is injected into the gate oxide.	Understand	CO 1	CLO 1	AEC017.01
19	Why does tunneling occur in MOSFET?	Due to doping in poly silicate insulators (which are heavily doped mostly) used in gate of MOSFET tunnel effect occurs from gate to channel / source / drain in forward bias and between gate to source / drain in reverse bias.	Understand	CO 1	CLO 1	AEC017.01
20	What is Sub-threshold current	An effect that is exacerbated by short channel designs is the sub-threshold current which arises from the fact that some electrons are induced in the channel even before strong inversion is established. For the low electron concentration (typically of sub-threshold regime), we expect diffusion current (proportional to carrier gradients) to dominate over drift currents (proportional to carrier concentrations). For very short channel lengths, such carrier diffusion from source to drain can make it impossible to turn off the device below threshold. The sub-threshold current is made worse by the DIBL effect which increases the injection of electrons from the source.	Understand	CO 1	CLO 2	AEC017.02
21	How mobility degradation occurs in MOSFET?	Lateral Field Effect: In case of short channels, as the lateral field is increased, the channel mobility becomes field-dependent and eventually velocity saturation occurs.	Understand	CO 1	CLO 3	AEC017.03

S.No	QUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
		This results in current saturation. Vertical Field Effect: As the vertical electric field also increases on shrinking the channel lengths, it results in scattering of carriers near the surface. Hence the surface mobility reduces. Thus for short channels, the mobility degradation which occurs due to velocity saturation and scattering of carriers.				
22	What is V_T roll off?	The variations in threshold voltage with respect to channel length in short channel devices is VT roll off	Understand	CO 1	CLO 3	AEC017.03
23	What is Drain punch through	When the drain is at high enough voltage with respect to the source, the depletion region around the drain may extend to the source, causing current to flow irrespective of gate voltage (i.e. even if gate voltage is zero). This is known as Drain Punch Through condition	Remember	CO 1	CLO 3	AEC017.03
24	What is aspect ratio	The ratio of width to length (W/L) in a MOSFET is called aspect ratio or β ratio or transistor ratio	Remember	CO 1	CLO 1	AEC017.01
25	Write down drain current equation of NMOS in linear region of operation	$I_D = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$ $for\ V_{GS} > V_T, V_{DS} \le V_{GS} - V_T$	Remember	CO 1	CLO 1	AEC017.01
26	What is channel length modulation	Channel length modulation (CLM) is a shortening of the length of the inverted channel region with increase in drain bias for large drain biases.	Remember	CO 1	CLO 1	AEC017.01
27	What is leakage current?	The current in a MOSFET when the MOSFET is in OFF state. It is also known as static current / OFF current	Understand	CO 1	CLO 1	AEC017.01
28	State Moore's law	The number of transistors per square inch on integrated circuits had doubled every year since the integrated circuit was invented.	Remember	CO 1	CLO 1	AEC017.01
29	Why Moore's law is ending?	Moore's law is ending due to continually shrinking of the size of components on a chip (due to technology scaling)	Remember	CO 1	CLO 1	AEC017.01
30	What is Tick Tock model?	In technology terms, tick-tock typically refers to Intel's model of releasing new processor families each year, with the "tick" applying	Remember	CO 1	CLO 1	AEC017.01

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		to processors fabricated on a smaller die shrink and the "tock" representing processors that is based on a new processor micro-architecture. The "tick" processors feature enhanced performance and energy efficiency on a smaller, more refined silicon chip, while the "tock" processors typically optimize the value of the increased number of transistors available from the "tick" release and also integrate the latest technology updates available.				
31	What is technology scaling	Technology scaling is reduction of the lateral and vertical dimensions of transistors. The supply voltage (VDD) is scaled down to reduce power dissipation and to maintain device reliability.	Understand	CO 1	CLO 3	AEC017.03
32	What is ITRS?	The International Technology Roadmap for Semiconductors	Remember	CO 1	CLO 1	AEC017.01
33	What is the impact of down scaling the MOSFET on power dissipation?	Power reduces	Understand	CO 1	CLO 2	AEC017.01
34	What is the impact of down scaling the MOSFET on propagation delay?	Propagation delay increases	Understand	CO 1	CLO 2	AEC017.01
35	What is the impact of down scaling the MOSFET on area?	Area reduces	Understand	CO 1	CLO 3	AEC017.03
36	What is velocity saturation?	Saturation velocity is the maximum velocity a charge carrier in a semiconductor, generally an electron, attains in the presence of very high electric fields. When this happens, the semiconductor is said to be in a state of velocity saturation	Understand	CO 1	CLO 3	AEC017.03
37	What is Bi-CMOS technology?	Bi-CMOS technology is a combination of Bipolar and CMOS technologies.	Remember	CO 1	CLO 1	AEC017.02
38	What is mobility?	Mobility is the measure of how quickly an electron can move through a metal or semiconductor in presence of electrical field.	Remember	CO 1	CLO 1	AEC017.01

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39	What is totem pole configuration?	Totem-pole output, also known as a push-pull output, is a type of electronic circuit and usually realized as a complementary pair of transistors. The High and Low level of the output are determined. The output of high level is 10 V max, low level is 0.5 V min.	Remember	CO 1	CLO 1	AEC017.02
UNIT-II						
1	Define dry oxidation process	Dry oxidation means, it is oxidized with oxygen. $Si + O_2 \rightarrow SiO_2$	Remember	CO 2	CLO 5	AEC017.05
2	Define wet oxidation process	Wet oxidation means the silicon is oxidized with stream or water vapor. $Si + 2H_2O \rightarrow SiO_2 + 2H_2$	Understand	CO 2	CLO 5	AEC017.05
3	What are the different oxidation processes?	1. Thermal oxidation 2. Electrochemical oxidation	Remember	CO 2	CLO 5	AEC017.05
4	What is masking?	Exposing photoresist through n-well mask is called masking	Remember	CO 2	CLO 1	AEC017.02
5	What is Chemical Vapor Deposition (CVD) process	Chemical vapor deposition (CVD) is a vacuum deposition method used to produce high quality, high-performance, solid materials. In typical CVD, the wafer (substrate) is exposed to one or more volatile precursors, which react and/or decompose on the substrate surface to produce the desired deposit.	Understand	CO 2	CLO 1	AEC017.01
6	What is diffusion	In fabrication processing, the term “diffusion” usually refers to the entire process of adding a dopant to the surface of wafer at high temperature.	Understand	CO 2	CLO 5	AEC017.05
7	What is oxide stripping	Stripping off the remaining oxidation layer is called oxide stripping	Remember	CO 2	CLO 5	AEC017.05
8	What is Metallization	Aluminum is sputtered on the whole wafer	Remember	CO 2	CLO 5	AEC017.05
9	What is sputtering	In physics, sputtering is a phenomenon in which microscopic particles of a solid material are ejected from its surface, after the material is itself bombarded by energetic particles of a plasma or gas.	Remember	CO 2	CLO 5	AEC017.05
10	What is etching?	Etching is used in microfabrication to chemically remove layers from the surface of a wafer during manufacturing. Etching is a critically important process	Remember	CO 2	CLO 5	AEC017.05

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		module, and every wafer undergoes many etching steps before it is complete.				
11	What is ion implantation	Ion implantation is a low-temperature process by which ions of one element are accelerated into a solid target, thereby changing the physical, chemical, or electrical properties of the target.	Understand	CO 2	CLO 5	AEC017.05
12	What is Twin Well/Tub Technology	The process of creating both a p-well and an n-well for the n-MOSFET's and p-MOSFET respectively is twin well or twin tub technology. Such a choice means that the process is independent of the dopant type of the starting substrate (provided it is only lightly doped).	Understand	CO 2	CLO 5	AEC017.05
13	What is lithography?	Lithography is the process of transferring circuit pattern directly on to the silicon wafer. But first, the designer must have designed the circuit, determined the size of various circuit elements down to transistor bases to lead width, and their exact positions on the chip.	Understand	CO 2	CLO 5	AEC017.05
14	What is SOI CMOS technology?	Silicon on insulator (SOI) CMOS technology refers to the use of a layered silicon–insulator–silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, especially microelectronics, to reduce parasitic device capacitance, thereby improving performance	Understand	CO 2	CLO 5	AEC017.05
15	What is the significance of SOI CMOS technology?	Latch up and body effect issues are solved in this technology by reducing parasitic capacitances.	Remember	CO 2	CLO 5	AEC017.05
16	What is voltage droop?	Voltage droop is the intentional loss in output voltage from a device as it drives a load.	Remember	CO 2	CLO 7	AEC017.07
17	What is ground bounce?	Ground bounce is usually seen on high density VLSI where insufficient precautions have been taken to supply a logic gate with a sufficiently low resistance connection (or sufficiently high capacitance) to ground.	Remember	CO 2	CLO 7	AEC017.07
18	Define noise margin in	Noise margin is the amount of noise that a CMOS	Understand	CO 2	CLO 7	AEC017.07

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	CMOS circuit?	circuit could withstand without compromising the operation of circuit				
19	Define propagation delay	Propagation delay is the difference in time (calculated at 50% of input-output transition), when output switches, after application of input.	Remember	CO 2	CLO 7	AEC017.07
20	Define power consumption	power consumption refers to the electrical energy per unit time	Remember	CO 2	CLO 7	AEC017.07
21	What are the components of power	1. Dynamic / Switching power 2. Static / leakage power 3. Short circuit Power	Remember	CO 2	CLO 7	AEC017.07
22	What is PTL (Pass transistor logic) ?	Pass transistor logic describes one of the several logic families in CMOS. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors.	Understand	CO 2	CLO 8	AEC017.08
23	What is the output voltage in PTL (Pass transistor logic) device?	$Vout = V_{DD} - V_T$	Understand	CO 2	CLO 5	AEC017.05
24	How to overcome voltage drop in PTL device	By using level restorer transistors	Understand	CO 2	CLO 5	AEC017.05
25	What is NBTI in CMOS?	Negative-bias temperature instability (NBTI) is a key reliability issue in MOSFETs. NBTI manifests as an increase in the threshold voltage and consequent decrease in drain current and transconductance of a MOSFET. The degradation is often approximated by a power-law dependence on time. It is of immediate concern in p-channel MOS devices (pMOS), since they almost always operate with negative gate-to-source voltage; however, the very same mechanism also affects nMOS transistors when biased in the accumulation regime, i.e. with a negative bias applied to the gate.	Remember	CO 2	CLO 7	AEC017.07
26	What are the advantages of PTL	Low Power Less Propagation delay Low PDP Low EDP	Understand	CO 2	CLO 7	AEC017.07
27	What are different	1.Intrinsic gate capacitance 2.overlap capacitance.	Remember	CO 2	CLO 7	AEC017.07

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	components in gate capacitance?					
28	Define diffusion capacitance?	The parasitic capacitance arise from reverse biased p-n junction are called as diffusion capacitance.	Remember	CO 2	CLO 7	AEC017.07
29	Define self-aligning?	Polysilicon with underlying thin oxide and the thick oxide act as mask during diffusion – the process is self-aligning	Remember	CO 2	CLO 5	AEC017.05
30	How latch up problem is avoided?	Latch up problem can be reduced by using a low-resistivity epitaxial P-Substrate as the starting material which act as very low resistance .	Remember	CO 2	CLO 5	AEC017.05
31	What is the purpose of the N buried layer?	The **function** of this **layer** is to reduce the collector resistance of the transistor.	Understand	CO 2	CLO 5	AEC017.05
32	What is pull down device?	A device connected so as to pull the output voltage to the lower supply voltage usually 0V is called pull down device.	Understand	CO 2	CLO 8	AEC017.08
33	What is pull up device?	A device connected so as to pull the output voltage to the upper supply voltage usually VDD is called pull up device.	Remember	CO 2	CLO 8	AEC017.08
34	Why NMOS technology is preferred more than PMOS technology?	N- channel transistors has greater switching speed when compared tp PMOS transistors.	Remember	CO 2	CLO 8	AEC017.08
35	What are the different operating regions foe an MOS transistor	Cutoff region Non- Saturated Region Saturated Region	Remember	CO 2	CLO 5	AEC017.05
36	Define Short Channel devices?	Transistors with Channel length less than 3- 5 microns are termed as Short channel devices. With short channel devices the ratio between the lateral & vertical dimensions are reduced.	Remember	CO 2	CLO 8	AEC017.08
37	What are the advantages of CMOS process?	Low power Dissipation High Packing density Bi directional capability	Understand	CO 2	CLO 7	AEC017.07
38	What are the basic processing steps involved in Bi-CMOS process?	Additional masks defining P base region N Collector area Buried Sub collector (SCCD) Processing steps in CMOS process	Understand	CO 2	CLO 5	AEC017.05
39	What are the steps involved in twin-tub process?	Tub Formation, Thin-oxide Construction Source & Drain Implantation, Contact cut definition, Metallization.	Remember	CO 2	CLO 5	AEC017.05

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40	What are the advantages of Silicon-on-Insulator process?	No Latch-up, Due to absence of bulks transistor structures are denser than bulk silicon.	Remember	CO 2	CLO 5	AEC017.05
UNIT-III						
1	What are the basic layers of MOS circuits?	MOS circuits formed by four basic layers n-diffusion, p-diffusion, polysilicon and metal.	Remember	CO 3	CLO 10	AEC017.10
2	Define Stick Diagram?	It is used to convey information through the use of color code. Also it is the cartoon of a chip layout.	Remember	CO 3	CLO 10	AEC017.10
3	What are the uses of Stick diagram?	It can be drawn much easier and faster than a complex layout. These are especially important tools for layout built from large cells	Understand	CO 3	CLO 10	AEC017.10
4	Give the various color coding used in stick diagram?	Green – n-diffusion , Red-polysilicon, Blue –metal, Yellow- implant, Black-contact areas.	Remember	CO 3	CLO 10	AEC017.10
5	What is the aim of Circuit designers in IC design?	Circuit designers in general prefer tighter, smaller layouts for improved performance and decreased silicon area.	Understand	CO 3	CLO 11	AEC017.11
6	What is the aim of Process engineers with respect to design rules?	Process engineers wants design rules which are controllable and reproducible process.	Understand	CO 3	CLO 11	AEC017.11
7	What are Lambda-based design rules?	Design rules specify line widths, separations and extensions in terms of lambda.	Understand	CO 3	CLO 11	AEC017.11
8	What is the width and spacing between two diffusion layers?	The width of n-diffusion and p-diffusion should be 2λ, the spacing between two diffusion layers should be 3λ according to design rules.	Understand	CO 3	CLO 11	AEC017.11
9	What is the layer used to separate each transistor layer?	Each and every layer is isolated by thick or thin silicon dioxide insulating layers.	Understand	CO 3	CLO 10	AEC017.10
10	Define Butting contacts	The gate and source of a depletion device can be connected by a method known as butting contact. Here metal makes contact to both the diffusion forming the source of the depletion transistor and to the poly silicon forming this device's gate.	Remember	CO 3	CLO 10	AEC017.10
11	What is the width and spacing between two metal	The width of the metal 1 layer should be 3λ and metal 2 should be 4λ, spacing between two metal 1 layers should be	Understand	CO 3	CLO 11	AEC017.11

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	layers?	3λ and spacing between two metal 2 should be 4λ,				
12	What is the design rule for implant	Implant for a n-mos depletion mode transistor should extend minimum of 2λ from the channel in all the directions.	Remember	CO 3	CLO 11	AEC017.11
13	Which type of contact cuts is better?	Buried contacts are much better than butted contacts. In butted contacts the two layers are joined together or binded together using adhesive type of material where as in buried contact one layer is interconnected or fitted into another.	Understand	CO 3	CLO 11	AEC017.11
14	Define Buried contacts	The buried contact is a method to make direct ohmic contact between the polysilicon gate material and the junctions, in silicon-gate integrated circuits.	Remember	CO 3	CLO 11	AEC017.11
15	Define hard failures in bathtub curve?	It means permanent functional failures of the chip	Remember	CO 3	CLO 13	AEC017.13
16	Which is more complex process in butting?	Butting contact is complex process whereas buried contact is simple process because butting contact should be done more carefully to serve well and be strong.	Understand	CO 3	CLO 11	AEC017.11
17	Define transient failures?	Transient failures can come bit flips and timing errors.	Remember	CO 3	CLO 13	AEC017.13
18	Which layer is used for power and signal lines?	Metal layers are used for power and signal lines as metals has good thermal and electrical conductivity.	Remember	CO 3	CLO 10	AEC017.10
19	What is the Minimum n-well width should be in micro meter?	The minimum width of n-well is 3 micro meter because n-well should be with little thickness and in it p-type devices are formed.	Remember	CO 3	CLO 11	AEC017.11
20	What is the Minimum spacing between two n-well	The minimum spacing between two n-well is 8.5 micro meter according to the lambda based design rules.	Remember	CO 3	CLO 11	AEC017.11
21	What are the advantages of design rules?	Design rules are those are durable, scalable, portable, increases designer efficiency and automatic translation to final layout can be done.	Understand	CO 3	CLO 11	AEC017.11
22	Which color is used for polysilicon,polysilicon2?	Red is used to represent polysilicon layers, Orange color is used to represent polysilicon-2 layer	Understand	CO 3	CLO 10	AEC017.10
23	Define metallization failure	Defect that occurs due to Scratches and voids, mechanical damage, non-	Remember	CO 3	CLO 13	AEC017.13

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	mechanism	ohmic contacts, step coverage, weak adhesion, improper thickness, corrosion, electromigration, stress migration.				
24	How to represent implant?	Implant is represented using yellow color dotted lines. It is drawn in the middle of the nMOS or pMOS where ever the implant is used.	Remember	CO 3	CLO 11	AEC017.11
25	Define electrical contact in stick diagram?	When two or more sticks of same type cross or touch each other, then that forms a contact called electrical contact.	Remember	CO 3	CLO 10	AEC017.10
26	What is the effect of Interconnect on MOS devices ?	Interconnect increases circuit delay for two reasons. First, the wire capacitance adds loading to each gate. Second, long wires have significant resistance that contributes distributed RC delay or *flight time*. wire delay grows quadratically with length.	Remember	CO 3	CLO 12	AEC017.12
27	Define crosstalk effect of wires?	wires have capacitance to their adjacent neighbors as well as to ground. when wire *A* switches, it tends to bring its neighbor *B* along with it on account of capacitive coupling, also called *crosstalk*.	Understand	CO 3	CLO 12	AEC017.12
28	Define infant mortality?	Chip failures that are caused by a variety of fabrication flaws that create marginal structures such as thin wires or malformed transistors.	Remember	CO 3	CLO 13	AEC017.13
29	Define mean time to failure (MTTF).	This metric defines the mean time to the next occurrence of a given failure mechanism. Based on MTTF, we can determine other interesting metrics, such as **lifetime**.	Remember	CO 3	CLO 13	AEC017.13
30	Define diffusion and junctions failures?	Crystal defects, impurity precipitation, mask misalignment, surface contamination.	Remember	CO 3	CLO 13	AEC017.12
31	Define passivation failure ?	Failure that occurs due to Pinholes and cracks, thickness variations, contamination, surface inversion	Understand	CO 3	CLO 13	AEC017.13
32	Define Time-dependent	*TDDB* Time-dependent dielectric breakdown	Understand	CO 3	CLO 13	AEC017.13

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	dielectric breakdown	occurs because the electric fields across gate oxides induce stresses that damage the oxide.				
33	Define hot carrier	It is a carrier that gains enough energy to jump from the silicon substrate into the gate oxide. As these hot carriers accumulate, they create a space charge in the oxide that affects the transistor's threshold voltage and other parameters	Remember	CO 3	CLO 13	AEC017.13
34	Define Negative bias temperature instability	It refers to shifts in Vth/g_m of pMOS devices due to stress that introduces interface states and space charge.	Remember	CO 3	CLO 13	AEC017.13
35	Define failure mechanism occurs in oxides?	It is due to Mobile ions, pinholes, interface states, hot carriers, time dependent dielectric breakdown.	Remember	CO 3	CLO 13	AEC017.13
36	Define Electromigration	Electrons drifting through the voltage gradient on a metal line collide with the metal grains. Under high currents, electron collisions with metal grains cause the metal to move; this process is called metal migration (also known as electromigration).	Understand	CO 3	CLO 13	AEC017.13
37	Define stress migration	Stress migration is caused by mechanical stress and can occur even when no current flows through the wire. These stresses are caused by the different thermal expansion coefficients of the wires and the materials in which they reside	Remember	CO 3	CLO 13	AEC017.13
38	Define soft errors in VLSI	Soft errors cause memory cells to change state. Soft errors can be caused by alpha particles that generate excess carriers as they travel through the substrate.	Understand	CO 3	CLO 13	AEC017.13
39	Define Latch-up in CMOS ?	Latch-up is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between V_{DD} and V_{ss}	Remember	CO 3	CLO 13	AEC017.13
40	Define via contact?	It is the contact between metal 1 and metal 2.	Remember	CO 3	CLO 11	AEC017.11
UNIT-IV						
1	What is static CMOS logic?	Static CMOS logic is a combination of two networks ,Pull up Network using PMOS transistors and Pull down network using NMOS transistors. They are dual with	Remember	CO 4	CLO 19	AEC017.19

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		each other.At any time ,any one of the network is on				
2	What is dynamic CMOS logic?	Dynamic circuits reduce the drawbacks of ratioed circuits using a clock input to the pull up transistor(PMOS).It requires N+2 transistors and there are two modes of operation ,Pre-charge and Evaluation	Understand	CO 4	CLO 19	AEC017.19
3	What are the disadvantages of dynamic logic?	• Consume significant dynamic power • Sensitive to noise during evaluation • Carefull clocking • Monotonicity problem	Remember	CO 4	CLO 19	AEC017.19
4	Why domino logic is preferred over dynamic logic?	In dynamic logic ,there is cascading problem. This can be solved by placing a static – CMOS inverter between dynamic gates. The dynamic –static pair together is called domino logic.	Understand	CO 4	CLO 19	AEC017.19
5	Define propagation delay	The propagation delay is the time taken to change the output after applying the input. This is the upper bound on interval between valid inputs and valid outputs.	Remember	CO 4	CLO 15	AEC017.15
6	What **is** the cause of static power dissipation?	Static dissipation is due to sub threshold conduction through off transistor.	Understand	CO 4	CLO 19	AEC017.19
7	State any two criteria for low power logic design	The low power can be achieved by lowering the effective capacitance. The non active modules can be made to stand by mode to reduce the power.	Remember	CO 4	CLO 21	AEC017.21
8	What is transmission gate?	Transmission gate is constructed by combining an NMOS transistor and PMOS transistor in parallel. It acts as a switch that turns on when a '1' is applied to the gate 'A'. When A=1,'0'and '1'can be passed strongly through IN	Understand	CO 4	CLO 14	AEC017.14
9	What is pass transistor logic?	This type of logic uses NMOS transistors alone. In this gate is driven by a control signal ,the source (out), the drain of the transistor is called constant or variable voltage potential (in) when the control signal is high, the input is passed to the output	Remember	CO 4	CLO 14	AEC017.14

S.No	QUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
		and when the control signal is low, the output is floating such topology circuit is called pass transistor.				
10	Why single phase dynamic logic structure cannot be cascaded? Justify	In cascading problem arises because the output of each gate are pre-charged to '1' and due to finite propagation delay Due to this, some charge will be loss and leads to reduced noise margin and potential malfunctioning	Understand	CO 4	CLO 19	AEC017.19
11	Write the design style classification of Semi custom design ASICs	Standard cell design Gate array design : Channelled Gate Array Channel less Gate Array	Remember	CO 4	CLO 17	AEC017.17
12	Write the design style classification of Programmable ASICs	PLDs, FPGA	Understand	CO 4	CLO 17	AEC017.17
13	What are the two types of ASICs?	Full Custom ASICs Semi custom ASICs	Remember	CO 4	CLO 17	AEC017.17
14	What are the different types of programming structure available in PAL?	Programming Techniques of PAL are 1. Fusible Links programming 2. UV-Erasable EPROM programming 3. EEPROM programming	Understand	CO 4	CLO 17	AEC017.17
15	What are the features of standard cell ASICs?	All mask layers are customized- transistors and interconnect. Custom blocks can be embedded. Manufacturing lead time is about eight weeks.	Remember	CO 4	CLO 17	AEC017.17
16	Define Total wire capacitance?	It is defined as the sum of area capacitance and fringing field capacitance.	Understand	CO 4	CLO 15	AEC017.15
17	How the Interlayer capacitance occurs	Interlayer capacitance occurs due to parallel plate effect between one layer and another. When one capacitance value comes closer to another they create some combined effects.	Understand	CO 4	CLO 15	AEC017.15
18	What are the characteristics of FPGA?	• None of the mask layers are customized. • .A method for programming the basic logic cells and the interconnect. • This is used to implement combinational as well as sequential	Remember	CO 4	CLO 17	AEC017.17

S.No	QUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
		logic (flip-flops).				
19	What is programmable logic array?	A programmable logic array (PLA) is a programmable device used to implement combinational logic circuits. The PLA has a set of programmable AND planes, which link to a set of programmable OR planes.	Understand	CO 4	CLO 17	AEC017.17
20	What is mean by Programmable logic plane?	The Programmable logic plane is programmable read -only memory (PROM) array that allows the signals present on the devices pins (or the logical components of those signals) to be routed to an output logic macro cell	Remember	CO 4	CLO 17	AEC017.17
21	How the switch logic is designed?	Switch logic is designed using n or p pass transistors or from complementary switches.	Understand	CO 4	CLO 14	AEC017.14
22	List the steps in ASIC design flow	Design entry. Enter the design into an ASIC design system, either using a hardware description language (HDL) or schematic entry. Logic synthesis. Use an HDL (VHDL or Verilog) and a logic synthesis tool to produce a net list.	Understand	CO 4	CLO 17	AEC017.17
23	Define Fall time	Fall time, τf is the time taken for a waveform to fall from 90% to 10% of its steady state value.	Remember	CO 4	CLO 15	AEC017.15
24	Define Delay time	Delay time, τd is the time difference between input transition (50%) and the 50%output level. This is the time taken for a logic transition to pass from input to output.	Understand	CO 4	CLO 15	AEC017.15
25	What are two components of power dissipation?	These are: i) Static dissipation due to leakage current or other current drawn continuously from the power supply. ii) Dynamic dissipation due to - Switching transient current - Charging and discharging of load capacitances.	Remember	CO 4	CLO 19	AEC017.19
26	What is the full custom ASIC design?	In a full custom ASIC, an engineer designs some or all of the logic cells, circuits or layout specifically for one ASIC.	Understand	CO 4	CLO 17	AEC017.17
27	What is the standard cell-based ASIC design?	A cell-based ASIC (CBIC) uses predesigned logic cells known as standard cells.. The ASIC designer defines only the placement of standard cells and the interconnect in a	Understand	CO 4	CLO 17	AEC017.17

S.No	QUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
		CBIC. All the mask layers of a CBIC are customized and are unique to a particular customer.				
28	Differentiate between channeled & channel less gate array.	In Channeled Gate Array only the interconnect is customized but in channelless Gate Array only the top few mask layers customized.	Understand	CO 4	CLO 17	AEC017.17
29	Give the constituent of I/O cell in 22V10.	2V10 I/O cell consists of a register ,output 4:1 mux, a tri-state buffer,a 2:1 input mux.	Remember	CO 4	CLO 17	AEC017.17
30	What are the different methods of programming of PALs?	The programming of PALs is done in three main ways:• Fusible links • UV – erasable EPROM • EEPROM (E2PROM) – Electrically Erasable Programmable ROM	Understand	CO 4	CLO 17	AEC017.17
31	What are Programmable Interconnects ?	In a PAL, the device is programmed by changing the characteristics if the switching element. An alternative would be to program the routing.	Understand	CO 4	CLO 17	AEC017.17
32	What is the advantage of switch logic?	The switch logic approach takes no static current from the supply rails and is faster for small arrays.	Understand	CO 4	CLO 14	AEC017.14
33	Define Gate logic?	Gate logic is also called as restoring logic. This is a logic circuitry designed so that even with an imperfect input pulse a standard output occurs at the exit of each successive logic gate.	Understand	CO 4	CLO 14	AEC017.14
34	What is the pull up and pull down impedance ratio is pseudo nMOS design ?	For a pseudo nMOS design, the ratio of Zp.u. and Zp.d. is 3:1.	Understand	CO 4	CLO 14	AEC017.14
35	In which region Pseudo-nMOS logic operates?	In Pseudo-nMOS logic, n transistor operates in saturation region and p transistor operates in resistive region.	Understand	CO 4	CLO 14	AEC017.14
36	What are the features of switch logic approach	Some of the features of switch logic approach are that it occupies more area, eliminates undesirable threshold voltage and has low power dissipation.	Understand	CO 4	CLO 14	AEC017.14
37	Which contribute to the wiring capacitance?	The sources of capacitances which contribute to the total wiring capacitance are fringing field capacitance, interlayer capacitance and peripheral capacitance.	Remember	CO 4	CLO 15	AEC017.15
38	Which capacitance must be higher?	Metal to polysilicon capacitance should be higher than metal to substrate	Remember	CO 4	CLO 15	AEC017.15

S.No	QUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
		capacitance. This is due to that when one layer underlies the other and inconsequence interlayer capacitance is highly dependent on layout.				
UNIT-V						
1	What is parallel adder?	A parallel adder is an arithmetic combinational logic circuit that is used to add more than one bit of data simultaneously.	Remember	CO5	CLO 19	AEC017.19
2	What is memory cell?	The memory cell is an electronic circuit that stores one bit of binary information and it must be set to store a logic 1 (high voltage level) and reset to store a logic 0 (low voltage level). Its value is maintained/stored until it is changed by the set/reset process.	Understand	CO5	CLO 19	AEC017.19
3	What is ROM?	ROM is a type of memory that normally can only be read, as opposed to RAM which can be both read and written	Remember	CO5	CLO 19	AEC017.19
4	What is PROM?	This is a type of ROM that can be programmed using special equipment; it can be written to, but only once.	Understand	CO5	CLO 19	AEC017.19
5	What is Synchronous DRAM?	An asynchronous DRAM chip has power connections, some number of address inputs (typically 12), and a few (typically one or four) bidirectional data lines.	Remember	CO5	CLO 19	AEC017.19
6	What is Synchronous DRAM?	An asynchronous DRAM chip has power connections, some number of address inputs (typically 12), and a few (typically one or four) bidirectional data lines.	Remember	CO5	CLO 20	AEC017.20
7	What is meant by BCD adder?	BCD adder A 4-bit binary adder that is capable of adding two 4-bit words having a BCD (binary-coded decimal) format	Understand	CO5	CLO 21	AEC017.21
8	Where is BCD used?	Binary-coded Decimal or BCD is a way of representing a decimal number as a string of bits suitable for use in electronic systems.	Remember	CO5	CLO 21	AEC017.21
9	What is a 4 bit parallel adder?	a combinational circuit which is used to add two N-bit binary numbers	Remember	CO5	CLO 21	AEC017.21
10	What is a in binary code?	A binary code represents text, computer processor instructions, or any other data using a two-symbol system.	Understand	CO5	CLO 21	AEC017.21

S.No	QUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
11	What is fast adder?	A carry-lookahead adder (CLA) or fast adder is a type of adder used in digital logic.	Remember	CO5	CLO 20	AEC017.20
12	What are universal shift registers?	A Universal shift register is a register which has both the right shift and left shift with parallel load capabilities. Universal shift registers are used as memory elements in computers.	Understand	CO5	CLO 20	AEC017.20
13	What is the difference between register and shift register?	Both shift registers and counters are made of flip-flops. A shift register is simply a chain of FFs where the Q output of one FF connects to the D input of the next. A shift register will transfer data from one FF to the next on each clock event	Understand	CO5	CLO 20	AEC017.20
14	What is a dynamic shift register?	A dynamic shift register circuit comprises an input terminal and an output terminal. The logic circuit is made operative by an output signal of the signal follower circuit and produces an inverter function at the output terminal, in response to an output signal of the second transfer gate circuit.	Remember	CO5	CLO 20	AEC017.20
15	Define Sequential circuits.	Sequential circuit has memory so output can vary based on input. This type of circuits uses previous input, output, clock and a memory element.	Understand	CO5	CLO 21	AEC017.21
16	What is EPROM?	An EPROM is a ROM that can be erased and reprogrammed	Remember	CO5	CLO 21	AEC017.21
17	What is EEPROM?	Electrically Erasable Programmable ROM	Understand	CO5	CLO 22	AEC017.22
18	What is DRAM?	Dynamic random-access memory	Remember	CO5	CLO 22	AEC017.22
19	Define decoder.	A decoder is a circuit that changes a code into a set of signals. It is called a decoder because it does the reverse of encoding, but we will begin our study of encoders and decoders with decoders because they are simpler to design.	Remember	CO5	CLO 22	AEC017.22
20	Define an encoder.	The n output lines generate the binary code for the possible 2n input lines. Let us take an example of an octal-to-binary encoder.	Understand	CO5	CLO 21	AEC017.21
21	Define priority encoder.	Binary Encoders generally have a number of inputs that must be mutually exclusive,	Understand	CO5	CLO 21	AEC017.21

S.No	QUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
		i.e. only one of the inputs can be active at any one time. The encoder then produces a binary code on the output pins, which changes in response to the input that has been activated.				
22	Define half adder.	Half adder is a combinational circuit, which performs the addition of two binary numbers A and B are of single bit. It produces two outputs sum, S & carry, C.	Understand	CO5	CLO 21	AEC017.21
23	What is binary adder?	The most basic arithmetic operation is addition. The circuit, which performs the addition of two binary numbers, is known as Binary adder.	Understand	CO5	CLO 19	AEC017.19
24	Define full adder.	Full adder is a combinational circuit, which performs the addition of three bits A, B and C_{in}. Where, A & B are the two parallel significant bits and C_{in} is the carry bit, which is generated from previous stage.	Understand	CO5	CLO 19	AEC017.19
25	Define multiplexer.	Multiplexer is a combinational circuit that has maximum of 2^n data inputs, 'n' selection lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines.	Understand	CO5	CLO 19	AEC017.19
26	Define Demultiplexer	De-Multiplexer is a combinational circuit that performs the reverse operation of Multiplexer. It has single input, 'n' selection lines and maximum of 2^n outputs. The input will be connected to one of these outputs based on the values of selection lines.	Remember	CO5	CLO 19	AEC017.19
27	Define comparator.	Digital Comparator. A magnitude digital comparator is a combinational circuit that compares two digital or binary numbers (consider A and B) and determines their relative magnitudes in order to find out whether one number is equal, less than or greater than the other digital number.	Remember	CO5	CLO 20	AEC017.20
28	What is code converter?	Codes and code converters Coding is the process of translating the input	Understand	CO5	CLO 21	AEC017.21

S.No	QUESTION	ANSWER	Blooms Level	CO	CLO	CLO Code
		information which can be understandable by the machine or a particular device. Coding can be used for security purpose to protect the information from steeling or interrupting.				
29	What is parallel adder?	A parallel adder is an arithmetic combinational logic circuit that is used to add more than one bit of data simultaneously.	Remember	CO5	CLO 21	AEC017.21
30	What is one-to-one mapping?	each input code word produces a different output code word	Remember	CO5	CLO 21	AEC017.21
31	What is binary decoder?	has an n-bit binary input code and a 1-out-of-2n output code	Understand	CO5	CLO 22	AEC017.22
32	What is binary encoder?	If the device's output code has fewer bits than the input code, the device is usually called an encoder	Remember	CO5	CLO 22	AEC017.22
33	What is multiplexer?	a digital switch—it connects data from one of n sources to its output	Remember	CO5	CLO 22	AEC017.22
34	What is comparator?	A circuit that compares two binary words and indicates whether they are equal is called a comparator	Understand	CO5	CLO 21	AEC017.21
35	What is ALU?	arithmetic logic unit (ALU) is a digital circuit used to perform arithmetic and logic operations	Remember	CO5	CLO 21	AEC017.21
36	What is Barrel shifter?	A barrel shifter is a digital circuit that can shift a data word by a specified number of bits without the use of any sequential logic, only pure combinational logic	Remember	CO5	CLO 19	AEC017.19
37	What is a counter?	Counts those pulses which are driven by a clock.	Understand	CO5	CLO 19	AEC017.19
38	What are the categories Counters?	(i) Asynchronous and Synchronous counters. (ii) Single and multi mode counters. (iii) Modulus counters.	Remember	CO5	CLO 19	AEC017.19
39	What is a multimode counter?	If the same counter circuit can be operated in both the UP and DOWN modes, it is called a multimode counters.	Remember	CO5	CLO 20	AEC017.20
40	What is a asynchronous counters?	Each flip flop is triggered by the previous flip flop.	Understand	CO5	CLO 22	AEC017.22

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