Code No: 09A50201 R09

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD**
**B. Tech III Year I Semester Examinations, May/June – 2013**
**IC Applications**
**(Common to EEE, ECE, ETM)**

**Time: 3 hours** **Max. Marks: 75**

**Answer any five questions**
**All questions carry equal marks**
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1.a) Write about the parameters that should be considered for ac and dc applications of operational amplifier.
b) What are the ideal characteristics of the operational amplifier and how do they differ practically?
c) Explain why open loop op-amp configurations are not used in linear applications. [4+6+5]

2.a) Discuss the operation of a FSK generator using 555 timer.
b) Write about the design aspects of IC 1496 balanced modulator. [7+8]

3.a) Explain about IGMF configuration in active filter design.
b) Distinguish between active and passive filters. [10+5]

4.a) Draw the functional diagram and connection diagram of sample and hold IC LF 398 and explain.
b) What are the applications of sample and hold circuit? [10+5]

5.a) Discuss about successive approximation converter with necessary diagrams.
b) Explain about ladder type DAC with neat diagram. [7+8]

6.a) Draw the functional block diagram of IC 555 timer and explain the significance of each block.
b) What are the applications of PLL? Explain any one of it in detail. [7+8]

7.a) Explain about TTL NAND gate with necessary diagrams.
b) Write about applications of TTL gate. [10+5]

8.a) Draw the logic diagram of J-K Flip-Flop and how to convert a J-K Flip-Flop to D Flip-Flop.
b) Explain the working of Decade counter using IC74XX. [7+8]

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R09

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**

**B. Tech III Year I Semester Examinations, November/December - 2012**

**IC APPLICATIONS**

**(Common to EEE, ECE, ETM)**

**Time: 3 hours** **Max. Marks: 75**

**Answer any five questions**

**All questions carry equal marks**

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1.a) List the reasons for differences in ideal and practical non-inverting Op-Amp amplifier.

b) Derive expressions for input and output impedances of a practical non-inverting Op-Amp amplifier.

c) Discuss how a voltage follower is built using an Op-Amp. [15]

2.a) What is the operation performed by an inverting Op-Amp amplifier if its feedback resistance is replaced by a capacitance? Explain the functioning of such circuit. What are the practical difficulties associated with this circuit?

b) What is the purpose of an n-channel MOSFET in a typical Op-Amp based sample and Hold Circuit? Explain through circuit operation and relevant waveforms.

c) Explain the operation of an Op-Amp astable multivibrator used as square wave generator. Suggest a method to restrict its output swing to predetermined values. [15]

3.a) List out the merits and demerits of active filters over passive filters.

b) Explain the functioning of any one RC type oscillator based on suitable circuit diagrams. What are the typical frequencies of oscillation? [7+8]

4.a) Discuss how a 555 timer can be used for FSK modulation, missing pulse detection, pulse width and pulse position modulation. State the mode of operation of 555 in each case.

b) What is the role played by a phase detector in the operation of a PLL? Explain through its block diagram. Define lock and capture ranges of a PLL. [7+8]

5.a) List the specifications and draw the pin configuration of IC 1408 DAC.

b) What is the significance of 'linearity' and 'conversion time' in an ADC?

c) Explain the operation of a weighted resistor type DAC. [15]

6.a) Why are tristated outputs and open collector outputs used in TTL ICs? List the advantages for both types of outputs.

b) List the differences between various logic family ICs under TTL family like 74 series, 74F series, 74 ALS series, 74 AS series ICs. [7+8]

7.a) Draw the pin diagram of 74 series decoder IC and explain its functioning. Explain how Boolean functions can be generated using decoders through an example.

b) List out the 74 series IC No.s for code converters to translate BCD-to-seven – segment display and BCD-to-gray scale. Draw pin diagrams. [7+8]

8. Design a 3-bit synchronous counter using JK flip-flops. [15]

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**III B.Tech I Semester Examinations,May/June 2012**
**IC APPLICATIONS**
**Common to Electronics And Telematics, Electronics And Communication Engineering, Electrical And Electronics Engineering**

**Time: 3 hours** **Max Marks: 75**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Discuss about stability of an OP-Amp.
   (b) Draw high frequency model of an OP-Amp and explain its working. [5+10]
2. (a) Compare R-2R and weighted resistor types of DACs.
   (b) Write short notes on A/D converters.
   (c) Define the following terms as related to DAC:
      i. Linearity
      ii. Resolution. [7+4+4]
3. (a) Explain the operation of limiters using Op-Amp.
   (b) Explain the characteristics of comparator and draw the circuit for comparator using Op-Amp. [10+5]
4. (a) Differentiate between the feedback networks of RC phase shift oscillator and Wein Bridge Oscillator.
   (b) List out the applications of Wein Birdge Oscillator. [10+5]
5. (a) Design a CMOS transistor circuit that has the functional behavior f (Z) =A.(B+C)
   (b) Design a 4-input CMOS AND-OR-INVERT gate. Draw the logic diagram and function table. [7+8]
6. (a) Write the specifications of NE555 timer IC.
   (b) Design a 555 timer circuit whose output frequency is 2 KHz when the trigger input signal frequency is 4 KHz.
   (c) In the 555 monostable multivibrator circuit if $R_A = 10$ kΩ determine the value of C for output pulse duration of 1 m sec. [5+6+4]
7. (a) Design a 32 to 1 multiplexer using four 74×151 multiplexers and 74×139 decoder.
   (b) Realize the following expression using 74×151 IC
   f(Y ) = AB + BC + AC [7+8]
8. (a) Design a modulo-8 binary counter and decoder with glitch-free outputs. Explain the operation.

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(b) Design a modulo-100 counter using two 74×163 binary counters. [7+8]

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Code No: 09A50201 **R09** **Set No. 4**

**III B.Tech I Semester Examinations,May/June 2012**
**IC APPLICATIONS**
**Common to Electronics And Telematics, Electronics And Communication Engineering, Electrical And Electronics Engineering**

**Time: 3 hours** **Max Marks: 75**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Define the terms with respect to logic families: fan out, power dissipation, propagation delay and noise margin.
   (b) Distinguish between open collector output and totem pole output. [8+7]
2. (a) State and explain Barkhausen criterion for oscillations.
   (b) Derive the expression for gain and frequency of oscillations of RC phase shift oscillator. [5+10]
3. (a) Draw the pin diagram of 555 timer and explain the function of each pin.
   (b) Write about the electrical specifications of 555 timer. [10+5]
4. (a) Draw the frequency response of practical differentiator and explain its working.
   (b) Design a differentiator that will differentiate an input signal with $f_{max}$=100Hz.
   (c) Mention some applications of Differentiation. [7+4+4]
5. (a) Explain the significance of current mirror in an OP-Amp circuit.
   (b) Discuss in detail about OP-Amp, compensating networks. [8+7]
6. (a) Design a conversion circuit to convert a T flip-flop to D flip-flop.
   (b) Explain the operation of parallel-in-parallel-out shift register. [7+8]
7. (a) Explain the operation of a multiplying DAC and mention its applications.
   (b) A 12-bit D to A converter has a full-scale range of 15 volts. Its maximum differential linearity error is ± 1/2 LSB.
      i. What is the percentage resolution?
      ii. What are the minimum and maximum possible values of the increment in its output voltage? [7+8]
8. (a) Design the 32 input to 5 output priority encoder using four 74LS148 and gates?
   (b) Design a CMOS transistor circuit with the functional behavior
   $f(x) = \left(A + \bar{B}\right)\left(B + \bar{D}\right)\left(A + \bar{D}\right)$ [8+7]

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**III B.Tech I Semester Examinations,May/June 2012**
**IC APPLICATIONS**
**Common to Electronics And Telematics, Electronics And Communication Engineering, Electrical And Electronics Engineering**
**Time: 3 hours** **Max Marks: 75**

**Answer any FIVE Questions**
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1. (a) Draw the circuit diagram, function table of a controlled D- latch.
   (b) Explain the operation of a D latch through suitable timing diagrams for various possibilities of input.
   (c) What are the problems encountered while using a D latch? Suggest methods to overcome these problems. [5+5+5]

2. (a) Define the terms:
      i. Free-running frequency $f_O$
      ii. Lock in range
      iii. Capture range
      iv. Pull in time.
   (b) Differentiate between analog and digital phase detector. [8+7]

3. (a) Draw the logic diagram of 74×194 and explain the operation.
   (b) Design a serial binary adder. [8+7]

4. (a) With a neat diagram explain about all pass filter.
   (b) Determine the order of a low pass Butter worth filter that is to provide 40 dB attenuation at $\omega/\omega_h = 2$. [8+7]

5. (a) Write about Instrumentation Amplifier with neat diagram.
   (b) Design a practical integrator circuit to integrate a sinusoidal input of 10 mV and upto 1 KHz.
   (c) Explain how Instrumentation amplifier can be used as Analog weight scale. [7+4+4]

6. (a) Explain the operation of an 8-bit tracking type Analog to Digital converter.
   (b) Compare the conversion times and efficiencies of 8-bit tracking type and successive approximation type Analog to Digital converters. [7+8]

7. (a) Draw the logic diagram equivalent to the internal structure of an 8-input CMOS NAND gate. Show the transistor circuit for this gate and explain the operation with the help of function table.
   (b) Draw the circuit diagram of basic CMOS gate and explain the operation. [11+4]

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8. (a) With a neat diagram explain about construction of differential amplifier with three OP Amps.
   (b) Explain how variable gain can be achieved with differential amplifiers. [8+7]

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Code No: 09A50201 **R09** **Set No. 3**

**III B.Tech I Semester Examinations,May/June 2012**
**IC APPLICATIONS**
**Common to Electronics And Telematics, Electronics And Communication Engineering, Electrical And Electronics Engineering**

**Time: 3 hours** **Max Marks: 75**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Mention the advantages and disadvantages of active filters over passive filters.
   (b) Write the various Design steps of Second order high pass Butter worth filter.
   (c) Explain about frequency scaling in active filters. [5+6+4]
2. (a) Explain 4 bit serial in parallel out register.
   (b) Draw the circuit of edge trigged SR flip flop made up of by basic gates & explain the operation. Sketch the wave form. [7+8]
3. (a) Write about classification of ICs on the basis of application and chip complexity.
   (b) Differentiate between monolithic and hybrid circuits with suitable examples.
   (c) Write about the temperature ranges and power supply requirements of Integrated circuits. [5+5+5]
4. (a) Explain the process of multiplication using operational amplifier.
   (b) Explain the processing of division using operational amplifier.
   (c) Explain how square root of a signal could be obtained using operational amplifier. [6+6+3]
5. (a) Describe about frequency divider using 555 timer.
   (b) With a neat diagram explain about pulse width modulation using 555 timer. [7+8]
6. (a) Using two 74×138 decoders design a 4 to 16 decoder.
   (b) Design a 32: 1 MUX using 74×151 MUX units and 74×139 decoder unit.[7+8]
7. (a) In which type of Analog to Digital converter, a Digital to Analog converter is used? Explain its operation in detail.
   (b) List important specifications of Analog to Digital converter and Digital to Analog converters indicating their typical values. [7+8]
8. (a) Explain in detail all the parameters of logic families.
   (b) Explain the operation of basic NAND and NOR latches.
   (c) Explain how a CMOS device is destroyed. [7+4+4]

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Code No: R31043 **R10** **Set No: 1**

III B.Tech. I Semester Regular Examinations, November/December - 2012

**LINEAR IC APPLICATIONS**

(Common to Electronics and Communications Engineering & Electronics and Instrumentation Engineering & Bio-Medical Engineering & Electronics and Computer Engineering)

**Time: 3 Hours** **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain DC coupling of cascaded differential amplifiers using relevant diagrams and necessary expressions.
   (b) Explain why $R_E$ is replaced by a constant current source in a differential amplifier circuit.

2. (a) An op-amp has a slew rate of 2V/μs. Find the rise time for an output voltage of 15V amplitude resulting from a rectangular pulse input if the op-amp is slew rate limited.
   (b) Define input offset voltage, total output offset voltage and also present the methods of compensation.

3. (a) Design a circuit using op-amp to generate a output $V_o= 0.1V_1-V_2+10V_3$ where $V_1,V_2,V_3$ are input voltages.
   (b) Explain the working of a Transconductance amplifier with floating and grounded loads. Is there any limitation on the size of the load when grounded?

4. (a) Construct a full wave rectifier using op-amps and explain the operation using the equivalent circuits and wave forms for $V_i>0$ and $V_i<0$ , where $V_i$ is input voltage.
   (b) What is the purpose of clamp diodes in a comparator? Draw a comparator where clamp diodes are used and explain the operation of a basic comparator.

5. (a) Draw the circuit diagram of a second order low-pass Butterworth filter and write the design steps of such filter.
   (b) Design a first order low-pass Butterworth filter with a cutoff frequency of 3 kHz and passband gain of 3.

6. (a) Draw the block diagram of a 565 PLL and explain its salient features. Derive the expression for capture range.
   (b) Explain the application of PLL as a frequency translator.

7. (a) A dual slope ADC uses a 16-bit counter and a 4 MHz clock rate. The maximum input voltage is +10V. The maximum integrator output voltage should be -8 V when the counter has cycled through $2^n$ counts. The capacitor used in the integrator is 0.1μF. Find the value of the resistor R of the integrator. If the analog signal voltage is +4.129 V, find the equivalent digital number.
   (b)Explain the working of successive approximation type converter and compare the conversion times of tracking and successive approximation type ADCs.

8. Write short notes on
   (a) Sample and hold amplifiers
   (b) Four quadrant multiplier

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Code No: R31043 **R10** **Set No: 2**

III B.Tech. I Semester Regular Examinations, November/December - 2012

**LINEAR IC APPLICATIONS**

(Common to Electronics and Communications Engineering & Electronics and Instrumentation Engineering & Bio-Medical Engineering & Electronics and Computer Engineering)

**Time: 3 Hours** **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain the methods to improve CMRR using relevant circuit diagrams.
   (b) Describe the advantages of differential amplifiers and justify their applicability in op-amp with reference to stability and noise immunity.

2. (a) Derive slew rate equation and discuss the effect of slew rate in applications of op-amp.
   (b) Explain the term thermal drift. Find the output voltage of a non-inverting amplifier if the temperature rises to $50^{o}$C for an offset voltage drift of 0.15mV/$^{o}$C if it was nulled at $25^{o}$C.

3. (a) Design a circuit using an op-amp to generate a output $V_o = -(0.2V_1+10V_2+V_3)$ , where $V_1, V_2, V_3$ are input voltages.
   (b) Explain the operation of high input impedance non-inverting AC amplifier.
   (c) Explain the operation of a practical differentiator.

4. (a) Construct a half wave rectifier using op-amps and explain the operation using relevant wave forms.
   (b) Draw the circuit of an anti-log amplifier and support with appropriate derivation.

5. (a) Describe the characteristics of a first order low-pass Butterworth filter and write the design steps of such filter.
   (b) Design a second order low-pass Butterworth filter at a high cutoff frequency of 2 kHz and write the expression for magnitude of frequency response of such filter.

6. (a) Draw the block diagram of a 565 PLL and explain its salient features. Derive the expression for lock range.
   (b) Design a 1 kHz square wave generator using 555 timer for duty cycle i)0.25 ii)0.5.

7. (a) Draw the circuit diagram of a 6 bit inverted R-2R ladder DAC. For V(1) = 5V, what is the maximum output voltage? What is the minimum voltage that can be resolved?
   (b) Explain the operation of dual slope ADC.

8. Write short notes on
   (a)Multiplexers.
   (b) Four quadrant multiplier.

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Code No: R31043 **R10** **Set No: 3**

III B.Tech. I Semester Regular Examinations, November/December - 2012

**LINEAR IC APPLICATIONS**

(Common to Electronics and Communications Engineering & Electronics and Instrumentation Engineering & Bio-Medical Engineering & Electronics and Computer Engineering)

**Time: 3 Hours** **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Draw the differential Amplifier circuit using BJT.
   (b) A differential amplifier has (i) CMRR = 1000 and (ii) CMRR = 10000. The first set of inputs is $\nu_1$ = 100 μV and $\nu_2$ = -100 μV. The second set of inputs is $\nu_1$ = 1100 μV and $\nu_2$ = 900 μV. Calculate the percentage difference in output voltages obtained for the two sets of input voltage and also comment on this.

2. (a)For an op-amp PSRR =60 db(min), CMRR= $10^4$ and the differential mode gain is $10^5$, the voltage changes by 20 V in 4 μ sec. calculate (i) numerical value of the PSRR (ii) common mode gain. (iii) Slew rate.
   (b) Explain why the frequency compensation is needed in op-amp's and what is role of a phase and gain margin.

3. (a) Explain how op-amp is used as differentiator with necessary equations. Draw the input and output waveforms by considering the sine wave as a input.
   (b) For a non inverting single supply AC amplifier $R_{in}$=50 Ω, $C_i$=0.1μF, $C_1$=0.1μF, $R_1$=$R_2$=$R_3$=100K Ω, $R_f$= 1M Ω and $V_{CC}$= +12 V. Determine the bandwidth of the amplifier and maximum voltage swing.

4. (a)Draw the Schmitt trigger circuit using OPAMP and explain its operation.
   (b) Explain about the zero crossing detector? How it is used as sine wave to square converter.

5. (a) Design a wide band reject filter having $f_H$=200 Hz, $f_L$=1 KHz with pass band gain of 2.
   (b) Why the narrow band filter is called as notch filter? Explain.

6. (a) Explain the operation of the PLL with the help of the block diagram.
   (b) Explain how the PLL is used as frequency synthesizer.

7. (a) Explain the working of the weighted resistor digital to analog converter and state the features.
   (b)LSB of 9-bit DAC is represented by 19.6 Volts. If an input of 9 zero bits is represented by 0 volts.
   (i) Find the output of the DAC for an input of 10110 1101 and 01101 1011.
   (ii )What is the full scale reading (FSR) of this DAC.

8. write a short note on
   (a) Sample and hold circuit.
   (b) Analog switches.

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Code No: R31043 **R10** **Set No: 4**

III B.Tech. I Semester Regular Examinations, November/December - 2012

**LINEAR IC APPLICATIONS**

(Common to Electronics and Communications Engineering & Electronics and Instrumentation Engineering & Bio-Medical Engineering & Electronics and Computer Engineering)

**Time: 3 Hours** **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a)For a differential amplifier $R_C$=1 KΩ, $R_S$=1 K Ω, $h_{ie}$=1 K Ω, $h_{fe}$=50, the emitter resistance of 2.5 M Ω while the differential input of 1 mV. Calculate the output voltage and CMRR in db. If the common mode input is 20 mV. Assume single ended output.
   (b) Explain the use of the active load to improve the CMRR.

2. (a) Explain the op-amp operation with the help of the block diagram.
   (b) Write the characteristics of the ideal op-amp? Write the characteristics and draw the pin diagram for 741 op-amp.

3. (a) Explain how the op-amp is used as integrator with necessary equations and draw the input and output waveforms by considering the square wave as input.
   (b) Design an inverting amplifier with an input resistance of 5 K Ω and the gain of -4.

4. (a) Design a op-amp free running multivibrator with ON period of 2 m sec. and OFF period of 3 msec.
   (b) Discuss how op amp is used as comparator. What are the limitations of the op-amp as comparators?

5. (a) What is an all pass filter? Show that the magnitude response of the all pass filter is 1.
   (b) Design a first order high pass filter at cutoff frequency of 500Hz. And pass band gain of 1.

6. (a) Explain the role of a low pass filter in PLL.
   (b) Explain about the free running range, capture range and lock range in PLL with necessary equations.

7. (a) Explain the R-2R Digital to analog converter with necessary sketches.
   (b) Find the step size and analog output for 4-bit R-2R ladder DAC when the input is 1000 and 1111. Assume $V_{ref}$=+5V.
   (c) If the maximum output voltage of a 7 bit D/A converter is 25.4 V. What is the smallest change in the output as the binary count increases.

8. write a short notes on
   (a) Analog switches.
   (b) Applications of the Sample and hold circuits.

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Code No: R05310402 **Set No. 1**

**III B.Tech I Semester Regular Examinations, November 2007**
**DIGITAL IC APPLICATIONS**
**( Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)**

**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) What are the parameters that are necessary to define the electrical characteristics of CMOS circuits? Mention the typical values of a CMOS NAND gate.
   (b) Design a CMOS 4-input AND-OR-INVERT gate. Draw the logic diagram and function table. [8+8]
2. (a) Mention the DC noise margin levels of ECL 10K family.
   (b) A single pull-up resistor to +5V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor? How much high state DC noise margin can be provided in this case? [6+10]
3. (a) Write a VHDL Entity and Architecture for a 3-bit synchronous counter using Flip-Flops.
   (b) Explain the use of Packages. Give the syntax and structure of a package in VHDL. [8+8]
4. Design a logic circuit to detect prime number of a 5-bit input. Write the structural VHDL program for the same. [16]
5. Design a 10 to 4 encoder with inputs 1- out of ?10 code and outputs in BCD? Provide the data flow style VHDL program? [16]
6. Write VHDL program for 1-bit comparator circuit with the input bits and equal, grater than and less than inputs from the previous stage and the outputs contain equal, greater than and less than conditions. Using this entity write VHDL program for 16-bit comparator using data flow style. Do not use any additional logic for this purpose. [16]
7. (a) Differentiate between ripple counter and synchronous counter? Design a 4-bit counter in both modes and estimate the propagation delay.
   (b) Design a modulo-88 counter using 74X163 Ics. [8+8]
8. (a) Explain the necessity of two-dimensional decoding mechanism in memories. Draw MOS transistor memory cell in ROM and explain the operation.
   (b) Determine the ROM size needed to realize the logic function performed by 74×153 and 74×139. [8+8]

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Code No: R05310402 **Set No. 2**

**III B.Tech I Semester Regular Examinations, November 2007**
**DIGITAL IC APPLICATIONS**
**( Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)**

**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Explain how to estimate sinking current for low output and sourcing current for high output of CMOS gate.
   (b) Analyze the fall time of CMOS inverter output with $R_L = 100\Omega, V_L = 2.5V$ *and* $C_L = 10PF$. Assume $V_L$ as stable state voltage. [8+8]

2. (a) Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation.
   (b) Explain sinking current and sourcing current of TTL output. Which of the above parameters decide the fan-out and how? [8+8]

3. (a) Write a VHDL Entity and Architecture for the following function?

$$F(x) = a \oplus b \oplus c$$

   Also draw the relevant logic diagram.
   (b) Explain the use of Packages Give the syntax and structure of a package in VHDL [8+8]

4. Design the logic circuit and write a data-flow style VHDL program for the following functions.
   (a) $F(X) = \Sigma_{A,B,C,D}\,(0, 2, 5, 7, 8, 10, 13, 15) + d\,(1, 6, 11)$
   (b) $F(Y) = \Pi_{A,B,C,D}\,(1, 4, 5, 7, 9, 11, 12, 13, 15))$ [8+8]

5. With the help of logic diagram explain 74×157 multiplexer? Write the data flow style VHDL program for this IC? [16]

6. Design a 24-bit comparator circuit using 74×682 ICs and discuss the functionality of the circuit. Also implement VHDL source code in data flow style. [16]

7. (a) Distinguish between latch and flip-flop. Show the logic diagram for both. Explain the operation with the help of function table.
   (b) Design a Modulo-12 ripple counter using 74×74? Write a VHDL program for this logic using data flow style. [8+8]

8. (a) Discuss how PROM, EPROM and EEPROM technologies differ from each other.

(b) With the help of timing waveforms, explain read and write operations of SRAM. [8+8]

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Code No: R05310402 **Set No. 3**

**III B.Tech I Semester Regular Examinations, November 2007**
**DIGITAL IC APPLICATIONS**
**( Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)**

**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Design CMOS transistor circuit for 3-input AND gate. With the help of function table explain the operation of the circuit diagram.
   (b) Design a CMOS transistor circuit that has the functional behavior as

$$f(x) = \overline{(a + \overline{b})\ (b\ +\ c)(a + \overline{c})}$$

   Also draw the relevant circuit diagrams. [8+8]

2. (a) Explain the following terms with reference to TTL gate.
      i. Voltage levels for logic '1' & logic '0'
      ii. DC Noise margin
      iii. Low-state unit load
      iv. High-state fan-out
   (b) Design a transistor circuit of 2-input ECL NOR gate. Explain the operation with the help of function table. [8+8]

3. Explain with an example the syntax and the function of the following VHDL statements.
   (a) Process statement
   (b) If, else and elseif statements
   (c) Case statement
   (d) Loop statement [4×4=16]

4. Design a logic circuit to detect prime number of a 5-bit input. Write the structural VHDL program for the same. [16]

5. (a) It is necessary to identify the position of mechanical disk, when rotates with a step of $45^0$. Give the necessary encoding mechanism and draw the logic circuit?
   (b) Using two 74×138 decoders design a 4 to 16 decoder. [16]

6. (a) Write a VHDL program for the circuit that counts number of Ones in a 16-bit register using structural style of modeling.
   (b) Design a 4×4 combinational multiplier and the write the necessary VHDL program data flow model. [8+8]

7. Show the logic diagram of 74×175 IC and write VHDL program for this IC in data flow style. Using this entity develop the program for 16-bit register and show the corresponding circuit also explain how the register is cleared? [16]

8. (a) Draw the basic cell structure of Dynamic RAM. What is the necessity of refresh cycle? Explain the timing requirements of refresh operation.

   (b) Discuss in detail ROM access mechanism with the help of timing waveforms. [8+8]

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Code No: R05310402 **Set No. 4**

**III B.Tech I Semester Regular Examinations, November 2007**
**DIGITAL IC APPLICATIONS**
**( Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)**

**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Design CMOS transistor circuit for 3-input AND gate. With the help of function table explain the operation of the circuit diagram.
   (b) Design a CMOS transistor circuit that has the functional behavior as

$$f(x) = \overline{(\mathrm{a} + \overline{\mathrm{b}})\ (\mathrm{b}\ +\ \mathrm{c})(\mathrm{a} + \overline{\mathrm{c}})}$$

   Also draw the relevant circuit diagrams. [8+8]

2. (a) Design a transistor circuit of 2-input ECL NOR gate. Explain the operation with the help of function table.
   (b) A single pull-up resistor to +5V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor? How much high state DC noise margin can be provided in this case? [8+8]

3. (a) Explain the various data types supported by VHDL. Give the necessary examples.
   (b) Discuss the case statement and its use in the VHDL program. [8+8]

4. Design a logic circuit to detect prime number of a 5-bit input. Write the structural VHDL program for the same. [16]

5. Design a two-digit BCD adder with logic gates. Using this logic write the VHDL program. In structural style of modeling. [8+8]

6. Design a combinational logic circuit that counts the number of ones in a 24-bit register. Write a VHDL program for the same using structural style or modeling. [16]

7. (a) Draw the logic diagram of 74×163 binary counter and explain its operation.
   (b) Design a modulo-100 counter using two 74×163 binary counters? [8+8]

8. (a) Design an 8×4 diode ROM using 74×138 for the following data starting from the first location.

$$6, 9, 0, C, D, 1, F, D$$

   (b) How many ROM bits are required to build a 16-bit adder/subtractor with mode control, carry input, carry output and two's complement overflow output. Show the block schematic with all inputs and outputs. [8+8]

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Code No: R05310401 **Set No. 1**

**III B.Tech I Semester Regular Examinations, November 2007**
**LINEAR IC APPLICATIONS**
**(Electronics & Communication Engineering)**

**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Explain the use of constant bias circuit in operation of differential amplifier.
   (b) Analyze the dual input balanced output configuration of differential amplifier using DC. [8+8]
2. (a) Explain how the input offset voltage compensated for?
   (b) How fast can the output of an op - amp change by 10V, if its slew rate is 1 V/$\mu$s.
   (c) Define thermal drift & slew rate. [6+4+6]
3. (a) Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 1KHz. If a sine wave of 1V peak at 1000 Hz is applied to this differentiator draw the output waveforms.
   (b) Why active differentiator circuits are not used in analog computer to solve differential equations. [10+6]
4. (a) Explain, How to obtain triangular wave using a square wave generator.
   (b) With the help of a neat circuit diagram explain the working of a logarithmic amplifier. [8+8]
5. (a) Define Bessel, Butterworth and Chebysher filters, and compare their frequency response.
   (b) Sketch the circuit diagram of band elimination filter and design a wide band-reject having $f_H$=200Hz and $f_L$=1KHz. Assume necessary data. [8+8]
6. Explain an application in which the 555 timer can be used as Astable multivibrator. [16]
7. (a) Compare R - 2R and weight resistor types of DACs.
   (b) Write short notes on A/D converters.
   (c) Define the following terms as related to DAC:
      i. Linearity
      ii. Resolution. [8+4+4]
8. What are all basic blocks of analog multiplexer? Explain how the data selections process is performed it. [16]

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Code No: R05310401 **Set No. 2**

**III B.Tech I Semester Regular Examinations, November 2007**
**LINEAR IC APPLICATIONS**
**(Electronics & Communication Engineering)**

**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Explain how large open circuit voltage gain of an op - amp can be obtained by using cascading of differential amplifier stages.
   (b) Explain ac analysis of differential amplifier. [8+8]
2. (a) Discuss the Pole - Zero and Dominant pole compensation techniques for an op - amp.
   (b) An op - amp has a slew rate of 1.5V/$\mu$s. What is the maximum frequency of an output sinusoid of peak value 10 V at which the distortion sets in due to the slew rate limitation? [8+8]
3. (a) Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 1KHz. If a sine wave of 1V peak at 1000 Hz is applied to this differentiator draw the output waveforms.
   (b) Why active differentiator circuits are not used in analog computer to solve differential equations. [10+6]
4. (a) Describe the operation of logarithmic amplifier using op - amp.
   (b) List the conditions for oscillation in all the three types of oscillators, namely, RC phase shift, Wien - bridge and quadrature oscillators. [8+8]
5. (a) Draw the wide band reject filter circuit and also the frequency response of it.
   (b) Draw the schematic diagram of an all pass filter and determine the phase shift $\phi$ between the input and output at f = 2kHz. [8+8]
6. (a) Configure a 555 timer as a Schmitt trigger and explain.
   (b) Explain frequency translation and FSK demodulation using 565 PLL. [8+8]
7. (a) Explain the difference between Analog to Digital converter and Digital to Analog converters through underlying equations.
   (b) Illustrate one application each of Analog to Digital and Digital to Analog converters. [6+10]
8. (a) Explain the function of a typical adjustable voltage regulator. How can you increase the current driving capacity of the regulator?
   (b) Describe the principle of working of a balanced modulator using op - amp. Give the applications of it. [6+10]

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Code No: R05310401 **Set No. 3**

**III B.Tech I Semester Regular Examinations, November 2007**
**LINEAR IC APPLICATIONS**
**(Electronics & Communication Engineering)**

**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Explain how large open circuit voltage gain of an op - amp can be obtained by using cascading of differential amplifier stages.
   (b) Explain ac analysis of differential amplifier. [8+8]
2. (a) Calculate the effect of variation in power supply voltages on the output offset voltage for an op - amp circuit.
   (b) Why frequency compensation is required for an op - amp and explain frequency compensation technique using suitable diagrams. [6+10]
3. (a) Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 1KHz. If a sine wave of 1V peak at 1000 Hz is applied to this differentiator draw the output waveforms.
   (b) Why active differentiator circuits are not used in analog computer to solve differential equations. [10+6]
4. (a) Derive the expression of the output voltage of an antilog amplifier using op - amp.
   (b) Design a saw tooth wave form generator using op - amp and plot the waveforms for the given specifications frequency: 5kHz, $V_{sat} = \pm$ 15V (Assume necessary data). [8+8]
5. (a) For the all pass filter, determine the phase shift $\phi$ between the input and output at f = 2kHz. To obtain a phase shift $\phi$ , what modifications are necessary in the circuit?
   (b) Derive the expression for the transfer function of $2^{nd}$ order High pass filter. [8+8]
6. (a) Explain the operation of Monostable multivibrator using 555 timer. Derive the expression of time delay of a Monostable multivibrator using 555 timer.
   (b) Design monostable multivibrator using 555 timer to produce a pulse width of 100 m sec. [10+6]
7. (a) What are the basic blocks preceding an Analog to Digital converter in a typical application like digital audio recording?
   (b) With the help of a neat circuit diagram and waveforms, explain the operation of a dual slope ADC. What are its special features? [6+10]
8. Write short notes on:

(a) IC 1496 and its applications

(b) Sample and hold circuit. [16]

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Code No: R05310401 **Set No. 4**

**III B.Tech I Semester Regular Examinations, November 2007**
**LINEAR IC APPLICATIONS**
**(Electronics & Communication Engineering)**

**Time: 3 hours** **Max Marks: 80**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) Discuss the differences between the differential amplifiers used in the first two stages of op - amp.
   (b) Compare and contrast an ideal op - amp and practical op - amp.
   (c) Draw an ideal voltage transfer curve of an op - amp. [8+5+3]
2. (a) What are the three factors that effect the electrical parameters of an op - amp
   (b) Compare and contrast an ideal op - amp and practical op - amp.
   (c) What are the features of 741 op - amp and also draw the pin diagram.[3+6+7]
3. (a) Draw the circuit diagram of a two input non-inverting type summing amplifier and derive the expression for the output voltage.
   (b) Briefly explain why negative feedback is desirable in amplifier applications.
   (c) How does negative feedback affect the performance of an inverting amplifier? [7+5+4]
4. (a) Derive the expression of the output voltage of an antilog amplifier using op - amp.
   (b) Design a saw tooth wave form generator using op - amp and plot the waveforms for the given specifications frequency: 5kHz, $V_{sat} = \pm$ 15V (Assume necessary data). [8+8]
5. (a) List the conditions for oscillation in all the three types of oscillators, namely, RC phase shift, Wien - bridge and quadrature oscillators.
   (b) Design an op ? amp based relaxation oscillator and derive the frequency of oscillation. [8+8]
6. (a) Draw the circuit of PLL as frequency multiplier and explain its working.
   (b) Explain with neat diagram how 555 timers can be used as a Schmitt trigger. [8+8]
7. (a) Sketch and explain the transfer characteristic of a DAC with necessary equations.
   (b) LSB of a 9 - bit DAC is represented by 19.6mv. If an input of 9 zero bits is represented by 0 volts.
      i. Find the output of the DAC for an input 10110 1101 and 01101 1011.
      ii. What is the Full scale reading (FSR) of this DAC? [8+8]

8. (a) Describe the operation of four quadrant multiplier with neat diagram.
   (b) Explain the operation of IC 1496 as mixer circuit. [8+8]

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| Code No: RR311001 | RR | SET-1 |
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**B. Tech III Year I Semester Examinations, December-2011**

**LINEAR AND DIGITAL IC APPLICATIONS**

**(COMMON TO ELECTRONICS AND INSTRUMENTATION ENGINEERING, MECHANICAL ENGINEERING(MECHATRONICS), ELECTRONICS AND TELEMATICS ENGINEERING)**

**Time: 3 hours** **Max. Marks: 80**

**Answer any five questions**

**All questions carry equal marks**

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1.a) Compare the ideal and practical characteristics of an op-amp.
b) Explain the miller frequency compensation technique employed in op-amp.
c) Explain the significance of Virtual ground in an op-amp. [16]

2.a) An IC op-amp 741 is used as an inverting amplifier with a gain of 100. The voltage gain Vs Frequency characteristic is flat upto 12KHZ. Find the maximum peak-to-peak input signal that can be fed without causing any distortion to the output?
b) Explain and draw the output waveforms of the ideal integrator circuit when the input is square-wave.
c) Draw the circuit diagram of an logarithmic amplifier using op-amps and explain its operation. [16]

3.a) What is timer IC555? Draw the internal structure of IC555 Timer.
b) List the applications of 555 timer. [8+8]

4.a) Explain the method of boosting the current of a three terminal voltage regulator.
b) Draw the block diagram of PLL and explain the function of each block. [8+8]

5.a) Define an all-pass filter How can it be justifiably called a phase shift circuit?
b) Design a narrowband bandpass filter using op-amp. The resonant frequency is 100Hz and Q=2. Assume C=0.1 μF. [8+8]

6.a) What is tristate logic? Give some examples.
b) How to interface the TTL logic gates to the CMOS logic gates.
c) Draw the basic DTL Gate and explain its operation. [16]

7.a) What are the limitations of weighted resistor type D/A converter?
b) What do you mean by quantization error in an A/D converter/?
c) With neat block diagram, explain successive approximation type A/D converter in detail. [16]

8. Write a short notes on the following
a) IC1496
b) VCSV. [16]

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| Code No: RR311001 | RR | SET-2 |
|---|---|---|

**B. Tech III Year I Semester Examinations, December-2011**
**LINEAR AND DIGITAL IC APPLICATIONS**
**(COMMON TO ELECTRONICS AND INSTRUMENTATION ENGINEERING, MECHANICAL ENGINEERING(MECHATRONICS), ELECTRONICS AND TELEMATICS ENGINEERING)**

**Time: 3 hours** **Max. Marks: 80**

**Answer any five questions**
**All questions carry equal marks**
**---**

1.a) What is timer IC555? Draw the internal structure of IC555 Timer.
b) List the applications of 555 timer. [8+8]

2.a) Explain the method of boosting the current of a three terminal voltage regulator.
b) Draw the block diagram of PLL and explain the function of each block. [8+8]

3.a) Define an all-pass filter How can it be justifiably called a phase shift circuit?
b) Design a narrowband bandpass filter using op-amp. The resonant frequency is 100Hz and Q=2. Assume C=0.1 μF. [8+8]

4.a) What is tristate logic? Give some examples.
b) How to interface the TTL logic gates to the CMOS logic gates.
c) Draw the basic DTL Gate and explain its operation. [16]

5.a) What are the limitations of weighted resistor type D/A converter?
b) What do you mean by quantization error in an A/D converter/?
c) With neat block diagram, explain successive approximation type A/D converter in detail. [16]

6. Write a short notes on the following
a) IC1496
b) VCSV. [16]

7.a) Compare the ideal and practical characteristics of an op-amp.
b) Explain the miller frequency compensation technique employed in op-amp.
c) Explain the significance of Virtual ground in an op-amp. [16]

8.a) An IC op-amp 741 is used as an inverting amplifier with a gain of 100. The voltage gain Vs Frequency characteristic is flat upto 12KHZ. Find the maximum peak-to-peak input signal that can be fed without causing any distortion to the output?
b) Explain and draw the output waveforms of the ideal integrator circuit when the input is square-wave.
c) Draw the circuit diagram of an logarithmic amplifier using op-amps and explain its operation. [16]

**--ooOoo--**

| Code No: RR311001 | RR | SET-3 |
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**B. Tech III Year I Semester Examinations, December-2011**
**LINEAR AND DIGITAL IC APPLICATIONS**
**(COMMON TO ELECTRONICS AND INSTRUMENTATION ENGINEERING, MECHANICAL ENGINEERING(MECHATRONICS), ELECTRONICS AND TELEMATICS ENGINEERING)**

**Time: 3 hours** **Max. Marks: 80**

**Answer any five questions**
**All questions carry equal marks**
**---**

1.a) Define an all-pass filter How can it be justifiably called a phase shift circuit?
b) Design a narrowband bandpass filter using op-amp. The resonant frequency is 100Hz and Q=2. Assume C=0.1 μF. [8+8]

2.a) What is tristate logic? Give some examples.
b) How to interface the TTL logic gates to the CMOS logic gates.
c) Draw the basic DTL Gate and explain its operation. [16]

3.a) What are the limitations of weighted resistor type D/A converter?
b) What do you mean by quantization error in an A/D converter/?
c) With neat block diagram, explain successive approximation type A/D converter in detail. [16]

4. Write a short notes on the following
a) IC1496
b) VCSV. [16]

5.a) Compare the ideal and practical characteristics of an op-amp.
b) Explain the miller frequency compensation technique employed in op-amp.
c) Explain the significance of Virtual ground in an op-amp. [16]

6.a) An IC op-amp 741 is used as an inverting amplifier with a gain of 100. The voltage gain Vs Frequency characteristic is flat upto 12KHZ. Find the maximum peak-to-peak input signal that can be fed without causing any distortion to the output?
b) Explain and draw the output waveforms of the ideal integrator circuit when the input is square-wave.
c) Draw the circuit diagram of an logarithmic amplifier using op-amps and explain its operation. [16]

7.a) What is timer IC555? Draw the internal structure of IC555 Timer.
b) List the applications of 555 timer. [8+8]

8.a) Explain the method of boosting the current of a three terminal voltage regulator.
b) Draw the block diagram of PLL and explain the function of each block. [8+8]

**--ooOoo--**

Code No: RR311001 | RR | SET-4

**B. Tech III Year I Semester Examinations, December-2011**
**LINEAR AND DIGITAL IC APPLICATIONS**
**(COMMON TO ELECTRONICS AND INSTRUMENTATION ENGINEERING, MECHANICAL ENGINEERING(MECHATRONICS), ELECTRONICS AND TELEMATICS ENGINEERING)**

**Time: 3 hours** **Max. Marks: 80**

**Answer any five questions**
**All questions carry equal marks**
**---**

1.a) What are the limitations of weighted resistor type D/A converter?
b) What do you mean by quantization error in an A/D converter/?
c) With neat block diagram, explain successive approximation type A/D converter in detail. [16]

2. Write a short notes on the following
a) IC1496
b) VCSV. [16]

3.a) Compare the ideal and practical characteristics of an op-amp.
b) Explain the miller frequency compensation technique employed in op-amp.
c) Explain the significance of Virtual ground in an op-amp. [16]

4.a) An IC op-amp 741 is used as an inverting amplifier with a gain of 100. The voltage gain Vs Frequency characteristic is flat upto 12KHZ. Find the maximum peak-to-peak input signal that can be fed without causing any distortion to the output?
b) Explain and draw the output waveforms of the ideal integrator circuit when the input is square-wave.
c) Draw the circuit diagram of an logarithmic amplifier using op-amps and explain its operation. [16]

5.a) What is timer IC555? Draw the internal structure of IC555 Timer.
b) List the applications of 555 timer. [8+8]

6.a) Explain the method of boosting the current of a three terminal voltage regulator.
b) Draw the block diagram of PLL and explain the function of each block. [8+8]

7.a) Define an all-pass filter How can it be justifiably called a phase shift circuit?
b) Design a narrowband bandpass filter using op-amp. The resonant frequency is 100Hz and Q=2. Assume C=0.1 μF. [8+8]

8.a) What is tristate logic? Give some examples.
b) How to interface the TTL logic gates to the CMOS logic gates.
c) Draw the basic DTL Gate and explain its operation. [16]

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