INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

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ELECTRONICS AND COMMUNICATION ENGINEERING

DEFINITIONS AND TERMINOLOGY QUESTION BANK

Course Name	:	DIGITAL SIGNAL PROCESSSORS AND ARCHITECTURE
Course Code	:	AEC507
Program	:	B.Tech
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Section	:	A,B,C,D
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Course Faculty	:	Mrs. C.Devisupraja, Assistant Professor, ECE

OBJECTIVES:

I	Impart the knowledge of basic DSP concepts and number systems to be used, different types of A/D, D/A conversion errors.
II	Learn the architectural differences between DSP and General purpose processor.
III	Learn about interfacing of serial & parallel communication devices to the processor.
IV	Implement the DSP & FFT algorithms.

DEFINITIONS AND TERMINOLOGY QUESTION BANK

S.No	QUESTION	ANSWER	BLOOMS TAXONOMY LEVEL	CO	CLO	CLO Code
	UNIT -I INTRODUCTION TO DIGITAL SIGNAL PROCESSING					
1	What is a SIGNAL?	A signal is a source of information, generally a physical quantity, which varies with respect to time, space, temperature like any independent variable".	Remember	CO 1	CLO 1	AEC507.01
2	What is a System?	System is a device or combination of devices, which can operate on signals and produces corresponding response. Input to a system is called as excitation and output from it is called as response.	Remember	CO 1	CLO 2	AEC507.02
3	Define Analog Signal?	Analog signals are continuous wave signals that change with time period	Remember	CO 1	CLO 1	AEC507.01
4	Define Digital Signal?	A digital signal is a signal that is being used to represent data as a sequence of discrete values; at any given time it can only take on one of a finite number of values.	Remember	CO 1	CLO 2	AEC507.02
5	What is Nyquist sampling rate?	According to the Nyquist Theorem, the sampling rate must be at least $2f_{max}$, or twice the highest analog frequency component.	Remember	CO 1	CLO 1	AEC507.01

S.No	QUESTION	ANSWER	BLOOMS TAXONOMY LEVEL	CO	CLO	CLO Code
6	What is DSP?	Digital signal processing (DSP) refers to performing operations on discrete and digital signals. i.e Processing of discrete signals by means of digital.	Remember	CO 1	CLO 2	AEC507.02
7	What is meant by radix -2?	FFT is most efficient algorithm to compute DFT. if number of output points N can be expressed as power of 2 then this algorithm known as radix -2 FFT algorithms.	Remember	CO 1	CLO 3	AEC507.03
8	Define Zero Padding	It simply refers to adding **zeros** to end of a time-domain signal to increase its length.	Understand	CO 1	CLO 1	AEC507.01
9	Define Convolution	Convolution is a mathematical way of combining two signals to form a third signal.	Understand	CO 1	CLO 2	AEC507.02
10	Define Linear convolution	A mathematical approach to determine the response of an LTI system with input and impulse response. If x(n) is a sequence of L number of samples and h(n) with M number of samples, after convolution y(n) will have N=L+M-1 samples.	Understand	CO 1	CLO 3	AEC507.03
11	Define Circular convolution	Circular convolution is same as linear convolution but circular is for periodic signals	Remember	CO 1	CLO 2	AEC507.02
12	What is meant by Aliasing	Aliasing refers to the effect produced when a signal is imperfectly reconstructed from the original signal. Aliasing occurs when a signal is not sampled at a high enough frequency to create an accurate representation.	Remember	CO 1	CLO 1	AEC507.01
13	What Is Meant By Fixed Point Number?	Fixed-point numbers are useful for representing fractional values, usually in base 2 or base 10, when the executing processor has no floating point unit	Remember	CO 1	CLO 4	AEC507.04
14	What is a power signal?	A power signal is one whose average power P= finite value and whose total energy E=∞.	Understand	CO 1	CLO 1	AEC507.01
15	How will you classify the discrete time signals?	Causal and Non causal, Periodic and non periodic, even and odd, energy and power signals.	Remember	CO 1	CLO 2	AEC507.02
16	Define time invariant system	If a system's operation is independent of time then its time invariant, i.e delayed system response is equal to system's response for delayed input.	Remember	CO 1	CLO 1	AEC507.01
17	What is linear system	If a system satisfies homogeneity principle and superposition principle then it is Linear.	Remember	CO 1	CLO 2	AEC507.02
18	What is Non linear system	If a system does not satisfies homogeneity principle and superposition principle then it is Non Linear system.	Understand	CO 1	CLO 3	AEC507.03
19	Define Floating Point number	A floating-point number is one where the position of the decimal point can "float" rather than being in a fixed position within a number.	Understand	CO 1	CLO 3	AEC507.03
20	Define Q-Notation	Q is a fixed point number format where the number of fractional bits are specified.	Understand	CO 1	CLO 1	AEC507.01

S.No	QUESTION	ANSWER	BLOOMS TAXONOMY LEVEL	CO	CLO	CLO Code
21	Define Auto Correlation	Autocorrelation can also be referred to as lagged correlation or serial correlation, as it measures the relationship between a variable's current value and its past values.	Understand	CO 1	CLO 2	AEC507.02
22	What is meant by radix -2?	FFT is most efficient algorithm to compute DFT. if number of output points N can be expressed as power of 2 .	Understand	CO 1	CLO 2	AEC507.02
23	Why convolution is required?.	Convolution is required to determine the response of an LTI system for a given input and impulse response	Remember	CO 1	CLO 1	AEC507.01
24	List the methods used in sectional convolution.	Over- lap save method and over-lap add method	Remember	CO 1	CLO 3	AEC507.03
25	What is zero padding?	Number of zeros adding to given length sequence To obtained desired length of sequence from given length of sequence	Remember	CO 1	CLO 4	AEC507.04
26	What are uses of zero padding?	To get better display of frequency spectrum .With zero padding, DFT can be used in linear filtering	Understand	CO 1	CLO 1	AEC507.01
27	What is meant by sectioned convolution?	If the input data sequence of longer duration , it is very difficult to obtained the output sequence due to limited memory of digital system therefore input data sequence is divided into smaller sections . These sections are processed separately one at a time and combined later to get output.	Remember	CO 1	CLO 2	AEC507.02
28	What is divide and conquer approach?	This approach is based on the decomposition of an N point DFT into successively smaller DFTs this leads to a family computationally efficient algorithm. N factorized as two integers.	Remember	CO 1	CLO 2	AEC507.02
29	What is Linear time invariant system (LTI)?	A LTI system is one which obeys properties of linearity and time invariant. These systems are characterized by unit sample response. Output of LTI system is computed by convolution of input and unit sample response.	Remember	CO 1	CLO 3	AEC507.03
30	What is an energy signal?	An energy signal is one whose total energy E=finite value and whose average power P=0.	Remember	CO 1	CLO 2	AEC507.02
UNIT – II ARCHITECTURE OF PROGRAMMABLE DSPs						
1	What is the role of Barrel shifter in Programmable DSP?	A barrel shifter is a digital circuit that can shift a data word by a specified number of bits without the use of any sequential logic, only pure combinational logic.	Understand	CO 2	CLO 6	AEC507.06
2	Explain guard bits in a MAC unit of Programmable DSP.	Guard bits are extra bits which are produced while the intermediate steps to yield maximum accuracy in the final results. In numerical analysis, one or more guard digits can be used to reduce	Remember	CO 2	CLO 7	AEC507.07

S.No	QUESTION	ANSWER	BLOOMS TAXONOMY LEVEL	CO	CLO	CLO Code
		the amount of round off error.				
3	List the various Applications of Programmable DSP.	• Audio applications • MPEG Audio • Portable audio • Digital cameras	Remember	CO 2	CLO 7	AEC507.07
4	What are the types of Programmable DSPs	• Multiplier • Shifter • Multiply and accumulate (MAC) unit • Arithmetic logic unit	Remember	CO 2	CLO 6	AEC507.06
5	What are the Specialized addressing modes in Programmable DSPs	• Circular Addressing Mode • Bit Reversal	Remember	CO 2	CLO 6	AEC507.06
6	Write about Circular Buffers of Programmable DSPs	Circular buffering is also useful in off-line processing. Consider a program where both the input and the output signals are completely contained in memory. for the calculation at hand.	Remember	CO 2	CLO 6	AEC507.06
7	Define Harvard architecture of Programmable DSP Processors	The Harvard architecture is a computer architecture with separate storage and signal pathways for instructions and data	Understand	CO 2	CLO 5	AEC507.05
8	List the architectural features of Programmable DSP Processors.	• Multiplier • Shifter • Multiply and accumulate (MAC) unit • Arithmetic logic unit	Remember	CO 2	CLO 5	AEC507.05
9	Write about Bit-reversed addressing of Programmable DSPs	Bit-reversed addressing is used for simplifying and speeding-up the access to the arrays in FFT (Fast Fourier Transform) algorithms.	Remember	CO 2	CLO 6	AEC507.06
10	What is VLIW architecture.	Very long instruction word (VLIW) refers to instruction set architectures designed to exploit instruction level parallelism (ILP). VLIW processor allows programs to explicitly specify instructions to execute in parallel.	Remember	CO 2	CLO 8	AEC507.08
11	List the advantages of VLIW architecture.	• Reduces Hardware Complexity • Dependencies are determined by the compiler	Understand	CO 2	CLO 6	AEC507.06
12	Define Von Neumann Architecture	A von Neumann architecture machine, designed by physicist and mathematician John von Neumann (1903–1957) is a theoretical design for a stored program computer that serves as the basis for almost all modern computers. A von Neumann machine consists of a central processor with an arithmetic/logic unit and a control unit, a memory, mass storage, and input and output. A central processor consisting of a control unit and an arithmetic/logic unit.	Understand	CO 2	CLO 5	AEC507.05

S.No	QUESTION	ANSWER	BLOOMS TAXONOMY LEVEL	CO	CLO	CLO Code
13	List the disadvantages of VLIW architecture.	• Higher complexity of the compiler • Unscheduled events • Code density • Code expansion	Remember	CO 2	CLO 8	AEC507.08
14	What is pipelining technique?	Pipelining is a technique where multiple instructions are overlapped during execution. Pipeline is divided into stages and these stages are connected with one another to form a pipe like structure. Instructions enter from one end and exit from another end. Pipelining increases the overall instruction throughput.	Remember	CO 2	CLO 7	AEC507.07
15	What are the different stages in pipelining?	• Instruction fetch • Instruction decode and register fetch • Execute • Memory access • Register write back	Remember	CO 2	CLO 7	AEC507.07
16	Define the SIMD architecture.	SIMD instructions are widely used to process 3D graphics, although modern graphics cards with embedded SIMD have largely taken over this task from the CPU. Some systems also include permute functions that re-pack elements inside vectors, making them particularly useful for data processing and compression. They are also used in cryptography.	Understand	CO 2	CLO 7	AEC507.07
17	Define underflow condition	A condition in which the value of a computed quantity is smaller than the smallest non-zero value that can be physically stored; usually treated as an error condition. The error condition that results from an attempt to retrieve an item from an empty stack.	Remember	CO 2	CLO 6	AEC507.06
18	Define overflow condition	An error that occurs when the computer attempts to handle a number that is too large for it. Every computer has a well-defined range of values that it can represent. If during execution of a program it arrives at a number outside this range, it will experience an overflow error. Overflow errors are sometimes referred to as overflow conditions.	Remember	CO 2	CLO 6	AEC507.06
19	List out various special Addressing modes	• Circular Addressing Mode • Bit Reversal	Remember	CO 2	CLO 7	AEC507.07
15	Explain working of bit reversed Addressing mode	Address generation unit can be provided with the capability of providing bit-reversed indices.	Understand	CO 2	CLO 8	AEC507.08
21	Explain About Indirect Addressing mode	In the indirect address mode uses the auxiliary register (ARS) to hold the address of operand in memory . in direct addressing ,any location in the 64-k word data memory space can be accessed using a 16- bit address contained in AR . each auxiliary register (AR0-AR7) provide flexible and powerful indirect addressing .	Understand	CO 2	CLO 7	AEC507.07

S.No	QUESTION	ANSWER	BLOOMS TAXONOMY LEVEL	CO	CLO	CLO Code
22	Write the applications of barrel shifter	• Pre scaling an input data-memory operand or the accumulator value before an ALU operation. • Performing a logical or arithmetic shift of the accumulator value. • Normalizing the accumulator. • Post scaling the accumulator before storing the accumulator value into data memory.	Understand	CO 2	CLO 7	AEC507.07
23	Define Host Port Interface	The Host Port Interface (HPI) is an 8-bit parallel port that interfaces a host device or host processor to the C54xE DSP. Information is exchanged between the C54x DSP and the host device through on-chip C54x DSP memory that is accessible by both the host and the C54x DSP	Understand	CO 2	CLO 7	AEC507.07
24	Explain About Immediate Addressing mode	Immediate addressing is used to handle constant data . it allows the program to operate on an actual value . the data can be either a 16-bit constant or constant length 7.9 or 13. depending on the length of the data , the addressing mode is referred to as long immediate or short immediate addressing mode	Understand	CO 2	CLO 7	AEC507.07
25	Explain About Multiply-Accumulate (MAC) Function	The MAC speed applies both to finite impulse response (FIR) and finite impulse response (IIR) filters. The complexity of the filter response dictates the number MAC operations required per sample period.	Understand	CO 2	CLO 6	AEC507.06
26	Define Accumulator	An accumulator is a register for short-term, intermediate storage of arithmetic and logic data in a computer's CPU (central processing unit).	Understand	CO 2	CLO 7	AEC507.07
27	Define Memory-Mapped Registers	The data memory space contains memory-mapped registers for the CPU and the on-chip peripherals. These registers are located on data page 0, simplifying access to them. The memory-mapped access provides a convenient way to save and restore the registers for context switches and to transfer information between the accumulators and the other registers	Understand	CO 2	CLO 5	AEC507.05
28	Define the Carry Bit	The ALU has an associated carry bit © that is affected by most arithmetic ALU instructions, including rotate and shift operations. It supports efficient computation of extended-precision arithmetic operations. Two conditional operands, C and NC, enable branching, calling, returning, and conditionally executing according to the status (set or cleared) of the carry bit	Understand	CO 2	CLO 8	AEC507.08
29	Explain about Dual 16-Bit Mode	For arithmetic operations, the ALU can operate in a special dual 16-bit arithmetic mode that performs two 16-bit operations (for instance, two additions or two subtractions) in one cycle. You can select this mode by setting the C16 field of ST1	Understand	CO 2	CLO 6	AEC507.06

S.No	QUESTION	ANSWER	BLOOMS TAXONOMY LEVEL	CO	CLO	CLO Code
30	Define Timer	The on-chip timer is a software-programmable timer that consists of three registers and can be used to periodically generate interrupts.	Understand	CO 2	CLO 7	AEC507.07
UNIT – III OVERVIEW OF TMS315C54XX PROCESSOR						
1	What is the architecture used in 54x DSPs?	The ’54x DSPs use an advanced, modified Harvard architecture that maximizes processing power by maintaining one program memory bus and three data memory buses. Separate program and data spaces allow simultaneous access to program instructions and data, providing the high degree of parallelism.	Understand	CO 3	CLO 13	AEC507.13
2	List the blocks of CPU of 54x DSPs?	The CPU of the ’54x devices contains: • A 40-bit arithmetic logic unit (ALU) • Two 40-bit accumulators • A barrel shifter • A 17 × 17-bit multiplier/adder • A compare, select, and store unit (CSSU)	Understand	CO 3	CLO 10	AEC507.10
3	What are the functions of ALU	The ’54x devices perform 2s-complement arithmetic using a 40-bit ALU and two 40-bit accumulators (ACCA and ACCB). The ALU also can perform Boolean operations. The ALU can function as two 16-bit ALUs and perform two 16-bit operations simultaneously when the C16 bit in status register 1 (ST1) is set.	Understand	CO 3	CLO 11	AEC507.11
4	Name the interrupt registers of 54x DSPs?	The interrupt-mask register (IMR) is used to mask off specific interrupts individually at required times. The interrupt-flag register (IFR) indicates the current status of the interrupts.	Understand	CO 3	CLO 12	AEC507.12
5	Define PMST.	The processor-mode status register (PMST) controls memory configurations of the ’54x devices.	Remember	CO 3	CLO 9	AEC507.09
6	What is the function of program control?	The program controller decodes instructions, manages the pipeline, stores the status of operations, and decodes conditional operations. Some of the hardware elements included in the program controller are the program counter, the status and control register, the stack, and the address-generation logic. Some of the software mechanisms used for program control include branches, calls, conditional instructions, a repeat instruction, reset, and interrupts. The ’54x supports both the use of hardware and software interrupts for program control.	Understand	CO 3	CLO 10	AEC507.10
7	Define Status Registers.	The status registers, ST0 and ST1, contain the status of the various conditions and modes for the ’54x devices.	Understand	CO 3	CLO 11	AEC507.11

S.No	QUESTION	ANSWER	BLOOMS TAXONOMY LEVEL	CO	CLO	CLO Code
8	Define TREG.	The TREG is used to hold one of the multiplicands for multiply and multiply/accumulate instructions. It can hold a dynamic (execution-time programmable) shift count for instructions with a shift operation such as ADD, LD, and SUB. It also can hold a dynamic bit address for the BITT instruction. The EXP instruction stores the exponent value computed into the TREG, while the NORM instruction uses the TREG value to normalize the number. For ACS operation of Viterbi decoding, TREG holds branch metrics used by the DADST and DSADT instructions.	Understand	CO 3	CLO 12	AEC507.12
9	What are the power down modes?	There are three power-down modes, activated by the IDLE1, IDLE2, and IDLE3 instructions. In these modes, the '54x devices enter a dormant state and dissipate considerably less power than in normal operation. The IDLE1 instruction is used to shut down the CPU. The IDLE2 instruction is used to shut down the CPU and on-chip peripherals. The IDLE3 instruction is used to shut down the '54x processor completely. This instruction stops the PLL circuitry as well as the CPU and peripherals.	Remember	CO 3	CLO 10	AEC507.10
10	What is the minimum memory address range for 54x devices?	The minimum memory address range for the '54x devices is 192K words — composed of 64K words in program space, 64K words in data space, and 64K words in I/O space. Selected devices also provide extended program memory space of up to 8M words. The program memory space contains the instructions to be executed as well as tables used in execution. The data memory space stores data used by the instructions. The I/O memory space interfaces to external memory-mapped peripherals and can also serve as extra data storage space	Remember	CO 3	CLO 11	AEC507.11
11	What is the function of boot loader?	A boot loader is available in the standard '54x on-chip ROM. This boot loader can be used to transfer user code from an external source to anywhere in the program memory at power up automatically	Understand	CO 3	CLO 12	AEC507.12
12	Define DARAM?	Dual-access RAM blocks can be accessed twice per machine cycle. This memory is intended primarily to store data values; however, it can be used to store program as well. At reset, the DARAM is mapped into data memory space	Understand	CO 3	CLO 11	AEC507.11

S.No	QUESTION	ANSWER	BLOOMS TAXONOMY LEVEL	CO	CLO	CLO Code
13	Define SARAM?	Each of the SARAM blocks is a single-access memory. This memory is intended primarily to store data values; however, it can be used to store program as well.	Understand	CO 3	CLO 13	AEC507.13
14	What is On-Chip Two-Way Shared RAM?	Select 54x devices with multiple CPU cores include two-way shared RAM blocks that allow simultaneous program space access from two CPU cores. Each CPU can perform a single access with zero-states to any location in the two-way shared RAM during each clock cycle.	Understand	CO 3	CLO 12	AEC507.12
15	What is On-Chip Memory Security?	A security feature is included on 54x devices to prevent the on-chip memory contents from being extracted by a user. This feature is enabled during the manufacturing process and is ONLY available to customers that order custom ROM programming. Consequently, memory security cannot be enabled/disabled by the user.	Remember	CO 3	CLO 11	AEC507.11
16	Define Emulation access?	The security feature completely disables the scan-based emulation capability of the ’54x to prevent the use of a debugger utility. Note that this only affects emulation, and does not prevent the use of the JTAG boundary scan test capability.	Understand	CO 3	CLO 13	AEC507.13
17	Define HPI access?	On select devices, HPI accesses are restricted when the security feature is enabled.	Understand	CO 3	CLO 13	AEC507.13
18	CPU access	The security feature prohibits the DSP CPU from accessing the on-chip memory. There are two levels of security associated with CPU accesses.	Understand	CO 3	CLO 13	AEC507.13
19	Define Bus Structure.	The ’54x device architecture is built around eight major 16-bit buses: One program-read bus (PB) which carries the instruction code and immediate operands from program memory.Two data-read buses (CB, DB) and one data-write bus (EB), which interconnect to various elements, such as the CPU. The CB and DB carry the operands read from data memory.The EB carries the data to be written to memory. Four address buses (PAB, CAB, DAB, and EAB), which carry the addresses needed for instruction execution	Understand	CO 3	CLO 12	AEC507.12

S.No	QUESTION	ANSWER	BLOOMS TAXONOMY LEVEL	CO	CLO	CLO Code
15	Need for Software-Programmable Wait-State Generators	The software-programmable wait-state generator can be used to extend external bus cycles to interface with slower off-chip memory and I/O devices. The software wait-state generator is incorporated without any external hardware.	Understand	CO 3	CLO 12	AEC507.12
21	Define The clock generator	The clock generator on the C54x devices consists of an internal oscillator and a phase locked loop (PLL) circuit. Currently, there are two different types of PLL circuits on C54x devices.	Understand	CO 3	CLO 10	AEC507.10
22	What is the purpose of Programmable Bank-Switching	Programmable bank-switching can be used to insert one cycle automatically when crossing memory-bank boundaries inside program memory or data memory space. One cycle can also be inserted when crossing from program-memory space to data-memory space ('54x) or from one program memory page to another program memory page on selected devices.	Understand	CO 3	CLO 12	AEC507.12
23	Define Direct Memory Access (DMA) Controller	The '54x direct memory access (DMA) controller transfers data between points in the memory map without intervention by the CPU. The DMA allows movements of data to and from internal program/data memory, internal peripherals (such as the McBSPs), or external memory devices to occur in the background of CPU operation.	Remember	CO 3	CLO 11	AEC507.11
24	Define DMA Memory Map	The DMA memory map includes access to on-chip memory on all devices and access to external memory on selected devices. The DMA memory map for on-chip memory is unaffected by the state of the memory control bits: MP/MC, DROM, and OVLY. For specific information on DMA implementations and memory maps, see the device-specific data sheets.	Understand	CO 3	CLO 13	AEC507.13
25	Define DMA Priority Level	Each DMA channel can be independently assigned high or low priority relative to each other. Multiple DMA channels that are assigned to the same priority level are handled in a round-robin manner.	Understand	CO 3	CLO 13	AEC507.13
26	Define Hardware PLL	There are two types of hardware PLL providing different sets of multiplication factors. The option-one hardware PLL provides divide-by-two operation and multiplication factors of 1, 1.5, 2, or 3. The option-two hardware PLL provides divide-by-two operation and multiplication factors of 1, 4, 4.5, or 5.	Understand	CO 3	CLO 9	AEC507.09

S.No	QUESTION	ANSWER	BLOOMS TAXONOMY LEVEL	CO	CLO	CLO Code
27	Define Software PLL	The software PLL is programmable and the clock multiplication factor can be changed under software control. The initial clock mode setting is determined by the state of the clock mode pins and then the PLL can be programmed to change the clock mode. The software PLL provides multiplication factors ranging from 0.25 to 16.	Understand	CO 3	CLO 9	AEC507.09
28	LAMM-	load accumulator with memory mapped register	Understand	CO 3	CLO 10	AEC507.10
29	SAMM	store accumulator in memory mapped register	Remember	CO 3	CLO 11	AEC507.11
30	Define on-chip ROM	The on-chip ROM is part of the program memory space and, in some cases, part of the data memory space.	Understand	CO 3	CLO 12	AEC507.12
UNIT – IV INTERFACING MEMORY AND I/O PERIPHERALS TO PDSPs						
1	Define interrupts?	An interrupt is a signal sent to the processor that interrupts the current process. It may be generated by a hardware device or a software program.	Understand	CO 4	CLO 14	AEC507.14
2	How is fast data access achieved in Digital Signal Processors	In DSP the fast data access is achieved by high bandwidth memory architecture like modified Harvard architecture, specialized addressing modes like circular and bit reversal addressing and DMA	Understand	CO 4	CLO 14	AEC507.14
3	What is modified Harvard architecture employed in DSP	The modified Harvard architecture employed in DSP's will have 2 or more internal memory blocks connected to CPU by separate buses. One memory block is reserved for code and data and the other block only for data.	Remember	CO 4	CLO 15	AEC507.15
4	List two special addressing modes in DSP.	Circular and bit reversal addressing modes.	Remember	CO 4	CLO 15	AEC507.15
5	What are the Special features of DSP's	• Fast data access • Fast computation • Fast execution control • Numerical fidelity	Understand	CO 4	CLO 15	AEC507.15
6	How is fast computation achieved in DSP's?	The fast computation in DSP's are achieved by providing single cycle MAC unit, pipelining of instruction execution.	Understand	CO 4	CLO 17	AEC507.17
7	What is MAC unit?	The MAC unit in DSP's is capable of performing multiply, add operations involved in convolution and correlation.	Understand	CO 4	CLO 15	AEC507.15
8	What is pipelining in DSP's?	The pipelining refers to overlapping of execution of various phases of different instructions so that a number of instructions can be executed in parallel.	Understand	CO 4	CLO 16	AEC507.16
9	What are the functional unitsof TMS315C54X?	Parallel logic unit, central ALU, Memory mapped registers, Auxiliary registers, and Arithmetic unit	Understand	CO 4	CLO 16	AEC507.16

S.No	QUESTION	ANSWER	BLOOMS TAXONOMY LEVEL	CO	CLO	CLO Code
10	What are the advantages of DMA	• DMA speedups the memory operations by bypassing the involvement of the CPU. • The work overload on the CPU decreases. • For each transfer, only a few numbers of clock cycles are required	Understand	CO 4	CLO 15	AEC507.15
11	Define Exponent Encoder	The exponent encoder is an application-specific hardware device dedicated to supporting the EXP instructions in a single cycle. With the EXP instruction, the exponent value in the accumulator can be stored in T as a 2s-complement value within a -8 through 31range	Understand	CO 4	CLO 14	AEC507.14
12	What are the disadvantages of DMA	• Cache coherence problem can be seen when DMA is used for data transfer. • Increases the price of the system.	Understand	CO 4	CLO 15	AEC507.15
13	What is Serial Interface	The serial interface acts as a communication interface between two digital systems that sends data as a series of voltage pulses over a wire.	Remember	CO 4	CLO 16	AEC507.16
14	What is Parallel Interface	A parallel interface transmits multiple bits simultaneously using different wires.	Understand	CO 4	CLO 16	AEC507.16
15	Define Fetch unit	The processor fetches (reads from memory) an instruction and then, depending on the instruction, executes it (takes some further action with it, such as shifting bits to the right or left). Then it fetches the next instruction, and so forth.	Remember	CO 4	CLO 15	AEC507.15
16	Define Execute unit	An execution unit (also called a functional unit) is a part of the central processing unit (CPU) that performs the operations and calculations as instructed by the computer program.	Understand	CO 4	CLO 14	AEC507.14
17	Define Decode unit	A decode unit is a piece of logic that is presented with a sequence of bits, that have been fetched from memory, and prepares the execution of one or more instructions in accordance with the instruction set architecture of a processor	Understand	CO 4	CLO 16	AEC507.16
18	Define a register	A register is a temporary storage area built into a CPU. Some registers are used internally and cannot be accessed outside the processor, while others are user-accessible.	Understand	CO 4	CLO 15	AEC507.15
19	Define Flag	A flag is a value that acts as a signal for a function or process. The value of the flag is used to determine the next step of a program. Flags are often binary flags, which contain a boolean value (true or false).	Understand	CO 4	CLO 14	AEC507.14
20	Define Interrupt Flag Register	The Interrupt flag (IF) is a system flag bit in the architecture's FLAGS register which determines whether or not the central processing unit (CPU) will handle maskable hardware interrupts	Understand	CO 4	CLO 14	AEC507.14

S.No	QUESTION	ANSWER	BLOOMS TAXONOMY LEVEL	CO	CLO	CLO Code
21	Define Interrupt Mask Register	An internal switch setting that controls whether an interrupt can be processed or not. The mask is a bit that is turned on and off by the program.	Understand	CO 4	CLO 15	AEC507.15
22	Write the Status and control registers	The C54x DSP has three status and control registers: I. Status register 0 (ST0), II. Status register 1 (ST1). III. Processor mode status register (PMST).	Understand	CO 4	CLO 16	AEC507.16
24	Define On-Chip Two-Way Shared RAM	The devices with multiple CPU cores include two-way shared RAM Blocks. All the shared memory is program write-protected or read only by the CPU, only the DMA controller can write to the shared memory. This shared RAM is most efficiently used when the two CPUs are executing identical programs.	Understand	CO 4	CLO 16	AEC507.16
UNIT – V IMPLEMENTATIONS OF BASIC DSP ALGORITHMS						
1	What is the need for multirate signal processing?	In real time data communication we may require more than one sampling rate for processing data in such a cases we go for multi-rate signal processing which increase and/or decrease the sampling rate.	Understand	CO 5	CLO 17	AEC507.17
2	What is meant by aliasing?	The original shape of the signal is lost due to under sampling.	Remember	CO 5	CLO 18	AEC507.18
3	How can aliasing be avoided?	Placing a LPF before down sampling	Remember	CO 5	CLO 19	AEC507.19
4	How can sampling rate be converted by a factor I/D.	Cascade connection of interpolator and decimator	Remember	CO 5	CLO 19	AEC507.19
5	What is meant by sub-band coding?	It is an efficient coding technique by allocating lesser bits for high frequency signals and more bits for low frequency signals.	Remember	CO 5	CLO 19	AEC507.19
6	What is meant by up sampling?	Increasing the sampling rate	Remember	CO 5	CLO 19	AEC507.19
7	What is meant by down sampling?	Decreasing the sampling rate.	Remember	CO 5	CLO 18	AEC507.18
8	What is meant by decimator?	Down sampling and a anti-aliasing filter.	Remember	CO 5	CLO 19	AEC507.19
9	What is meant by interpolator?	An anti-imaging filters and Up sampling.	Remember	CO 5	CLO 19	AEC507.19
10	What is meant by sampling rate conversion?	Changing one sampling rate to other sampling rate is called sampling rate conversion.	Remember	CO 5	CLO 19	AEC507.19

S.No	QUESTION	ANSWER	BLOOMS TAXONOMY LEVEL	CO	CLO	CLO Code
11	Define mean	Mxn=E[xn]=intg xpxn(x,n) dx	Remember	CO 5	CLO 20	AEC507.20
12	Define DFT	It is a popular form of the FFT algorithm. In this the output sequence X(k) is divided into smaller and smaller sub-sequences , that is why the name Decimation In Frequency	Remember	CO 5	CLO 18	AEC507.18
13	Define variance.	Zxn2=E[{xn=mxn}2]	Remember	CO 5	CLO 18	AEC507.18
14	Define cross correlation of random process	R xy (n.m)= intxy*pxn,ym(x,n,y,m)dxdy. cross-correlation is a measure of similarity of two series as a function of the displacement of one relative to the other. This is also known as a sliding dot product or sliding inner-product.	Remember	CO 5	CLO 18	AEC507.18
15	Define DTFT of cross correlation	Txy(e jw) = x rxy(l) e jwl	Remember	CO 5	CLO 19	AEC507.19
16	What is the cutoff frequency of Decimator?	Pi/M where M is the down sampling factor	Remember	CO 5	CLO 19	AEC507.19
17	What is the cutoff frequency of Interpolator?	Pi/L where L is the UP sampling factor	Remember	CO 5	CLO 20	AEC507.20
18	Define Decimation	The Decrease in the Sampling Rate are termed as decimation or Down sampling. The No. of Samples per Cycle is reduced to M-1 no. of terms	Remember	CO 5	CLO 20	AEC507. 20
19	Define Interpolation	The Increase in the Sampling rate is termed as Interpolation or Up sampling. The No. of Samples per Cycle is increased to L-1 No. of terms	Remember	CO 5	CLO 19	AEC507.19
15	Define Filter	Electronic filters are electrical circuits which perform signal processing functions, specifically to remove unwanted frequency components from the signal	Remember	CO 5	CLO 18	AEC507.18
21	Define FIR Filter	A finite impulse response (FIR) filter is a filter structure that can be used to implement almost any sort of frequency response digitally.	Remember	CO 5	CLO 18	AEC507.18
22	Define IIR Filter	An infinite impulse response (IIR) filter is a digital filter that depends linearly on a finite number of input samples and a finite number of previous filter outputs	Remember	CO 5	CLO 18	AEC507.18
23	Define FFT	The Fast Fourier Transform is an algorithm used to compute the DFT. It makes use of the symmetry and periodicity properties of twiddle factor to effectively reduce the DFT computation time. It is based on the fundamental principle of decomposing the computation of DFT of a sequence of length N into successively smaller DFTs.	Understand	CO 5	CLO 18	AEC507.18

S.No	QUESTION	ANSWER	BLOOMS TAXONOMY LEVEL	CO	CLO	CLO Code
24	Define DIT-FFT	Decimation-In-Time algorithm is used to calculate the DFT of a N point sequence. The idea is to break the N point sequence into two sequences, the DFTs of which can be combined to give the DFT of the original N point sequence	Remember	CO 5	CLO 18	AEC507.18
25	Define DFT-FFT	It is a popular form of the FFT algorithm. In this the output sequence X(k) is divided into smaller and smaller sub-sequences , that is why the name Decimation In Frequency.	Remember	CO 5	CLO 18	AEC507.18
26	Define Correlation	Correlation computes a measure of similarity of two input signals as they are shifted by one another.	Understand	CO 5	CLO 19	AEC507.19
27	What is meant by radix -2?	FFT is most efficient algorithm to compute DFT. if number of output points N can be expressed as power of 2 .	Remember	CO 5	CLO 18	AEC507.18
28	Define Cross Correlation	In signal processing, cross-correlation is a measure of similarity of two series as a function of the displacement of one relative to the other.	Understand	CO 5	CLO 19	AEC507.19
29	Define Auto Correlation	Autocorrelation can also be referred to as lagged correlation or serial correlation, as it measures the relationship between a variable's current value and its past values.	Remember	CO 5	CLO 18	AEC507.18
30	How many complex multiplications and additions are involved in butterfly computation?	One complex multiplication and two complex additions are required in butterfly computation	Remember	CO 5	CLO 18	AEC507.18

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