

## DIGITAL LOGIC DESIGN

<b>III Semester: CSE / IT</b>																				
Course Code	Category	Hours / Week			Credit	Maximum Marks														
AEC020	Foundation	L	T	P	C	CIA	SEE	Total												
		3	1	-	4	30	70	100												
<b>Contact Classes: 45</b>		<b>Tutorial Classes: 15</b>		<b>Practical Classes: Nil</b>		<b>Total Classes: 60</b>														
<p><b>I. COURSE OVERVIEW:</b>                      This course intended to logic gates, various logic families. Design of digital circuits using logic gates, combinational circuits and sequential circuits. Apply op-amp characteristics to design analog to digital converters and digital to analog converters. Classification and characteristics of memories such as Read-only memory, Random access memory and programmable logic devices such as programmable logic array and programmable array logic.</p> <p><b>II. OBJECTIVES:</b>  <b>The course should enable the students to:</b></p> <ul style="list-style-type: none"> <li>I Simplification of the logic functions using Boolean algebraic theorems and techniques.</li> <li>II Implementation of conventional combinational and sequential circuits including conversions of flip-flops</li> <li>III The exploration of the logic families and semiconductor memories.</li> </ul> <p><b>III. COURSE OUTCOMES:</b>  <b>After successful completion of the course, students should be able to:</b></p> <ul style="list-style-type: none"> <li>CO 1 <b>Understand</b> the different forms of number representations and binary codes in digital logic circuits. Understand</li> <li>CO 2 <b>Make use of</b> Boolean postulates, theorems and k-map for obtaining minimized Boolean expressions. Remember</li> <li>CO 3 <b>Implement</b> the combinational logic circuits using the logic gates. Apply</li> <li>CO 4 <b>Utilize</b> the functionality and characteristics of flip-flops and latches for designing sequential circuits. Apply</li> <li>CO 5 <b>Construct</b> the synchronous and asynchronous modules using flip flops used for memory storing applications. Apply</li> <li>CO 6 <b>Extend</b> the knowledge of memories and programmable logic devices for understanding the architectural blocks of FPGA. Apply</li> </ul> <p><b>IV. SYLLABUS:</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%; text-align: center; color: blue;"><b>UNIT-I</b></td> <td style="text-align: center; color: blue;"><b>NUMBERS SYSTEMS AND CODES</b></td> <td style="text-align: right; color: blue;"><b>Classes: 09</b></td> </tr> <tr> <td colspan="3" style="padding: 5px;">Review of number systems, number base conversion; Binary arithmetic: Binary weighted and non-weighted codes; Complements: Signed binary numbers; Error detection and correcting codes; Binary logic.</td> </tr> <tr> <td style="text-align: center; color: blue;"><b>UNIT-II</b></td> <td style="text-align: center; color: blue;"><b>BOOLEAN ALGEBRA AND GATE LEVEL MINIMIZATION</b></td> <td style="text-align: right; color: blue;"><b>Classes: 09</b></td> </tr> <tr> <td colspan="3" style="padding: 5px;">Postulates and theorems; representation of switching functions; SOP and POS forms; Canonical forms; Digital logic gates; Karnaugh Maps: Minimization using three variable; four variable; five variable K-Maps; Don't Care Conditions; NAND and NOR implementation; Other Two-level implementation; Exclusive –OR function.</td> </tr> </table>									<b>UNIT-I</b>	<b>NUMBERS SYSTEMS AND CODES</b>	<b>Classes: 09</b>	Review of number systems, number base conversion; Binary arithmetic: Binary weighted and non-weighted codes; Complements: Signed binary numbers; Error detection and correcting codes; Binary logic.			<b>UNIT-II</b>	<b>BOOLEAN ALGEBRA AND GATE LEVEL MINIMIZATION</b>	<b>Classes: 09</b>	Postulates and theorems; representation of switching functions; SOP and POS forms; Canonical forms; Digital logic gates; Karnaugh Maps: Minimization using three variable; four variable; five variable K-Maps; Don't Care Conditions; NAND and NOR implementation; Other Two-level implementation; Exclusive –OR function.		
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<b>UNIT-III</b>	<b>DESIGN OF COMBINATIONAL CIRCUITS</b>	<b>Classes: 09</b>
Combinational circuits: Analysis and design procedure; Binary adder and subtractors; Carry look-ahead adder; Binary multiplier. Magnitude comparator; BCD adder; Decoders; Encoders; Multiplexers; Demultiplexer.		
<b>UNIT-IV</b>	<b>DESIGN OF SEQUENTIAL CIRCUITS</b>	<b>Classes: 10</b>
Combinational vs sequential circuits ; Latches, flip flops: RS flip flop, JK flip flop, T flip flop, D flip flop, Master-Slave flip flop, flip flops excitation functions; Conversion of one flip flop to another flip flop; Shift registers; Design of asynchronous and synchronous circuits; State table, state diagram, state reduction and state assignment for mealy and moore machines.		
<b>UNIT-V</b>	<b>MEMORY</b>	<b>Classes: 08</b>
Random access memory; Types of ROM; Memory decoding; Address and data bus; Sequential memory; Cache memory; Programmable logic arrays; Memory hierarchy in terms of capacity and access time.		
<b>Text Book:</b>		
1. M. Morris Mano, "Digital Design", Pearson Education/PHI, 3 <sup>rd</sup> Edition, 2001.		
<b>Reference Books:</b>		
<ol style="list-style-type: none"> <li>1. Charles H. Roth Jr, "Fundamentals of Logic Design", Thomson Brooks/Cole, 5<sup>th</sup> Edition, 2004.</li> <li>2. C. V. S. Rao, "Switching Theory and Logic Design, Pearson Education, 1<sup>st</sup> Edition, 2005.</li> <li>3. M. Rafiquzzaman, "Fundamentals of Digital Logic and Micro Computer Design", John Wiley, 5<sup>th</sup> Edition, 2005.</li> <li>4. Zvi. Kohavi, "Switching and Finite Automata Theory", Tata McGraw Hill, 2<sup>nd</sup> Edition, 1991.</li> </ol>		
<b>Web References:</b>		
<ol style="list-style-type: none"> <li>1. <a href="http://www.american.cs.ucdavis.edu/academic/ecs154a.sum14/postscript/cosc205.pdf">http://www.american.cs.ucdavis.edu/academic/ecs154a.sum14/postscript/cosc205.pdf</a></li> <li>2. <a href="http://www.engr.cs.com/courses/engr250/engr250lecture.pdf">http://www.engr.cs.com/courses/engr250/engr250lecture.pdf</a></li> <li>3. <a href="http://www.ece.rutgers.edu/~marsic/Teaching/DLD/slides/lec-1.pdf">http://www.ece.rutgers.edu/~marsic/Teaching/DLD/slides/lec-1.pdf</a></li> <li>4. <a href="http://www.iare.ac.in">http://www.iare.ac.in</a></li> </ol>		
<b>E-Text Books :</b>		
<ol style="list-style-type: none"> <li>1. <a href="https://drive.google.com/file/d/0B4ChICvNGHIfN2NmODE1NjAtZWl5Zi00MmU0LWIyMmQtOTU3ZGUyMzAwODc1/view">https://drive.google.com/file/d/0B4ChICvNGHIfN2NmODE1NjAtZWl5Zi00MmU0LWIyMmQtOTU3ZGUyMzAwODc1/view</a></li> <li>2. <a href="https://accessengineeringlibrary.com/browse/digital-logic-design-and-computer-organization-with-computer-architecture-for-security">https://accessengineeringlibrary.com/browse/digital-logic-design-and-computer-organization-with-computer-architecture-for-security</a></li> <li>3. <a href="http://www.ece.rutgers.edu/~marsic/Teaching/DLD/syllabus.html">http://www.ece.rutgers.edu/~marsic/Teaching/DLD/syllabus.html</a></li> </ol>		
<b>Course Home Page:</b>		