VLSI DESIGN LABORATORY

VII Semester: ECE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
AEC112	Core	-	-	3	2	30	70	100
Contact Classes: Nil	Total Tutorials: Nil	Total Practical Classes: 36				Total Classes: 36		

I. COURSE OVERVIEW:

The art of VLSI circuit design is dynamic with advances in process technology and innovations in the electronic design automation (EDA) industry. The objective of this laboratory course is to demonstrate the various stages in VLSI design flow using cadence software. Hands on training on logic and circuit simulations of MOSFETS, ring oscillators, multiplexers, analog amplifiers etc are included. The course also covers physical layout of complex logic gates for chip design.

II. OBJECTIVES:

The course should enable the students to:

- **I** Modern tools for functional level to physical layout with verification at intermediate stages in the VLSI design flow in top-down approach.
- **II** Design and simulations of analog, digital and mixed circuits for optimum values of area over head, power and time delay.
- **III** The Chip design through a practical approach using advanced modern tools such as vivado and cadence for front end & back end.

III. COURSE OUTCOMES:

After successful completion of the course, students should be able to:

CO 1	**Calculate** the static, dynamic and noise margin parameters of CMOS inverter using the output and transfer characteristics of MOSFETs.	Apply
CO 2	**Analyze** complex gates, switch logic and transmission gates for performance optimization of distortion, power consumption and circuit delays.	Analyze
CO 3	**Build** 4 X 1 multiplexer and ring oscillator using multiplexer & inverter circuit symbols with necessary inter connections.	Apply
CO 4	**Examine** the conditions for optimum performance of latches and registers with the knowledge of digital system design.	Analyze
CO 5	**Calculate** bandwidth, gain, and common mode rejection ratio parameters for differential, MOSFET and casode amplifiers.	Apply
CO 6	**Build** the stick diagrams, layouts of MOS circuits using design rule checks (DRC) and verification.	Apply

IV. SYLLABUS:

LIST OF EXPERIMENTS

Week-1	**MOSFET**

To plot the (i) output characteristics
(ii) Transfer characteristics of an n-channel and p-channel MOSFET.

Week-2	**CMOS INVERTER**

To design and plot the static (VTC) and dynamic characteristics of a digital CMOS inverter.

Week-3	**RING OSCILLATOR**

To design and plot the output characteristics of a 3-inverter ring oscillator.

Week-4	**LOGIC GATES**
To design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS technology.	
Week-5	**4X1 MULTIPLEXER**
To design and plot the characteristics of a 4x1 digital multiplexer using pass transistor logic.	
Week-6	**LATCHES**
To design and plot the characteristics of a positive and negative latch based on multiplexers.	
Week-7	**REGISTERS**
To design and plot the characteristics of a master-slave positive and negative edge triggered registers based on multiplexers.	
Week-8	**DIFFERENTIAL AMPLIFIER**
Design and simulation of a simple 5 transistor differential amplifier. Measure gain, ICMR, and CMRR.	
Week-9	**NMOS INVERTER AND CMOS INVERTER**
To design layout of NMOS and CMOS inverter.	
Week-10	**LAYOUT OF 2-INPUT NAND, NOR GATES**
To design the layout of 2-input NAND, NOR gates.	
Week-11	**COMMON SOURCE AMPLIFIER**
Analysis of Frequency response of Common source amplifiers.	
Week-12	**COMMON DRAIN AMPLIFIER**
Analysis of Frequency response of Common drain amplifiers.	
Week-13	**SINGLE STAGE CASCODE AMPLIFIER**
Design and Simulation of Single Stage Cascode Amplifier.	
Week-14	**BASIC CURRENT MIRROR, CASCODE CURRENT MIRROR AMPLIFIER**
Design and Simulation of Basic Current Mirror, Cascode Current Mirror Amplifier.	

Reference Books

1. Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw Hill Publications, 2002.
2. Allen Holberg, CMOS Analog Circuit Design, Oxford Publications, 2002.
3. Baker, Li, Boyce, CMOS Mixed Circuit Design, Wiley Publications, 2002.

Web References:

1. http://iitg.vlab.co.in/?sub=59&brch=165

Course Home Page:

SOFTWARE AND HARDWARE REQUIREMENTS FOR 36 STUDENTS

HARDWARE: Desktop Computer Systems 36 nos

SOFTWARE: Cadence tools