

## MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSING

<b>I Semester: ES</b>																																						
Course code	Category	Hours / Week			Credits	Maximum Marks																																
		L	T	P	C	CIA	SEE	Total																														
BESB02	Core	3	-	-	3	30	70	100																														
<b>Contact Classes: 45</b>		<b>Tutorial Classes: Nil</b>		<b>Practical Classes: Nil</b>			<b>Total Classes: 45</b>																															
<p><b>I. COURSE OVERVIEW:</b>                  This course is intended to provide fundamentals of ARM Cortex-M3 Processor and LPC 17XX Micro- controller architectures and their features. It includes the architectures of the Cortex-M3, instruction set summary, Programmable DSP processor. It is used in the applications of microcontrollers pro- gramming models and programmable digital signal processors.</p> <p><b>II. COURSE OBJECTIVES:</b>  <b>The students will try to learn:</b></p> <ol style="list-style-type: none"> <li>I. Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.</li> <li>II. Identify and characterize architecture of Programmable DSP Processors</li> <li>III. Develop small applications by utilizing the ARM processor core and DSP processor based platform.</li> </ol> <p><b>III. COURSE OUTCOMES:</b>  <b>After successful completion of the course, students should be able to:</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 10%;">CO 1</td> <td style="width: 70%;">Illustrate the Internal architecture and memory operations of ARM Cortex M3 processor for interfacing microprocessor applications</td> <td style="width: 20%;">Understand</td> </tr> <tr> <td>CO 2</td> <td>Analyze Exceptions handler mechanism to minimize interrupt latency using Nested Vectored Interrupt Controller</td> <td>Analyze</td> </tr> <tr> <td>CO 3</td> <td>Construct the high level of integration in embedded applications using LPC 17XX Microcontroller</td> <td>Apply</td> </tr> <tr> <td>CO 4</td> <td>Demonstrate various computational building blocks of programmable DSP architectures using interfacing of memory and I/O peripherals</td> <td>Understand</td> </tr> <tr> <td>CO 5</td> <td>Identify the CPU architecture, peripherals, and development tools for the TMS320C6000 digital signal processors</td> <td>Apply</td> </tr> <tr> <td>CO 6</td> <td>Develop the application for digital signal processing using code composer studio tool</td> <td>Apply</td> </tr> </table> <p><b>IV. SYLLABUS:</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 15%;"><b>UNIT-I</b></td> <td style="width: 60%;"><b>ARM CORTEX-M3 PROCESSOR</b></td> <td style="width: 25%; text-align: right;"><b>Classes: 09</b></td> </tr> <tr> <td colspan="3">                     ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.                 </td> </tr> <tr> <td><b>UNIT-II</b></td> <td><b>EXCEPTIONS AND INTERRUPT</b></td> <td style="text-align: right;"><b>Classes: 09</b></td> </tr> <tr> <td colspan="3">                     Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.                 </td> </tr> </table>									CO 1	Illustrate the Internal architecture and memory operations of ARM Cortex M3 processor for interfacing microprocessor applications	Understand	CO 2	Analyze Exceptions handler mechanism to minimize interrupt latency using Nested Vectored Interrupt Controller	Analyze	CO 3	Construct the high level of integration in embedded applications using LPC 17XX Microcontroller	Apply	CO 4	Demonstrate various computational building blocks of programmable DSP architectures using interfacing of memory and I/O peripherals	Understand	CO 5	Identify the CPU architecture, peripherals, and development tools for the TMS320C6000 digital signal processors	Apply	CO 6	Develop the application for digital signal processing using code composer studio tool	Apply	<b>UNIT-I</b>	<b>ARM CORTEX-M3 PROCESSOR</b>	<b>Classes: 09</b>	ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.			<b>UNIT-II</b>	<b>EXCEPTIONS AND INTERRUPT</b>	<b>Classes: 09</b>	Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.		
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<b>UNIT-III</b>	<b>LPC 17XX MICROCONTROLLER</b>	<b>Classes: 09</b>
LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC. UART and other serial interfaces, PWM, RTC, WDT.		
<b>UNIT-IV</b>	<b>PROGRAMMABLE DSP (P-DSP) PROCESSORS</b>	<b>Classes: 09</b>
Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.		
<b>UNIT-V</b>	<b>VLIW ARCHITECTURE</b>	<b>Classes: 09</b>
VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations Code Composer Studio for application development for digital signal processing, On chip peripherals , Processor benchmarking.		
<b>Text Books:</b>		
<ol style="list-style-type: none"> <li>1. Joseph Yiu, “The Definitive Guide to ARM Cortex-M3”, Elsevier, 3<sup>rd</sup> Edition 2014.</li> <li>2. Venkatramani B., Bhaskar M. “Digital Signal Processors: Architecture, Programming and Applications”, TMH, 2<sup>nd</sup> Edition 2011.</li> </ol>		
<b>Reference Books:</b>		
<ol style="list-style-type: none"> <li>1. Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publications,</li> <li>2. Steve furber, “ARM System-on-Chip Architecture”, Pearson Education.</li> <li>3. Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley Publications.</li> </ol>		

## WIRELESS LANS AND PANS

<b>I Semester: ES</b>								
Course Code	Category	Hours / Week			Credits	Maximum Marks		
BESB03	Elective	L	T	P	C	CIA	SEE	Total
		3	-	-	3	30	70	100
<b>Contact Classes: 45</b>		<b>Tutorial Classes: Nil</b>		<b>Practical Classes: Nil</b>			<b>Total Classes: 45</b>	

### I. COURSE OVERVIEW:

This course intended to provide wireless network communication over short distances using radio or infrared signals instead of traditional network cabling. The basic knowledge of the wireless system, IEEE standards, network architecture, and its protocols. It focuses on data transmission among devices such as computers, smartphones, tablets, and personal digital assistant

### II. COURSE OBJECTIVES:

The students will try to learn:

- I. The First and Second Generation Cellular Systems, Cellular Communications from 1G to3G, Wireless 4G systems.
- II. The importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies infrared technology, UHF narrowband technology, Spread Spectrum technology.
- III. The Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem and Reliability.

### III. COURSE OUTCOMES:

After successful completion of the course, students should be able to:

CO 1	<b>Recall</b> the generations of cellular systems for understanding the connectivity of wireless communication networks.	Understand
CO 2	<b>Organize</b> the random-access protocols to decrease collision and avoid crosstalk.	Apply
CO 3	<b>Justify</b> the importance of wireless LANs for connecting different devices through wireless communication to form an area network.	Evaluate
CO 4	<b>Estimate</b> the wireless PANs for interconnecting electronic devices within an individual person's workspace.	Evaluate
CO 5	<b>Analyze</b> the traffic engineering used to carry traffic flows that vary from those chosen automatically by the routing protocol.	Analyze
CO 6	<b>Interpret</b> the wireless networking standards and protocols for wireless transmission approved by IEEE.	Analyze

### IV. SYLLABUS:

<b>UNIT-I</b>	<b>WIRELESS SYSTEM &amp; RANDOM ACCESS PROTOCOLS</b>	<b>Classes: 08</b>
Introduction, First and Second Generation Cellular Systems, Cellular Communications from 1G to3G, Wireless 4G systems, The Wireless Spectrum; Random Access Methods: Pure ALOHA, Slotted ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA).		

<b>UNIT-II</b>	<b>WIRELESS LANS</b>	<b>Classes: 10</b>
Introduction, importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies: Infrared technology, UHF narrowband technology, Spread Spectrum technology.		
<b>UNIT-III</b>	<b>THE IEEE 802.11 STANDARD FOR WIRELESS LANS</b>	<b>Classes: 08</b>
Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem, Reliability, Collision avoidance, Congestion avoidance, Congestion control, Security, The IEEE 802.11e MAC protocol.		
<b>UNIT-IV</b>	<b>WIRELESS PANS</b>	<b>Classes: 10</b>
Introduction, importance of Wireless PANs, The Bluetooth technology: history and applications, technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks, Master-Slave Switch; Bluetooth security; Enhancements to Bluetooth: Bluetooth interference issues, Intra and Inter Piconet scheduling, Bridge selection, Traffic Engineering, QoS and Dynamics Slot Assignment, Scatter net formation.		
<b>UNIT-V</b>	<b>THE IEEE 802.15 WORKING GROUP FOR WPANS</b>	<b>Classes: 09</b>
The IEEE 802.15.3, The IEEE 802.15.4, ZigBee Technology, ZigBee components and network topologies, The IEEE 802.15.4 LR-WPAN Device architecture: Physical Layer, Data Link Layer, The Network Layer, Applications; IEEE 802.15.3a Ultra wideband.		
<b>TEXT BOOKS:</b>		
<ol style="list-style-type: none"> <li>1. Ad Hoc and Sensor Networks - Carlos de Morais Cordeiro and Dharma Prakash Agrawal, World Scientific, 2011.</li> <li>2. Wireless Communications and Networking - Vijay K.Garg, Morgan Kaufmann Publishers, 2009</li> </ol>		
<b>REFERENCE BOOKS:</b>		
<ol style="list-style-type: none"> <li>1. Wireless Networks - Kaveh Pahlaram, Prashant Krishnamurthy, PHI, 2002.</li> <li>2. Wireless Communication- Marks Ciampor, George Olenewa, Cengage Learning, 2007.</li> </ol>		