RISC PROCESSOR ARCHITECTURE AND PROGRAMMING

III Semester: ES

Course code	Category	Hours / Week			Credits	Maximum Marks		
		L	**T**	**P**	**C**	**CIA**	**SEE**	**Total**
BESB23	**Elective**	3	-	-	3	30	70	100

Contact Classes: 45	**Tutorial Classes: Nil**	**Practical Classes: Nil**	**Total Classes: 45**

I. COURSE OVERVIEW:

This course emphasizes on comprehensive treatment of embedded hardware and real time operating systems along with case studies, in tune with the requirements of Industry. It focus on design, construct, program, verify, analyze and troubleshoot ARM assembly and C language programs and supporting hardware. This course enable exposure to ARM architecture and make the students to learn the ARM programming & Thumb programming models.

II. COURSE OBJECTIVES:

The students will try to learn:
I.   The programming model of ARM processor and create and test assembly level programming.
II. The processor architecture and organization.
III. How to create and test C programming for ARM.

III. COURSE OUTCOMES:

After successful completion of the course, students should be able to:

CO1	**Outline the** design philosophy of embedded systems and architecture of ARM for different ARM Processor families	Understand
CO2	**Distinguish** the performance of pipelining and non pipelining environment in a Risc processor	Analyze
CO3	**Discuss** various instruction set and addressing modes for ARM programming	Remember
CO4	**Inspect** aware of the Thumb mode for programming of ARM Processor	Analyze
CO5	**Apply** Architecture, modes of operations, Exceptions to write assembly language program of ARM Processors	Apply
CO 6	**Identify** various types of Processors & Peripherals required to design an RISC processor architecture	Remember

SYLLABUS:

UNIT-I	**ARM ARCHITECTURE**	**Classes: 09**

ARM design philosophy, registers, program status register, instruction pipeline, interrupts and vector table, architecture revision, ARM processor families.

UNIT-II	**ARM PROGRAMMING MODEL – I**	**Classes: 09**

Instruction set: Data processing instructions, addressing modes and branch, load, store instructions, PSR instructions and conditional instructions.

UNIT-III	ARM PROGRAMMING MODEL – II	Classes: 09
Thumb instruction set: Register usage, other branch instructions and data processing instructions. Single register and multi register load, store instructions, stack and software interrupt instructions.		
UNIT-IV	ARM PROGRAMMING	Classes: 09
Simple C programs using function calls, pointers, structures, integer and floating point arithmetic, assembly code using instruction scheduling, register allocation, conditional execution and loops.		
UNIT-V	MEMORY MANAGEMENT	Classes: 09
Cache architecture, polices, flushing and caches, MMU, page tables, translation, access permissions, context switch.		

Text Books:

1. Andrew N. Sloss, Dominic Symes, Chris Wright., "ARM Systems Developer's Guides, Designing & Optimizing System Software," Elsevier, 1st Edition, 2008.

Reference Books:

1. Jonathan W. Valvano – Brookes / Cole, "Embedded Microcomputer Systems, Real Time Interfacing", Thomas Learning, 1st Edition, 1998.

Web References:

1. http://nptel.ac.in/courses/106103068/34
2. http://nptel.ac.in/courses/106103068/35
3. http://nptel.ac.in/courses/106103068/
4. http://nptel.ac.in/courses/106108055/5

E-Text Books:

1. nptel.ac.in/courses/Webcourse-contents/IIT.../comp...risc/1_Intro_risc_Suroj.doc
2. nptel.ac.in/reviewed_pdfs/106102062/lec7.pdf