VLSI DESIGN

VII Semester: ECE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
AECB27	Core	3	-	-	3	30	70	100
Contact Classes: 45	Tutorial Classes: Nil	Practical Classes: Nil				Total Classes: 45		

I. COURSE OVERVIEW:

This course introduces the students the fabrication techniques of design and implementation of very large scale (VLSI) circuits. Specific topics include: CMOS logic, MOSFET theory, design rules & layout procedures and logic and circuit simulations. The course further gives information on data path subsystems, PLD's performance parameters and testing approaches for the circuits.

II. OBJECTIVES:

The course should enable the students to:

I	The aspects of hierarchical VLSI design from the metal oxide semiconductor transistor up to the system level, fabrication and testing.
II	The subsystem design incorporating into a VLSI chip with contemporary techniques for achieving high-speed, low-power and low area overhead.
III	Advanced modern tools such as vivado and cadence for front end and back end forchip design through a practical approach.

III. COURSE OUTCOME:

After successful completion of the course, students should be able to:

CO 1	**Summarize** the MOSFET fabrication process, electrical properties, scaling for analyzing reliability issues and understandinglatest trends in VLSI.	Understand
CO 2	**Develop** the stick diagrams, layouts of MOS circuits using lambda,absolute and Euler physical design rules.	Apply
CO 3	**Describe** inverters, complex gates and dynamic CMOS circuits in terms of power consumption, distortion and speed of operation	Understand
CO 4	**Explain** data path subsystems and array subsystems using stickdiagrams and layouts.	Apply
CO 5	**Outline** the role of Programmable logic devices for realization of complex boolean functions.	Understand
CO 6	**Examine** the test strategies, implementation approach on full custom and semi custom design for speed, cost, reconfiguration and reliability parameters.	Analyze

IV. SYLLABUS:

MODULE-I	INTRODUCTION TO MOS TRANSISTORS	Classes:09

MOS Transistors, CMOS Logic, CMOS Fabrication and Layout, Design Partitioning, Fabrication, Packaging, and Testing, MOS transistor Theory, Long Channel I-V Characteristics, C-V Characteristics, Non-Ideal I-V Effects, DC Transfer Characteristics

MODULE-II	PRINCIPLES OF CIRCUIT DESIGN	Classes:09

CMOS Processing Technology, CMOS Technologies, Layout Design Rules, CMOS Process Enhancements, Technology-Related CAD Issues, Manufacturing Issues, Circuit Simulation, A SPICE Tutorial, Device Models, Device Characterization, Circuit Characterization, Interconnect Simulation. Combinational Circuit Design, Circuit Families, Silicon-On-Insulator Circuit Design, Sub Threshold Circuit Design. Sequential Circuit Design, Circuit Design of Latches and Flip-Flops, Static Sequencing Element Methodology, Sequencing Dynamic Circuits, Synchronizers, Wave Pipelining

MODULE-III	DESIGN METRICS AND SUB SYSTEM DESIGN	Classes: 10
Power, Sources of Power Dissipation, Dynamic Power, Static Power, Energy-Delay Optimization, Low Power Architectures, Robustness, Variability, Reliability, Scaling, Statistical Analysis of Variability, Variation-Tolerant Design. Delay, Transient Response, RC Delay Model, Linear Delay Model, Logical Effort of Paths, Timing Analysis Delay Models, Datapath Subsystems, Addition/Subtraction, One/Zero Detectors, Comparators, Counters, Boolean Logical Operations, Coding, Shifters, Multiplication		
MODULE-IV	**ROBUST DESIGN OF MEMORIES**	**Classes: 09**
Array Subsystems, SRAM, DRAM, Read-Only Memory, Serial Access Memories, Content-Addressable Memory, Programmable Logic Arrays, Robust Memory Design, Special-Purpose Subsystems.		
MODULE-V	**TESTING**	**Classes: 08**
Packaging and Cooling, Power Distribution, Clocks, PLLs and DLLs, I/O, High-Speed Links, Random Circuits, Design Methodology and Tools, Testing, Debugging, and Verification.		

Text Books:

1. Neil H.E. Weste, David Money Harris, "CMOS VLSI Design –A Circuits and Systems Perspective," Addision –Wesley, 2011
2. Jan M Rabey, "Digital Integrated Circuits," 2nd Edition, Pearson Education, 2003.
3. John F.Wakerly, "Digital Design Principles & Practices", 3rd Edition, 2005, PHI/ Pearson Education Asia,

Reference Books:

1. Wang Alice, Calhoun Benton High smith, Chandrakasan Anantha P., "Sub-threshold Design for Ultra Low-Power Systems," Springer 2006
2. Pucknell, Kamran Eshraghian, "Basic VLSI Design," Third Edition, Prentice Hall of India, 2007.
3. R. Jacob Baker, Harry W.LI., David E.Boyee, "CMOS Circuit Design, Layout and Simulation", Wiley-IEEE Press, USA, 2005. ISBN: 978-0-470-88132-3
4. Calhoun, B., C. Schurgers, A. Wang, A. Chandrakasan, "Low Energy Digital Circuit Design," in *Hardware Technology Drivers of Ambient Intelligence*, editors Satyen Mukherjee, 2006 Springer.
5. Park, Synghyun, "Towards Low-Power yet High-Performance Networks-on-Chip," *Ph.D. Thesis*, Massachusetts Institute of Technology, September 2014.
6. Sinangil, Mahmut, "Low-Power and Application-Specific SRAM Design for Energy-Efficient Motion Estimation," *Ph.D. Thesis* Massachusetts Institute of Technology, June 2012
7. Amirtharajah, Rajeevan, "Design of Low Power VLSI Systems Powered by Ambient Mechanical Vibration," *Ph.D. Thesis*, Massachusetts Institute of Technology, May 1999.

Web References:

1 http://dspace.mit.edu/handle/1721.1/93776
2 http://dspace.mit.edu/handle/1721.1/75650
3 https://engineering.purdue.edu/~vlsi/ECE559_Fall09/?_ga=2.120672008.1227662350.1573631317316737531.1573631317
4 Class Notes: http://cobweb.ecn.purdue.edu/~vlsi/ECE559_Fall09

E-Text Books:

1. https://www.springer.com/gp/book/9780387335155
2. http://swarm.cs.pub.ro/~mbarbulescu/SMPA/CMOS-VLSI-design.pdf