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Question Paper Code: BESB02



INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

M.Tech I Semester End Examinations (Regular) - January, 2019

Regulation: IARE-R18

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSING

Time: 3 Hours

(ES)

Max Marks: 70

Answer ONE Question from each Unit

All Questions Carry Equal Marks

All parts of the question must be answered in one place only

UNIT – I

1. (a) State and explain different operating modes of ARM Cortex-M3 processor. [7M]
(b) Explain the Pipelining mechanism in Cortex M3 processor with the help of diagram. [7M]
2. (a) Discuss the various blocks of ARM Cortex-M3 based controller. [7M]
(b) Describe the processor memory map, the behavior of memory accesses, and bit band operation. [7M]

UNIT – II

3. (a) Explain the Interrupt Inputs and Pending behaviour in Cortex M3 processor with the help of timing waveforms. [7M]
(b) Explain with neat diagram the nested vector interrupt controller and its operation with entry and exit. [7M]
4. (a) Explain in detail about the interrupt priority logic. [7M]
(b) Explain the interrupt pending register and interrupt mask register with an example. [7M]

UNIT – III

5. (a) Describe the feature and functionalities of LPC 17XX general purpose I/O (GPIO). [7M]
(b) Explain the features of TIMER in LPC TIMER 17xx microcontroller and mention its applications. [7M]
6. (a) Describe the features and benefits of LPC 17XX Microcontroller. [7M]
(b) Explain the features of PWM in LPC 17xx microcontroller and mention its applications. [7M]

UNIT – IV

7. (a) Briefly describe the Multi port memory of programmable DSP processors. [7M]
(b) With neat diagram explain the Harvard architecture for programmable DSP Processors. [7M]
8. (a) Explain with neat diagram of TI DSP processor family. [7M]
(b) Discuss about MAC unit used in programmable DSP processors. [7M]

UNIT – V

9. (a) Explain the architecture of a typical VLIW processor in detail. [7M]
(b) Describe the architectural details and features of a DSP TMS320C6000 series [7M]
10. (a) Explain the assembly instructions memory addressing of VLIW processor with examples. [7M]
(b) Explain in detail about the on chip peripherals and processor benchmarking. [7M]

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