Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC002

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

B.Tech III Semester End Examinations (Regular) - November, 2018

Regulation: IARE – R16

DIGITAL SYSTEM DESIGN

Time: 3 Hours **(ECE)** **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Add the following binary numbers. **[7M]**
   i) 11011+1101
   ii) 10111.101 + 110111.01
   iii) 1010.11 + 1101.10
   (b) Convert the following numbers from the given base to the other bases indicated. **[7M]**
   i) Decimal 225 to binary, octal
   ii) Octal 623 to decimal, binary

2. (a) The state of a 12-bit register is 010110010111. What is its content if it represents: **[7M]**
   i) three decimal digits in BCD
   ii) three decimal digits in Excess-3 code
   (b) Add the following BCD numbers **[7M]**
   i) 1001 and 0100
   ii) 00010110 and 00010101

UNIT – II

3. (a) Demonstrate the validity of the following identities by means of truth tables. **[7M]**
   i. DeMorgan's Theorem for three variables
   ii. Associative Law
   (b) Simply the following boolean expressions to a minimum number of literals. **[7M]**
   i. xyz + x'y + xyz'
   ii. xyz' + x'yz + xyz + x'yz'

4. (a) Simplify the following Boolean function using, four-variable K-map **[7M]**
   F (A, B ,C, D) = Σm(0,2, 4, 5, 6, 7, 8, 10, 13,15)
   (b) Simplify the following using Quine-McClusky minimization technique. **[7M]**
   $Y = F(A, B, C) = A'B'C' + A'B'C + A'BC + AB'C$

UNIT – III

5. (a) Design a combinational circuit with three inputs x, y, and z and three outputs A, B and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. **[7M]**

   (b) Implement full subtractor using NAND gates. **[7M]**

6. (a) Design a combinational circuit that adds 4-bit number. The circuit can be designed using four full-adders. **[7M]**

   (b) Design a combinational circuit with four inputs that represent a decimal digit in BCD and four outputs that produce the 9's complement of the input digit. **[7M]**

UNIT – IV

7. (a) Explain the operation of MSJK flip-flop using NAND gates. **[7M]**

   (b) Draw the logic diagram of mod 6 ripple counter using T flip-flops. **[7M]**

8. (a) Design a 3 bit binary Up-Down counter with necessary diagrams. **[7M]**

   (b) Design a bi-directional shift register with necessary diagrams. **[7M]**

UNIT – V

9. (a) Explain how the behavior of a clocked synchronous sequential circuit is described by a state table and discuss the method of state table reduction. **[7M]**

   (b) Convert the following Moore machine into corresponding Mealy machine as per given in Table 1. **[7M]**

Table 1

Present state	X=0	X=1	Output
A	D	B	1
B	A	D	0
C	C	C	0
D	B	A	1

10. (a) Design a 1011 sequence detector using JK flip-flop. **[7M]**

    (b) Distinguish Moore and Mealy machines with an example. **[7M]**