Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC002

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

B.Tech III Semester End Examinations (Supplementary) - January, 2019

Regulation: IARE – R16

DIGITAL SYSTEM DESIGN

Time: 3 Hours **(ECE)** **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Discuss binary system, Octal system, Decimal system, Hexa Decimal system of representation. **[7M]**

   (b) Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction **[7M]**
   i) X – Y
   i) Y - X using 2's complement and 1's complement.

2. (a) Convert the following binary number to Gray code **[7M]**
   i) 11000110
   ii) 00011001
   iii) 11110000

   (b) Perform the following addition using Excess-3 code **[7M]**
   i) 0011 0101 0110_2 + 0101 0111 1001_2
   ii) 0101 0100 1000_2 + 0001 0010 0010_2
   iii) 0010 0100 0111_2 + 0001 0001 0001_2

UNIT – II

3. (a) Find the complement of the following expressions: **[7M]**
   i) $xy' + x'y$
   ii)$(AB' + C)D' + E$

   (b) Convert the following expressions into sum of products: **[7M]**
   i) (AB + C)$(B + C'D)$
   ii) $x' + x(x + y)(y + z')$

4. (a) Define three input NAND gate and NOR gate with truth table. **[7M]**

   (b) Find the minimized product-of-sums expression for the following Boolean Function **[7M]**
   $F = \sum m(5, 7, 9, 10, 11) + \sum d(2, 13, 15)$

UNIT – III

5. (a) A majority function is generated in a combinational circuit when the output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3 input majority function. **[7M]**

   (b) Show that a full-subtractor can be constructed with two half-subtractors and an OR gate. **[7M]**

6. (a) Differentiate a parallel adder from serial adder. Explain a parallel adder/ subtractor using 2s complement system with the help of a logic diagram. **[7M]**

   (b) Design a combinational circuit with four inputs and four outputs. The output generates the 2's complement of the input binary number. **[7M]**

UNIT – IV

7. (a) Construct a D flip-flop using T flip-flop with the help of characteristic equations. **[7M]**

   (b) Design a synchronous binary counter using T flip flops to count the following sequence: **[7M]**
   000, 001, 010, 011, 100, 101, 110, 111

8. (a) Design a synchronous BCD counter with T flip-flops. **[7M]**

   (b) Consider a JK' flip-flop i.e., JK flip-flop with an inverter between the external input K' and the internal input K **[7M]**
   i) Obtain the characteristic equation.
   ii) Obtain the excitation table.

UNIT – V

9. (a) Explain the following with an example. **[7M]**
   i. State diagram
   ii. State table
   iii. State equation

   (b) Convert the following Mealy machine into corresponding Moore Machine as per given in Table 1. **[7M]**

Table 1

Present state	Next state, Z	
	X=0	X=1
A	D, 0	B, 1
B	A, 1	D, 0
C	C, 1	C, 0
D	B, 0	A, 1

10. (a) Elaborate the steps involved in the design of synchronous sequential circuits. **[7M]**

    (b) Design a 1011 sequence detector using T flip-flop with overlap. **[7M]**

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