INSTITUTE OF AERONAUTICAL ENGINEERING

Dundigal, Hyderabad - 500 043

COMPUTER SCIENCE AND ENGINEERING

ASSIGNMENT

Course Name : **Computer Organization**
Course Code : A40506
Class : II B. Tech II Semester
Branch : Computer Science and Engineering
Year : 2016– 2017
Course Faculty : Ms.S.J.Sowjanya, Mr.K.Chiranjeevi, Ms.B.Tejeshwi

OBJECTIVES

To meet the challenge of ensuring excellence in engineering education, the issue of quality needs to be addressed, debated and taken forward in a systematic manner. Accreditation is the principal means of quality assurance in higher education. The major emphasis of accreditation process is to measure the outcomes of the program that is being accredited.

In line with this, Faculty of Institute of Aeronautical Engineering, Hyderabad has taken a lead in incorporating philosophy of outcome based education in the process of problem solving and career development. So, all students of the institute should understand the depth and approach of course to be taught through this question bank, which will enhance learner's learning process.

S. No	Question	Blooms Taxonomy Level	Program Outcomes
	UNIT-I		
1	**Calculate** how many one-address instructions can be formulated when A Computer has 32-bit instructions and 12-bit address with 250 two-address instructions?	Apply	4
2	**List** a program to evaluate the arithmetic statement. $X= \frac{A\,[B+C\,(D+E)]}{F(G+H)}$ Using Zero address instructions.	Knowledge	4
3	**Calculate** the number of times control unit refer to memory when it fetches and executes an indirect addressing mode instruction if the instruction is a computational type requiring an operand from memory?	Apply	2
4	**Calculate** the address field of an indexed addressing mode instruction to make it the same as a register indirect mode instruction?	Apply	4
5	**List** the basic differences between a branch instruction, a call subroutine instruction, and a program interrupt?	Knowledge	3
6	**Define** an instruction format? Explain different types of instruction formats in detail.	Knowledge	1
7	**Explain** different types of addressing modes with Suitable examples?	Understand	1
8	**Define** an interrupt? Explain Types of interrupts?	Knowledge	3
9	**Illustrate** one-address and zero-address instruction formats, With Examples?	Apply	1
	UNIT-II		
1.	A CPU with a 20-MHZ clock is connected to a memory unit whose access time is 40 ns. Describe a read and write timing diagrams using a READ strobe and a WRITE strobe, Include the address in the timing diagram.	Understand	I
2.	**Calculate** How many characters per second can be transmitted over a 1200-baud line in each of the following mode ?(assume a character code of 8 bits) a) Synchronous serial Transmission. b) Asynchronous serial Transmission with one stop bit. c) Asynchronous serial Transmission with two stop bits.	Apply	2

S. No	Question	Blooms Taxonomy Level	Program Outcomes
3.	**Explain** the programming steps are required to check when a source interrupts the computer while it is still being service by a previous interrupt request from the same source?	Understand	2
4.	**Calculate** the minimum number of bits that a frame must have in the bit-oriented protocol?	Apply	1
5.	**Explain** Asynchronous communication interface with diagram?	Understand	3
6.	**Describe** the basic advantage of using Interrupt-Initiated data transfer over transfer under program control without an interrupt?	Understand	3
7.	In most computers an interrupt is recognized only after the execution of the instruction .Consider the possibility of acknowledging the interrupt at any time during the execution of the instruction. Discuss the difficulty that may arise.	Understand	b
8.	A DMA controller transfers 16-bit words to memory using Cycle stealing. The words are assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. Calculate how much will the CPU be slowed down because of the DMA transfer?	Apply	1
9.	**Explain** why DMA have priority over the CPU when both request a memory transfer?	Understand	3
10.	**Explain** briefly about Intel- 8089 Input-Output processor.	Understand	3
	UNIT - III		
1.	In many computers the cache block size is in the range 32 to 128 bytes. Discuss the main advantages and disadvantages of making the size of the cache blocks larger or smaller?	Understand	1
2.	**Define** a mapping function? Explain Set-Associative mapping technique with Example?	Understand	3
3.	**Explain** virtual memory Address translation with diagram?	Understand	3
4.	An eight-way set-associative cache consists of a total of 256 blocks. The main memory contains 8192 blocks, each consisting of 128 words. 1. Calculate number of bits in the main memory address? 2. Calculate number of bits in the TAG, SET and WORD fields?	Apply	5
5.	**Calculate** the number of page faults using Least Recently used (LRU) Page Replacement Algorithm for the following CPU References. 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1 Assume Main Memory contains 3 frames.	Apply	5
6.	**Calculate** the number of page faults using First In First out (FIFO) Page Replacement Algorithm for the following CPU References. 3 4 5 6 4 7 4 0 6 7 4 7 6 5 6 4 5 3 4 5 Assume Main Memory contains 4 frames.	Apply	5
7.	**Define** a mapping function? Explain Associative mapping technique with Example?	Understand	5
8.	**Explain** i) Write through policy ii) write back policy iii) Hit and Miss ratio.	Understand	c
9.	The Access Time of a Cache Memory is 100 ns and that of main memory 1000 ns. It is estimated that 80 percent of the memory requests are for read and the remaining 20 percent for write. The hit ratio for read access only is 0.9. A Write through Procedure is used. Calculate the average access time of the system considering only memory read cycles. Calculate the average access time of the system for both read and write requests. Calculate the hit ratio taking into consideration the write cycles?	Apply	5
10	A computer employs RAM chips of 256x8 and ROM chips of 1024x8 the computer system needs 2K bytes of RAM ,4K bytes of ROM and 4 interface units each with 4 registers .A memory mapped I/O configuration is used .the two highest order bits of the address bus are assigned 00 for RAM,01 for ROM , and 10 for interface register. a) Calculate How many RAM and ROM chips are needed? b) Draw a memory address map for the system. c) Give the address range in Hexadecimal for RAM, ROM ,and interface.	Understand	5

S. No	Question	Blooms Taxonomy Level	Program Outcomes
	UNIT – IV		
1.	**Explain** why 8086 internal architecture with the help of BIU and EU?	Understand	3
2.	**Define** arithmetic pipeline with an example?	Understand	3
3.	**Explain** about HOLD response sequence?	Understand	2
4.	**Explain** MINIMUM and MAXIMUM modes in 8086?	Understand	2
5.	**Differentiate** 8086 with 8085?	Understand	2
6.	**Explain** about interrupts in 8086?	Understand	3
7.	**Explain** what are the GPR & SPR registers in 8086?	Understand	3
8.	**Classify** flag registers in 8086 and explain it?	Apply	3
9.	**Differentiate** between physical address, effective address and offset Address?	Understand	1
10.	**Discuss** the addressing modes provided by 8086 with examples?	Understand	1
	UNIT – V		
1.	**Describe** the following instructions with examples? i) IMUL ii) XLATE iii) XCHG iv) MOVSB	Understand	1
2.	**Summarize** the following instructions i. WAIT ii. HLT iii. ESC iv. NOP.	Understand	1
3.	**Explain** briefly about string instructions.	Understand	3
4.	**Discuss** assembly language program to find sum of squares.	Understand	5
5.	**Explain** a program to read ASCII code after a strobe signal is sent from a Keyboard?	Understand	1
6.	I**dentify** the logical instructions available in 8086 with one example.	Understand	5
7.	**Define** non-Mask able interrupts.?	Apply	3
8.	**Explain** ALIGN & ASSUME?	Understand	3
9.	**Discuss** about cross-compiler.	Understand	3
10	**Explain** about the instruction format in 8086?	Understand	2