INSTITUTE OF AERONAUTICAL ENGINEERING

(AUTONOMOUS)
Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

ASSIGNMENT QUESTION BANK

Course Name	:	**DIGITAL DESIGN USING VERILOG HDL**
Course Code	:	A40410
Class	:	II - B. Tech II Semester
Branch	:	Electronics and Communication Engineering
Year	:	2016 – 2017
Course Faculty	:	Mr. Khalandhar Basha, Mr. K. Arun Sai, Mr. K Sudhakar Reddy, Mr. N Nagaraju

OBJECTIVES

Designing digital circuits at behavioral and RTL modeling of digital circuits using Verilog HDL. Verifying these models, and synthesizing RTL models to standard cell libraries and FPGAs.

Students gain practical experience by designing, modeling, implementing and verifying several digital circuits. This course aims provide students with the Understand of different technologies related to HDLs, constructs, compile and execute verilog HDL programs using provided software tools. Design digital components and circuits that are testable, reusable and synthesizable.

S.No	Question	Blooms Taxonomy Level	Course Outcome
	ASSIGNMENT-I **UNIT-I** **INTRODUCTION TO VERILOG HDL**		
1.	Discuss Level of design description.	Understand	1
2	Discuss Level of design description.	Understand	1
3	Write short notes on, (a) Concurrency (b) Functional verification	Evaluate	1
4	Define the following terms relevant to Verilog HDL, (a). Simulation versus synthesis. (b). PLI (c). System tasks.	Remember	1
5	Explain about, (a). Display tasks (b). Strobe tasks (c). Monitor tasks with examples.	Understand	1
6	Write a syntax functions and tasks with one example.	Apply	1
7	Explain about number system used in Verilog.	Understand	1
8	Write about $readmemb with example.	Apply	1
9	Explain the components of a Verilog module with block diagram.	Understand	1
10	Write about and differences scalars vectors in Verilog module with	Apply	1

S.No	Question	Blooms Taxonomy Level	Course Outcome
	examples.		
	ASSIGNMENT – II **UNIT-II** **GATE LEVEL MODELING AND MODELING AT DATAFLOW LEVEL**		
1	Explain clocked RS flip-flop Verilog module and test bench.	Understand	2
2	Design a D-Flip-flop with gate primitives and write its Verilog code.	Synthesis	2
3	Design a D flip flop using NAND gates.	Synthesis	2
4	Write a Verilog code for D flip flop using NAND gates.	Apply	2
5	Classify delays and explain.	Creating	2
6	Explain inertial and intra-assignment delays in Verilog.	Understand	2
7	Design a JK flip flop using NAND gates.	Synthesis	2
8	Write a Verilog code for JK flip flop using NAND gates.	Apply	2
9	Explain the design approach of a master slaveflip-flop with gate primitives. (OR)Design a master slave JK flip-flop using NAND gates.	Apply	2
10	Write a Verilog code for master slave JK flip flop using NAND gates.	Apply	2
	ASSIGNMENT – III **UNIT-III** **BEHAVIORAL MODELING**		
1	Write short notes on the following with examples, (a). Intra-assignment delays (b). Delay assignments (c). Zero delay.	Apply	3
2	What are the advantages of multiple always blocks? Explain with example.	remembering	3
3	Write a Verilog module for a rudimentary serial transmitter module.	Apply	3
4	Explain multiple always blocks.	Understand	3
5	Write a model using the behavioral modeling style to describe the behavior of a JK flip- flop using an always statement.	Apply	3
6	(a). Design Verilog module to identify the highest priority interrupts. (b). Write test bench simulation results of above questions with explanation	synthesis	3
7	(a). Design module to convert angels in radians to one in degrees. (b). Write Verilog code above question with explanation.	synthesis	3
8	Explain blocking and non-blocking statement with examples.	Understand	3
9	a Verilog HDL code for n-bit shift register with an enable input using blocking assignments.	Apply	3
10	Draw the flowchart for the simulation flow. OR Explain flowchart for the simulation flow.	Understand	3
	ASSIGNMENT – IV **UNIT-IV** **SWITCH LEVEL MODELING, SYSTEM TASKS FUNCTIONS AND COMPILERDIRECTIVES**		
1	Define and explain the following terms relevant to Verilog HDL, (a) Module parameters (b) File-based tasks and functions (c) Compiler directives.	Remember	4
2	Explain parameter declaration and assignments.	Understand	4
3	Explain type declaration for parameters.	Understand	4
4	Explain automatic(recursive) function.	Understand	4
5	Explain about module paths.	Understand	4
6	Define and explain the following terms relevant to Verilog HDL, (a) Hierarchical access (b) Path delays.	Remember	4
7	Explain $ finish task with example.	Understand	4
8	Explain $ random function with example.	Understand	4

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9	Explain asymmetric sequence generator with example.	Understand	4
10	Explain automatic(re-entrant) tasks with example.	Understand	4
	ASSIGNMENT – V **UNIT-V** **SEQUENTIAL CIRCUIT DESCRIPTION, COMPONENT TEST VERIFICATION**		
1	Define hold time. Design a Verilog module for D flip-flop with hold time.	Remember	5
2	Discuss about setuphold, width and period checks used in Verilog. Write a Verilog module for D flip-flop using setuphold, width and period checks.	Remember	5
3	Design a Verilog module for the following, (i) 8-bit transparent D-Latch (ii) 8-bit register with tri-state output.	synthesis	5
4	How does the memory initialization is carried out in Verilog? Explain with the help of an example.	synthesis	5
5	What are the rules to be followed to declare and to use the bidirectional lines?	Evaluate	5
6	Write a Verilog module for PLA.	Understand	5
7	What is functional register? Write and explain the Verilog module for basic shift register?	Evaluate	5
8	Design and explain the Verilog module for universal shift register.	synthesis	5
9	Explain about shift register that uses separates combinational and sequential blocks. Also write a Verilog code for the same.	Understand	5
10	Write a Verilog code for 4-binary up-down counter.	Understand	5

Prepared By: Mr. Khalandhar Basha, Mr. K Arun Sai, Mr. K Sudhakar Reddy, Mr. N Nagaraju.

HOD, ECE