Hall Ticket No | | | | | | | | | | | Question Paper Code: AEC010

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Four Year B.Tech V Semester End Examinations (Supplementary) - January, 2019

Regulation: IARE – R16

COMPUTER ORGANIZATION

Time: 3 Hours **(ECE)** **Max Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

UNIT – I

1. (a) Using an example explain about floating-point representation and normalize the final result. **[7M]**

   (b) Convert the following **[7M]**
   (i) $(724)_8 = ()_{10}$
   (ii) $(ABC)_{16} = ()_{10}$
   (iii) $(10.1011)_2 = ()_{10}$

2. (a) Briefly explain about instruction formats. **[7M]**

   (b) Show how can the following operation be performed using: **[7M]**
   a) three address instruction
   b) two address instruction
   c) one address instruction
   d) zero address
   instruction X = (A + B) * (C + D)

UNIT – II

3. (a) Explain about floating point addition & subtraction using flow chart. **[7M]**

   (b) With a help of flow chart explain the booth algorithm and show the step by step multiplication process for -9 X -13. **[7M]**

4. (a) Write the algorithm for division of floating point numbers and illustrate with an example **[7M]**

   (b) Explain about multiplication algorithm. Discuss step by step Multiplication operation on the following data **[7M]**
   B= 10111
   Q= 10101

UNIT – III

5. (a) Explain the concepts on Nano Programming in detail. **[7M]**

   (b) Illustrate data hazards in pipeline with an example. **[7M]**

6. (a) Write short note on the following **[7M]**
   (i) Microinstruction Format
   (ii) Micro operations
   (iii) Subroutine

   (b) Consider a computer with four floating-point pipeline processors. Suppose that each processor uses a cycle time of 40 ns. How long will it take to perform 400 floating - point operations? Is there a difference if the same 400 operations is carried out using a single pipeline processor with a cycle time of 10 ns? **[7M]**

UNIT – IV

7. (a) Write a short note on the following (i) Write back (ii) Locality of Reference (iii) Sequential access (iv) Random access **[7M]**

   (b) A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memorymapped 1/0 configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers. a) How many RAM and ROM chips are needed? b) Draw a memory-address map for the system. c) Give the address range in hexadecimal for RAM, ROM, and interface **[7M]**

8. (a) Write about memory mapping techniques **[7M]**

   (b) An 8-bit computer has a 16-bit address bus. The first 15 lines of the address are used to select a bank of 32K bytes of memory. The highorder bit of the address is used to select a register which receives the contents of the data bus. Explain how this configuration can be used to extend the memory capacity of the system to eight banks of 32K bytes each, for a total of 256K bytes of memory **[7M]**

UNIT – V

9. (a) Write a note on the following: **[7M]**
   i. Vectored interrupts
   ii. PCI interrupts
   iii. Pipeline interrupts

   (b) Describe in detail about bus arbitration and explain the methodology involved in IOP organization. **[7M]**

10. (a) What is RISC? and Differentiate RISC and CISC. **[7M]**

    (b) What is the advantage of two-wired hand shaking method and detailed about data transfer between source and destination. **[7M]**

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