INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

ASSIGNMENT QUESTIONS

Course Name	:	**VLSI Design**
Course Code	:	**A60432**
Class	:	**III B. Tech II Semester**
Branch	:	**Electronics and Communication Engineering**
Academic Year	:	**2017– 2018**
Course Faculty	:	**Prof.V. R. Seshagiri Rao, Professor, ECE,** **Dr. V. Vijay, Professor, ECE** **Mr. D Khalandar Basha, Assscciate Professor, ECE** **Ms. U. Dhanalakshmi, Assistant Professor, ECE**

OBJECTIVES:

To meet the challenge of ensuring excellence in engineering education, the issue of quality needs to be addressed, debated and taken forward in a systematic manner. Accreditation is the principal means of quality assurance in higher education. The major emphasis of accreditation process is to measure the outcomes of the program that is being accredited.

In line with this, Faculty of Institute of Aeronautical Engineering, Hyderabad has taken a lead in incorporating philosophy of outcome based education in the process of problem solving and career development. So, all students of the institute should understand the depth and approach of course to be taught through this question bank, which will enhance learner's learning process.

ASSIGNMENT-I

UNIT-I

INTRODUCTION AND BASIC ELECTRICAL PROPPERTIES

S. No	Questions	Blooms Taxonomy Level	Course Outcome
1	Explain the fabrication process of twin well CMOS processes with neat sketch.	Understand	1
2	Compare MOS, CMOS, and Bi-CMOS technologies.	Understand	1
3	Explain the various kinds of integrated registers and their characteristics.	Understand	1
4	Explain the various types of IC packages.	Understand	1
5	Explain the fabrication of PMOS transistor and its substrate fabrication process.	Understand	1
6	Explain different fabrication process of CMOS transistor.	Understand	1
7	Consider the nMOS transistor in a 65 nm process with a nominal threshold voltage of 0.3 V and a doping level of 8×10^{17} cm^{-3}. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 0.6 V instead of 0?	Understand	1
8	Derive an expression for Ids of an n channel enhancement MOSFET operating in saturation.	Understand	1

9	Explain the working of Bi-CMOS inverter using appropriate transfer characteristics.	Understand	1
10	Explain the working of CMOS switch with appropriate characteristics.	Understand	1
11	Explain the following a) Threshold voltage b) Pinch off voltage c) Channel length modulation d) Sub threshold leakage current e) Figure of merit.	Understand	1
12	Explain body effect of MOSFET.	Understand	1
13	Explain the various forms of pull-ups.	Understand	1
14	Explain what is latch up in CMOS and BiCMOS Susceptibility.	Understand	1
15	Differentiate the parameters of CMOS and Bipolar Technologies.	Understand	1
16	Consider the nMOS transistor in a 65 nm process with a nominal threshold voltage of 0.3 V and a doping level of 8×10^{17} cm^{-3}. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 0.6 V instead of 0?	Understand	1
17	What is the minimum threshold voltage for which the leakage current through an OFF transistor (V_{gs}=0) is 10^3 times less than that of a transistor that is barely ON ($V_{gs}=V_t$) at room temperature if n=1.5. One of the advantages of silicon-on insulator (SOI) processes is that they have smaller n. What threshold is required for SOI if n=1.3.	Understand	1
18	Consider an nMOS transistor in a 0.6 μm process with W/L = 4/2 λ (i.e., 1.2/0.6 μm). In this process, the gate oxide thickness is 100 A and the mobility of electrons is 350 cm2/V·s. The threshold voltage is 0.7 V. Plot I_{ds} vs. V_{ds} for V_{gs}=0, 1, 2, 3, 4, and 5 V.	Understand	1

UNIT-II
VLSI CIRCUIT DESIGN PROCESSES

S. No	Questions	Blooms Taxonomy Level	Course Outcome
1	Draw the circuit and layout diagram for the three input AND-OR-INVERT CMOS gate.	Understand	1
2	Discuss the need of stick diagram and explain with an example.	Remember	3
3	Design a stick diagram for NMOS logic for the logic Y=A+B+C.	Remember	3
4	Discuss CMOS logic design style. Compare with NMOS design style.	Remember	3
5	Discuss the effect of scaling on V_t.	Understand	3
6	Design layout diagram for NMOS inverter.	Understand	3
7	Sketch a stick diagram for a CMOS gate computing $Y=(A+B+C)\cdot D$ and estimate the cell width and height.	Remember	3
8	Design a layout diagram for the CMOS logic shown below Y=((A+B)·C).	Remember	3
9	Design a stick diagram for the CMOS logic shown below Y=(A+B+C).	Remember	3
10	Define scaling. What are the factors to be considered for transistor scaling?	Remember	3

UNIT-III
GATE LEVEL DESIGN

S. No	Questions	Blooms Taxonomy Level	Course Outcome
1	Explain PSEUDO nMOS Logic give its advantages and disadvantages	Remember	4
2	Explain CMOS domino logic circuit with an example. Compare its	Understand	4

	performance over that of CMOS logic.		
3	Derive the expression for rise and fall time of CMOS inverter. Comment on the expression derived.	Understand	4
4	Write notes on a. NAND CMOS logic b. Different cascade voltages switch logic.	Remember	4
5	Realize the function f=AB+CD using, a. CMOS static logic b. Pseudo-nMOS logic. Use only NAND gates.	Understand	4
6	Write notes on a. NOR CMOS logic b. Different cascade voltages switch logic.	Remember	4
7	Draw the CMOS implementation of 4-to-1 MUX using transmission gates.	Remember	4
8	Realize the function f=ABD+BCD using, a. CMOS static logic Pseudo-nMOS logic. Use only NAND gates.		
9	Explain clocked CMOS logic, domino logic, and n-p CMOS logic.	Understand	4
10	Explain Dynamic CMOS Logic give its advantages and disadvantages.	Remember	4
ASSIGNMENT-II			
1	Discuss about area capacitance of MOS layers and give area capacitance with suitable examples.	Understand	4
2	Discuss the problem that arises when corporately large capacitance loads are driven by inverters. Explain how super buffers can solve the problem.	Understand	4
3	Discuss about wiring capacitances.	Understand	4
4	Explain about Super Buffer.	Understand	4
5	Explain in detail about choice of layers	Understand	4
6	Explain about Bi CMOS drivers.	Understand	4
7	Design a 2-input multiplexer using CMOS transmission gates.	Remember	4
8	List the logical constraints of layers.	Remember	4
UNIT-IV GATE LEVEL DESIGN			
S. No	**Questions**	**Blooms Taxonomy Level**	**Course Outcome**
1	Design and explain a 6-bit Wallace tree multiplier.	Understand	5
2	Analyze about barrel shifter.	Remember	5
3	Implement and explain the working of a ripple carry adder using transmission gates.	Understand	5
4	What is a zero/one detector? Give two applications of it. Design, implement and explain a tree based zero/one detector circuit. Implement using pass gates.	Remember	5
5	Draw the logic diagram of zero/one detector and explain its operation with the help of stick diagram.	Remember	5
6	Draw the schematic and explain the principle and operation of Array Multiplier.	Remember	5
7	Explain the carry look ahead Adder.	Understand	5
8	Explain the design hierarchies and bring out which kind of approach is better to adopt for system design.	Understand	5
9	Describe briefly n-bit parallel adder.	Understand	5
10	What is the difference between synchronous and asynchronous counter.	Remember	6
11	Draw and explain the Read/Write operation of 4T SRAM cell.	Understand	6

12	Explain the divided word line architecture of RAM.	Understand	6
13	Explain about NAND based ROM design.	Understand	6
14	Explain about NOR based ROM design.	Understand	6
15	Explain the principle of a DRAM cell.	Understand	6
16	Give the schematic of a DRAM and explain how READ and WRITE operations are carried out.	Remember	6
17	What is content addressable memory and give any one application of it.	Understand	6
18	What are the advantages of SRAM and DRAMs compare them in all respects.	Remember	6
19	What are the different types of serial access memories?	Remember	6
20	Discuss in detail about classification of memory arrays.	Remember	6

UNIT-V
DATA PAT SUB SYSTEMS

S. No	Questions	Blooms Taxonomy Level	Course Outcome
1	Compare FPGA and CPLD.	Remember	8
2	Explain the I/O control block of CPLD.	Understand	8
3	Draw the typical architecture of PLA and explain its operation.	Understand	7
4	Implement JK flip-flop by using PLA.	Understand	7
5	Discuss the different methods of programming of PALs.	Understand	7
6	Distinguish PLAs, PALs, CPLDs, FPGAs, and standard cells in all respects.	Remember	7
7	Explain about the principle and operation of FPGAs. What are its applications?	Understand	8
8	Draw the schematic for PLA and explain the principle. What are the advantages of PLAs?	Remember	7
9	Explain the structure and principle of PAL.	Understand	7
10	Draw the schematic and examine how Full Adder can be implemented using PLA's.	Remember	7
11	Explain about configurable FPGA based I/O blocks.	Understand	8
12	Explain the terms controllability and observability with a suitable example.	Remember	8
13	Explain the architecture of JTAG.	Remember	8
14	What is fault simulation? Explain briefly fault models. Explain the various stuck at fault models with suitable examples.	Understand	8
15	Demonstrate about BIST in detail. List the advantages of it.	Understand	8
16	Categories of the various DFT techniques and explain them each.	Understand	8
17	Discuss about signature analysis in Testing. Explain with an example.	Remember	8
18	Explain about Memory-self Test with the help of a schematic.	Understand	9
19	Analyze the issues to be considered while implementing BIST and explain each.	Remember	9
20	Explain how layout design can be done for improving testability.	Understand	9
21	Explain about different fault models in VLSI testing with examples.	Remember	9
22	Analyze any TWO a) DFT b) BIST c) Boundary scan Testing	Remember	10
23	Discuss scan-based test techniques.	Understand	10
24	Explain Ad-Hoc testing and chip level test techniques.	Remember	10
25	Explain self-test techniques.	Understand	10
26	Briefly explain	Understand	10

	a) Fault grading & fault b) Simulation Delay fault testing c) Statistical fault analysis.		

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