INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNIACTION ENGINEERING

ASSIGNMENT

Course Name	:	**LINEAR AND DIGITAL INTEGRATED CIRCUITS APPLICATIONS**
Course Code	:	**A50425**
Class	:	III - B. Tech
Branch	:	ECE
Year	:	2017-18
Course Coordinator	:	Mr. D. Khalandar Basha
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OBJECTIVES

To meet the challenge of ensuring excellence in engineering education, the issue of quality needs to be addressed, debated and taken forward in a systematic manner. Accreditation is the principal means of quality assurance in higher education. The major emphasis of accreditation process is to measure the outcomes of the program that is being accredited.

In line with this, Faculty of Institute of Aeronautical Engineering, Hyderabad has taken a lead in incorporating philosophy of outcome based education in the process of problem solving and career development. So, all students of the institute should understand the depth and approach of course to be taught through this question bank, which will enhance learner's learning process.

ASSIGNMENT-I

S.No	QUESTION	Blooms taxonomy level	Course Outcome
	UNIT-I **OPERATIONAL AMPLIFIER**		
1	Explain the operation of a Schmitt trigger circuit using IC 741.	Understand	1
2	Explain practical integrator circuit using IC 741.	Analyze	1
3	Explain the internal structure of voltage regulator IC 723. Also draw a low voltage Regulator circuit using IC 723andexplain its operation.	Analyze	2
4	Explain the following terms in an OP-AMP. 1. Input Bias current 2. Input offset voltage 3. Input offset current	Remember	2
5	Explain non inverting comparator using op-amp.	Understand	3
6	Derive the gain for non inverting op-amp.	Remember	2
7	An op-amp with a slew rate = 0.5V/μS is used as an inverting amplifier to obtain a gain of 100. The voltage gain Vs frequency characteristic of the amplifier is flat up to 10 KHz. Determine i. The maximum peak-to-peak input signal that can be applied without any distortion to the output ii. The maximum frequency of the input signal to obtain a sine wave output of 2V peak.	Analyze	2
8	Design a Schmitt trigger for UTP =0.5v and LTP = -0.5V.assume necessary data.	Evaluate	3
9	Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 1 KHz. If a sine wave of 1V peak at 1000 Hz is applied to this differentiator draw the output waveforms.	Evaluate	2

10	Determine the output voltage of the differential amplifier having input voltages V1=1mV and V2=2 mV. The amplifier has a differential gain of 5000 and CMRR 1000.	Remember	2
11	Draw the output waveform for a sine wave of 1vpeak at 100Hzapplied to the differentiator.	Evaluate	2
12	Design an op-amp differentiator that will differentiate an Input signal with fmax = 100Hz	Remember	2
	UNIT -2 **OP-AMP, IC -555 & IC 565 APPLICATIONS**		
1	Design a second order low pass filter.	Evaluate	4
2	Draw the circuit of a 1st order low pass filter and derive its transfer function.	Analyze	4
3	Derive the expression for i) capture range in PLL ii) Lock in range in PLL.	Analyze	6
4	Draw the circuit of a 1st order band pass filter and derive its transfer function.	Analyze	4
5	Draw the circuit of a all pass filter and derive its transfer function.	Analyze	4
6	Derive the voltage to frequency converter factor for VCO.	Analyze	6
7	Explain any two applications of Astable multivibrator using 555IC.	Analyze	5
8	Explain VCO operation in PLL.	Understand	6
9	Design an Astable Multivibrator using 555 Timer to produce 1Khz square wave form for duty cycle=0.50	Evaluate	5
10	Design and draw the wave forms of 1KHZ square waveform generator using555 Timer for duty cycle D=25% .	Evaluate	5
11	Design a LPF at a cutoff frequency of 1 KHz and a pass band gain of 2.	Analyze	4
12	Design a 2^{nd} order HPF at a cutoff frequency of 2 KHz.	Analyze	4
13	Calculate output frequency f_0 , lock range and capture range of a 565 PLL if RT = 10K ohms, CT = 0.01µF and C = 10 µF.	Analyze	6
14	Design a square wave generator of frequency 100Hz and duty cycle of 75%.	Evaluate	5
	UNIT-3 **DATA CONVERTERS**		
1	Explain the working of a Weighted resistor D/A converter.	Evaluate	8
2	With neat diagram, explain the working principle of inverter R-2R ladder DAC.	Understand	8
3	Find the voltage at all nodes 0, 1, 2, …. And at the output of a 5-bit R-2R ladder DAC. The least Significant bit is 1 and all other bits are equal to 0. Assume VR = -10V and R=10KΩ.	Remember	8
4	With neat diagram, explain the working principle of R-2R ladder type DAC.	Analyze	8
5	Calculate basic step of 9 bit DAC is 10.3 mV. If 000000000 represents 0V, what output produced if the input is 101101111.	Apply	8
	ASSIGNMENT -2		
1	Explain successive approximation A/D converter.	Understand	8
2	Explain the working of a dual slope A/D converter.	Remember	8
3	Explain the operation of parallel comparator type ADC.	Analyze	8
4	Explain the working of a counter type A/D converter and state it's important feature.	Understand	8
5	A dual slope ADC uses a16-bit counter and a 4MHz clock rate. The maximum input voltage is+10v. The maximum integrator output voltage should be-8v when the counter has cycled through 2n counts. The capacitor used in the integrator is 0.1 µF Find the value of the resistor R of the integrator.	Apply	8
6	An ADC converter has a binary input of 0010 and an analog output of 20mv. What is the resolution?	Apply	7,8
	UNIT-IV **DIGITAL INTERAGETED CIRCUITS**		
1	Explain the following terms with reference to CMOS logic. i. Logic Levels ii. Noise margin	Apply	10

	iii. Power supply rails iv. Propagation delay		
2	Draw the circuit diagram of two-input 10K ECL OR gate and explain its operation.	Analyze	11
3	Design CMOS transistor circuit for 2-input AND gate. Explain the circuit with the help of function table?	Remember	11
4	Draw the resistive model of a CMOS inverter circuit and explain its behavior for LOW and HIGH outputs.	Remember	11
5	Design a three input NAND gate using diode logic and a transistor inverter? Analyze the circuit with the help of transfer characteristics.	Evaluate	11
6	Realize the logic function performed by 74×381 with ROM.	Evaluate	11
7	Analyze the fall time of CMOS inverter output with RL = 100, VL = 2.5V and CL=10PF. Assume VL as stable state voltage.	Analyze	11
8	Design a CMOS transistor circuit with the functional behavior f(X) = ((A+B')(B+D')(A+D'))'	Analyze	11
9	Design BCD to gray code converter.	Understand	11
10	Implement the following function with 8 : 1 MUX. F(W,X,Y,Z) = ∑m (2,4,6,7,10,11,12,13,14)	Analyze	11
11	Implement the following multi output combinational logic circuit using 4:16 decoder IC , AND external gates. F1 = ∑m (1,5,8,11) F2 = ∑m (1,6,8,9,12) F3 = ∑m (7,10,15)	Analyze	11
12	A single pull-up resistor to +5V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor? How much high state DC noise margin can be provided in this case?	Analyze	11
	UNIT-V **SEQUNTIAL LOGIC ICS AND MEMORIES**		
1	Draw the logic diagram of 74×163 binary counter and explain its operation.	Understand	13
2	Design a modulo-100 counter using two 74×163 binary counters?	Apply	13
3	Design a Modulo-12 ripple counter using 74×74?	Apply	13
4	Discuss how PROM, EPROM, EEPROM technologies differ from each other?	Analyze	13
5	Differentiate between ripple counter and synchronous counter? Design a 4-bit counter in both modes and estimate the propagation delay.	Remember	13
6	Design a modulo-88 counter using 74X163 Ics.	Understand	13
7	Draw the logic diagram of 74×163 binary counter and explain its operation.	Remember	11
8	Determine the ROM size needed to realize the logic function performed by 74×153 and 74×139.	Apply	13
9	Realize the logic function performed by 74×381 with ROM.	Evaluate	13
10	Explain the internal structure of 64K×1 DRAM with the help of timing diagrams.	Apply	13
11	Explain the necessity of two-dimensional decoding mechanism in memories. Draw MOS transistor memory cell in ROM and explain the operation.	Apply	13
12	Design excess-3 decimal counter using 74X163.	Apply	12
13	How many flip-flops are required to build a binary counter that counts from 0 to 256. And design the binary counter.	Apply	12
14	Design negative edge triggered D flip-flop.	Understand	12

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