ANALOG AND DIGITAL ELECTRONICS LABORATORY MANUAL

Subject Code	:	AECB04
Regulations	:	IARE – R18
Class	:	III Semester (EEE)

INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)

Dundigal – 500 043, Hyderabad

Department of Electrical and Electronics Engineering

VISION AND MISSION OF THE DEPARTMENT:

VISION

The vision of the Electrical and Electronics Engineering department is to build a research identity in all related areas of Electrical Engineering uniquely. Through core research and education, the students will be prepared as the best professional Engineers in the field of Electrical Engineering to face the challenges in such disciplines.

MISSION

The Electrical and Electronics Engineering Department supports the mission of the College through high quality teaching, research and services that provide students a supportive environment. The department will make the best effort to promote intellectual, ethical and technological environment to the students. The department invokes the desire and ability of life-long learning in the students for pursuing successful career in engineering.

INSTITUTE OF AERONAUTICAL ENGINEERING

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Department of Electrical and Electronics Engineering

Program Outcomes	
PO1	**General Knowledge**: An ability to apply the knowledge of mathematics, science and Engineering for solving multifaceted issues of Electrical Engineering.
PO2	**Problem Analysis**: An ability to communicate effectively and to prepare formal technical plans leading to solutions and detailed reports for electrical systems.
PO3	**Design/Development of Solutions**: To develop Broad theoretical knowledge in Electrical Engineering and learn the methods of applying them to identify, formulate and solve practical problems involving electrical power.
PO4	**Conduct Investigations of Complex Problems**: An ability to apply the techniques of using appropriate technologies to investigate, analyze, design, simulate and/or fabricate/commission complete systems involving generation, transmission and distribution of electrical energy.
PO5	**Modern Tool Usage:**An ability to model real life problems using different hardware and software platforms, both offline and real-time with the help of various tools along with upgraded versions.
PO6	**The Engineer and Society:**An Ability to design and fabricate modules, control systems and relevant processes to meet desired performance needs, within realistic constraints for social needs.
PO7	**Environment and Sustainability:** An ability To estimate the feasibility, applicability, optimality and future scope of power networks and apparatus for design of eco-friendly with sustainability
PO8	**Ethics:** ToPossess an appreciation of professional, societal, environmental and ethical issues and proper use of renewable resources.
PO9	**Individual and Team Work:** an Ability to design schemes involving signal sensing and processing leading to decision making for real time electrical engineering systems and processes at individual and team levels.
PO10	**Communication:** an Ability to work in a team and comprehend his/her scope of work, deliverables , issues and be able to communicate both in verbal ,written for effective technical presentation.
PO11	**Life-Long Learning:** An ability to align with and upgrade to higher learning and research activities along with engaging in life-long learning.
PO12	**Project Management and Finance**: To be familiar with project management problems and basic financial principles for a multi-disciplinary work.

Program Specific Outcomes	
PSO1	**Professional Skills:** Able to utilize the knowledge of high voltage engineering in collaboration with power systems in innovative, dynamic and challenging environment, for the research based team work.
PSO2	**Problem-Solving Skills:**Can explore the scientific theories, ideas, methodologies and the new cutting edge technologies in renewable energy engineering and use this erudition in their professional development and gain sufficient competence to solve the current and future energy problems universally.
PSO3	**Successful Career and Entrepreneurship:**The understanding of technologies like PLC, PMC, process controllers, transducers and HMI one can analyze, design electrical and electronics principles to install, test , maintain power system and applications.

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ATTAINMENT OF PROGRAM OUTCOMES & PROGRAM SPECIFIC OUTCOMES

Exp .No	Name of the Experiment	Program Outcomes Attained	Program Specific Outcomes Attained
1	Understand the pn junction diode characteristics.	PO 1	PSO1
2	Understand the zener diode characteristics and voltage regulator.	PO 1	PSO1
3	Understand half wave and full wave rectifier with and without filter.	PO 1	PSO1
4	Analyze input and output CE characteristics	PO 2	PSO1
5	Analyze input and output CB characteristics	PO 2	PSO1
6	Understand the frequency response of CE amplifier.	PO 2	PSO1
7	Understand Boolean expressions using gates	PO 1	PSO1
8	Understand universal gates	PO 2	PSO1
9	Understand nand / nor gates	PO 2	PSO1
10	Understand adder/ subtractor	PO 2	PSO1
11	Understand binary to gray conversion	PO 2	PSO1
12	Verify truth tables and excitation tables	PO 1	PSO1
13	Realize shift register	PO 1	PSO1
14	Realize 8x1 multiplexer	PO 1	PSO1
15	Realize 2 bit comparator	PO 1	PSO1

EXPERIMENT NO 1

PN JUNCTION DIODE CHARACTERISTICS

1.1 AIM

To plot the V-I characteristics of a PN junction diode in both forward and reverse directions. Find cut in voltage (knee voltage), static and dynamic resistance in forward direction at forward current of 2mA & 8mA respectively.Find static and dynamic resistance at 10V in reverse bias condition.

1.2 COMPONENTS & EQUIPMENT REQUIRED

S.NO	Device	Range /Rating	Quantity (in No.s)
1.	Semiconductor diode trainer Board Containing		
	DC Power Supply	(0-15) V	1
	Diode (Silicon)	1N 4007	1
	Diode (Germanium)	OA79	1
	Carbon Film Resistor	1 KΩ, 1/2 W	1
2.	DC Voltmeter	(0-1) V	1
	DC Voltmeter	(0-20) V	1
3.	DC Ammeter	(0-200) μA	1
	DC Ammeter	(0-20) mA	1
4.	Connecting wires	5A	10

1.3 THEORY

A p-n junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage.When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction

increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current due to minority charge carriers

1.4 PROCEDURE

Forward Bias

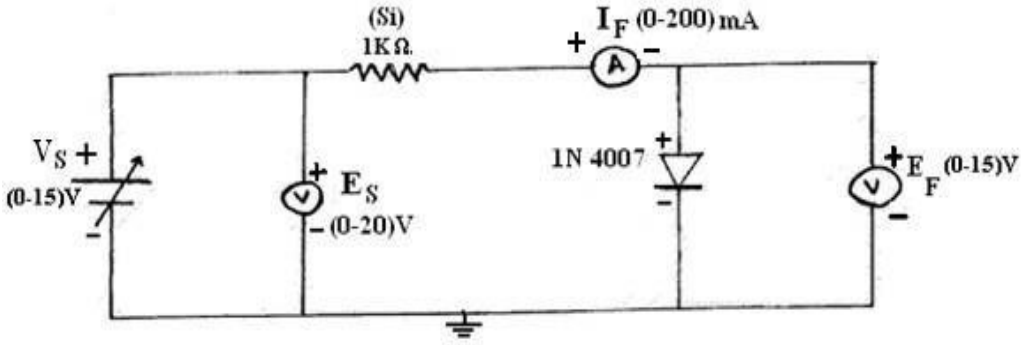
1. Connect the circuit as shown in figure(1).
2. Vary the supply voltage E_s in steps and note down the corresponding values of E_f and I_f as shown in the tabular column.

Reverse Bias

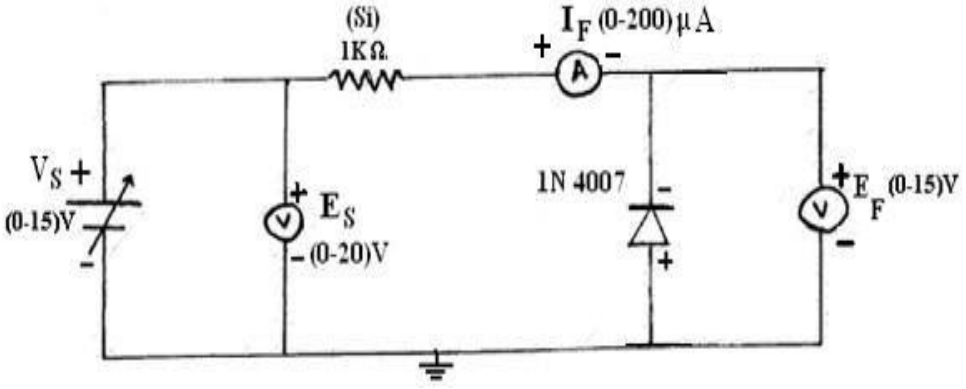
1. Connect the circuit as shown in figure (2).
2. Repeat the procedure as in forward bias and note down the corresponding Values of E_r and I_r as shown in the tabular column.

1.5 CIRCUIT DIAGRAMS

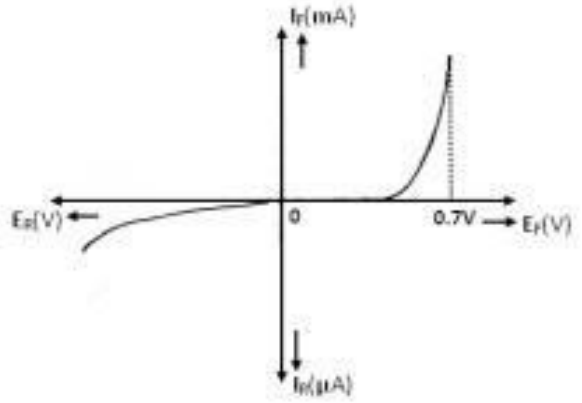
Forward Bias



Reverse Bias



1.6 EXPECTED GRAPHS



1.7 TABULAR COLUMN

Forward Bias

E_s (volts)	E_f (volts)	I_f (mA)
0.1		
0.2		
0.3		
0.4		
0.5		
0.6		
0.7		
0.8		
0.9		
1		
2		
4		
6		
8		
10		
12		
14		

Reverse Bias

E_s (volts)	E_r (volts)	I_r (μA)
0.1		
0.2		
0.3		
0.4		
0.5		
0.6		
0.7		
0.8		
0.9		
1		
2		
4		
6		
8		
10		
12		
14		

1.8 PRECAUTIONS

1. Ensure that the polarities of the power supply and the meters as per the circuit diagram.
2. Keep the input voltage knob of the regulated power supply in minimum position both when switching ON or switching OFF the power supply.
3. No loose contacts at the junctions.
4. Ensure that the ratings of the meters are as per the circuit design for precision.

1.9 CALCULATIONS

Forward Bias

Static Resistance at 8mA= E_f / I_f = Static

resistance at 2mA= E_f / I_f = Dynamic

resistance at 8mA=$\Delta E_f / \Delta I_f$ = Dynamic

resistance at 8mA=$\Delta E_f / \Delta I_f$ = **Reverse**

Bias

Static Resistance at (10V)= E_r / I_r =

Dynamic resistance at (10V)=$\Delta E_r / \Delta I_r$ =

1.10 RESULT

V-I characteristics of PN junction are plotted and verified in both forward and reverse directions.

Forward direction

(i) Cut-in-voltage=0.7V

(ii) a) Dynamic Resistance (at 8 mA) =

b) Dynamic Resistance (at 2mA) =

(iii) a) Static Resistance(at 8mA) =

b) Static Resistance (at 2mA) =

Reverse Direction

(i) Static Resistance (at 10V) =

(ii) Dynamic Resistance (at 10 V) =

1.11 LAB ASSIGNMENT

To plot the V-I characteristics of a PN junction (Germanium) diode in both forward and reverse directions by using multisim.

1.12 POST LAB QUESTIONS

1. Define cut-in voltage of a diode and specify the values for Si and Ge diodes?
2. What are the applications of a p-n diode?
3. What is PIV?
4. What is the break down voltage?
5. What is the effect of temperature on PN junction diodes?

EXPERIMENT No 2

ZENER DIODE CHARACTERISTICS AND VOLTAGE REGULATOR

2.1 AIM

Plot the V-I characteristics of a Zener diode, find zener breakdown voltage in reverse bias condition, find static and dynamic resistance in both forward and reverse bias conditions and perform zener diode voltage regulator.

2.2 COMPONENTS & EQUIPMENT REQUIRED

S.NO	DEVICES	RANGE /RATING	QUANTITY (in No.s)
1	Zener diode trainer Board Containing		
	a) DC Power Supply.	(0-15) V	1
	b) Zener Diode	4.7 V	1
	c) Zener Diode	6.2 V	1
	d) Carbon Film Resistor	1 KΩ, 1/2 W	1
2	DC Voltmeter	(0-1) V	1
	DC Voltmeter	(0-20) V	1
3	a) DC Ammeter	(0-200) μA	1
	b) DC Ammeter	(0-20) mA	1
4	Connecting wires	5A	10

2.3 THEORY

A zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage. High current through the diode can permanently damage the device.

To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals whatever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators.

2.4PROCEDUR

E ForwardBias

1. Connect the circuit as shown in figures (1)
2. Vary the supply voltage E_s in steps and note down the corresponding values of E_f and I_f as

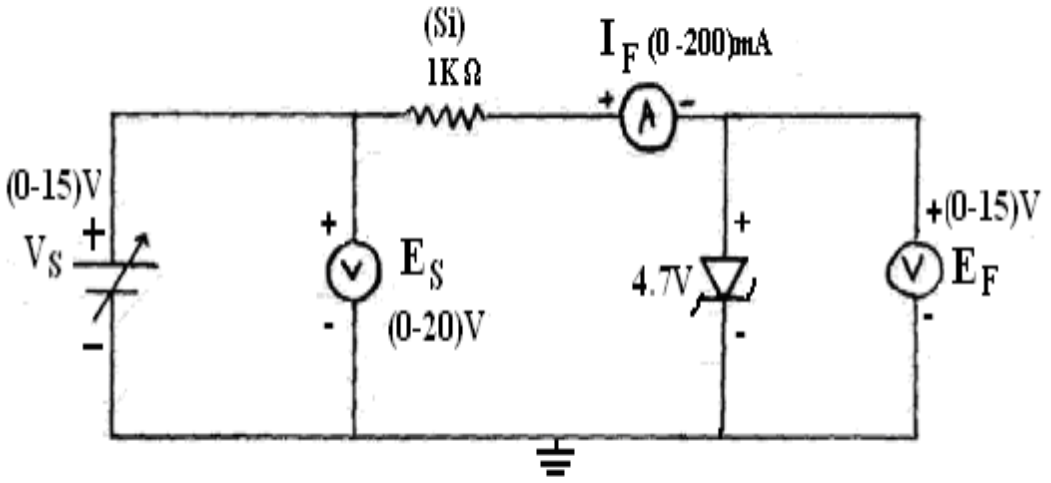
shown in the tabular column.

Reverse Bias

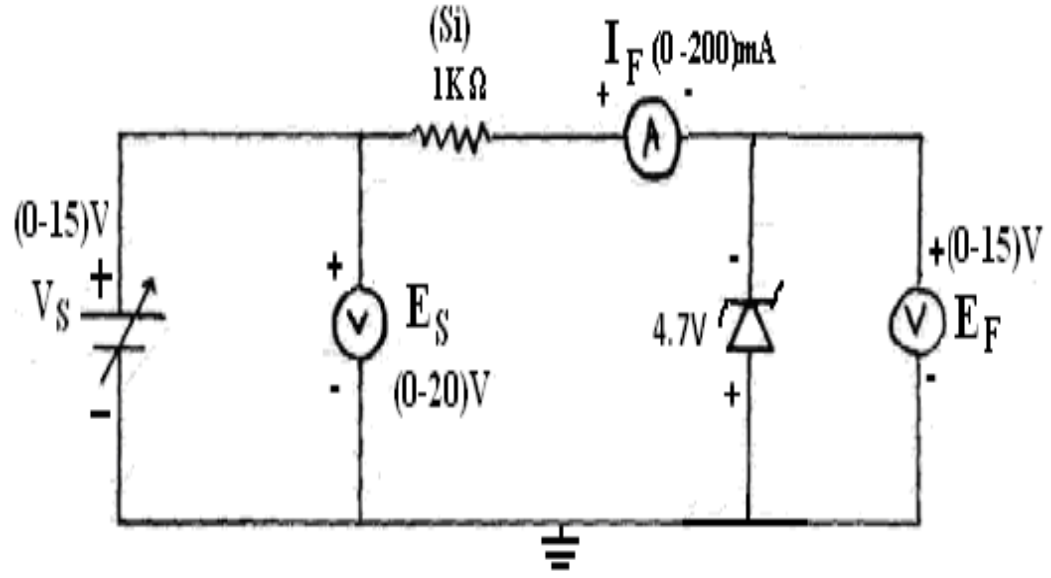
1. Connect the circuit as shown in figure (2).
2. Repeat the procedure as in forward bias and note down the corresponding values of E_r and I_r as shown in the tabular column.

2.5 CIRCUIT DIAGRAMS

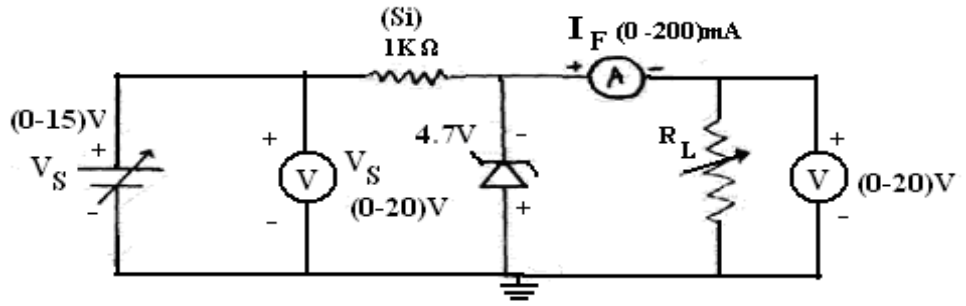
Forward Bias



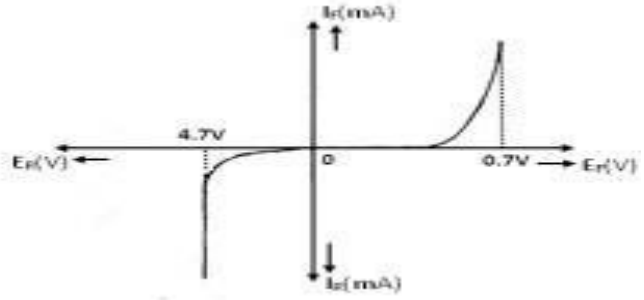
Reverse Bias



Zener Doide As Voltage Regulator



2.6 EXPECTED GRAPH



2.7 TABULAR COLUMN

Forward Bias

E_s (volts)	E_f (volts)	I_f (mA)
0.1		
0.2		
0.3		
0.4		
0.5		
0.6		
0.7		
0.8		
0.9		
1		
2		
4		
6		
8		
10		
12		
14		

Reverse Bias

E_s (volts)	E_r (volts)	I_r (mA)
0.1		
0.2		
0.3		
0.4		
0.5		
0.6		
0.7		
0.8		
0.9		
1		
2		
4		
6		
8		
10		
12		
14		

Zener Doide As Voltage Regulator:

V_{in}=15V , V_{NL}=____ **R_L=15K**

$R_L(\Omega)$	V_{FL}(volts)	I_L (mA)	%Regulation
100			
200			
500			
1K			
2K			
5K			
10K			
20K			

E_s (volts)	E_{FL} (volts)	I_L (mA)
1		
2		
4		
6		
8		
10		
12		
14		

2.8 PRECAUTIONS

1. Ensure that the polarities of the power supply and the meters as per the circuit diagram.
2. Keep the input voltage knob of the regulated power supply in minimum position both when switching ON or switching OFF the power supply.
3. No loose contacts at the junctions.
4. Ensure that the ratings of the meters are as per the circuit design for precision.

2.9 CALCULATIONS

1. Forward Static resistance at 6 mA= Ef/ If
2. Forward Dynamic resistance at 6mA=Δ Ef / Δ If
3. Reverse Static resistance at 6 mA= Ef/ If
4. Reverse Dynamic resistance at 6mA=Δ Ef / Δ I

2.10 RESULT

1. V-I characteristics of Zener diode are plotted and verified in both forward and reverse directions.
2. Zener breakdown voltage for 4.7V zener diode = 4.7V.
3. (i) Forward Bias:
    a) Static resistance at 6 mA =
    b) Dynamic resistance at 6 mA=

   (ii) Reverse Bias:

    a) Static resistance at 6 mA=
    b) Dynamic resistance at 6 mA=

2.11 LAB ASSIGNMENT

To plot the V-I characteristics of a Zener diode (6.1V) in both forward and reverse directions by using multisim.

2.12 LAB QUESTIONS

1. Explain briefly about avalanche and zener breakdowns?
2. Draw the zener equivalent circuit?
3. Differentiate between line regulation & load regulation?
4. In which region zener diode can be used as a regulator?

EXPERIMENT No 3

HALF WAVE AND FULL WAVE RECTIFIER

3.1 AIM

Examine the input and output waveforms of a half wave and full wave rectifier without and with filt ers. Calculate the ripple factor with load resistance of 1 KΩ and 10 KΩ respectively. Calculate ripple factor with a filter capacitor of 100μF and the load of 1KΩ and 10KΩ respectively.

3.2 COMPONENTS & EQUIPMENT REQUIRED

S.No	Device	Range/Rating	Quantity in No.
1	Rectifier and Filter trainer Board Containing a) AC Supply. b) Silicon Diodes c) Capacitor	 (9-0-9) V 1N 4007 100μF	 1 2 1
2	a) DC Voltmeter b) AC Voltmeter	(0-20) V (0-20) V	1 1
3	DC Ammeter	(0-50) mA	1
4	Cathode Ray Oscilloscope	(0-20) MHz	1
5	Decade Resistance Box	10Ω-100KΩ	1
6	Connecting wires	5A	12

3.3 THEORY

During positive half-cycle of the input voltage, the diode D1 is in forward bias and conducts through the load resistor R1. Hence the current produces an output voltage across the load resistor R1, which has the same shape as the +ve half cycle of the input voltage.

During the negative half-cycle of the input voltage, the diode is reverse biased and there is no current through the circuit. i.e, the voltage across R1 is zero. The net result is that only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified o/p voltage is the value measured on dc voltmeter.

For practical circuits, transformer coupling is usually provided for two reasons.

1. The voltage can be stepped-up or stepped-down, as needed.
2. The ac source is electrically isolated from the rectifier. Thus preventing shock hazards in the secondary circuit.

The circuit of a center-tapped full wave rectifier uses two diodes D1&D2. During positive half cycle of secondary voltage (input voltage), the diode D1 is forward biased and D2is reverse biased.

The diode D1 conducts and current flows through load resistor R_L. During negative half cycle, diode D2 becomes forward biased and D1 reverse biased. Now, D2 conducts and current flows through the load resistor R_L in the same direction. There is a continuous current flow through the load resistor R_L, during both the half cycles and will get unidirectional current as show in the model graph. The difference between full wave and half wave rectification is that a full wave rectifier allows unidirectional (one way) current to the load during the entire 360 degrees of the input signal and half-wave rectifier allows this only during one half cycle (180 degree).

3.4 PROCEDURE

Half Wave Rectifier without filter

1. Connect the circuit as shown in figure (a).
2. Adjust the load resistance, R_L to 500Ω, and note down the readings of input and output voltages through oscilloscope.
3. Note the readings of dc current, dc voltage and ac voltage.
4. Now, change the resistance the load resistance, RL to 1 KΩ and repeat the procedure as above. Also repeat for 10 KΩ.
5. Readings are tabulated as per the tabular column.

Half Wave Rectifier with filter

1. Connect the circuit as shown in figure (b) and repeat the procedure as for half wave rectifier without filter.

Full-wave Rectifier without filter

1. Connect the circuit as shown in the figure (c).
2. Adjust the load resistance R_L to 1KΩ and connect a capacitor of 100μF value in parallel with the load and note the readings of input and output voltages through Oscilloscope.
3. Note the readings of DC current, DC voltage and AC voltage.
4. Now change the load resistance R_L to 10KΩ and repeat the procedure as the above.
5. Readings are tabulate as per the tabular column.

Full-wave Rectifier with filter

1. Connect the circuit as shown in the figure (d).
2. Adjust the load resistance R_L to 1KΩand connect a capacitor of 100μF values in parallel with the load and note the readings of input and output voltages through Oscilloscope.
3. Note the readings of DC current, DC voltage and AC voltage.

4. Now change the load resistance R_L to 2KΩ and repeat the procedure as the above.
5. Readings are tabulate as per the tabular column.

3.5 CIRCUIT DIAGRAMS

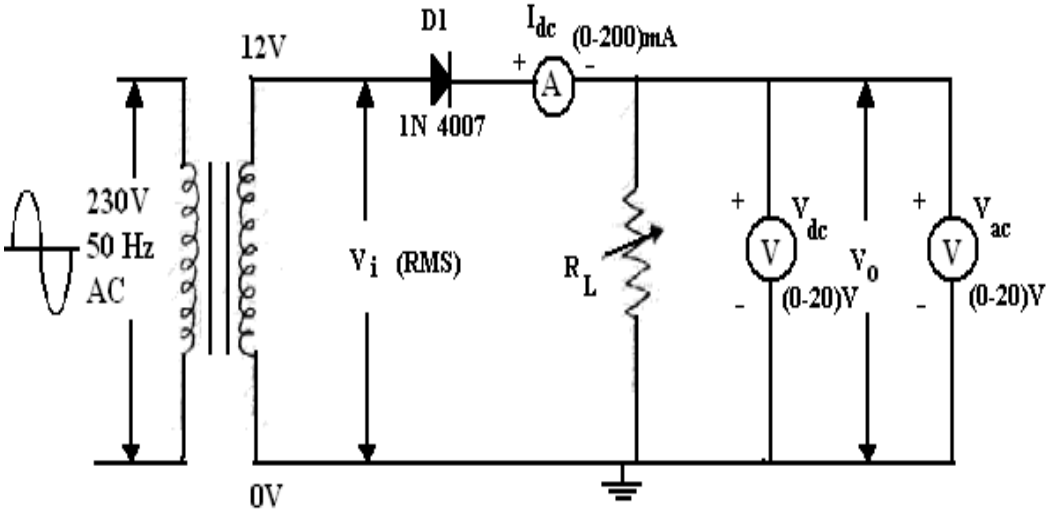


Figure (a) :Half Wave Rectifier without Filter

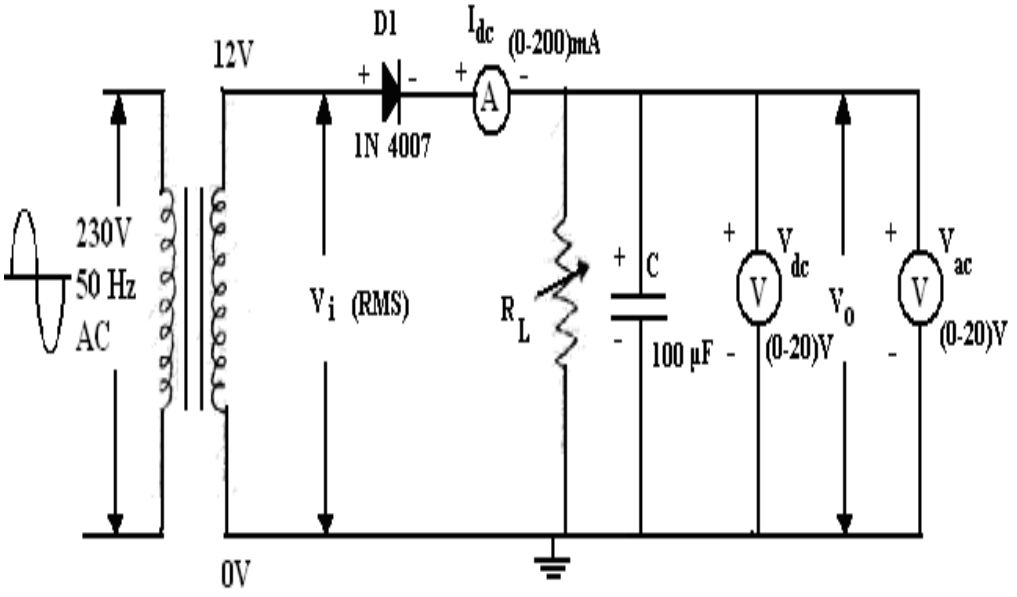


Figure (b):Half Wave Rectifier with Filter

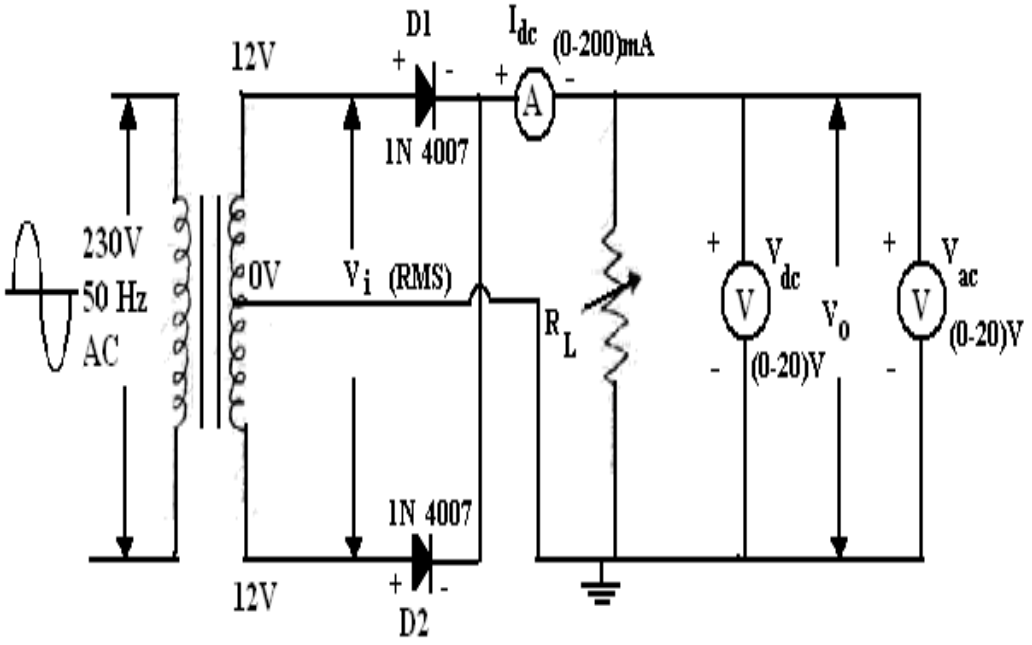


Figure (c): Full Wave Rectifier without Filter

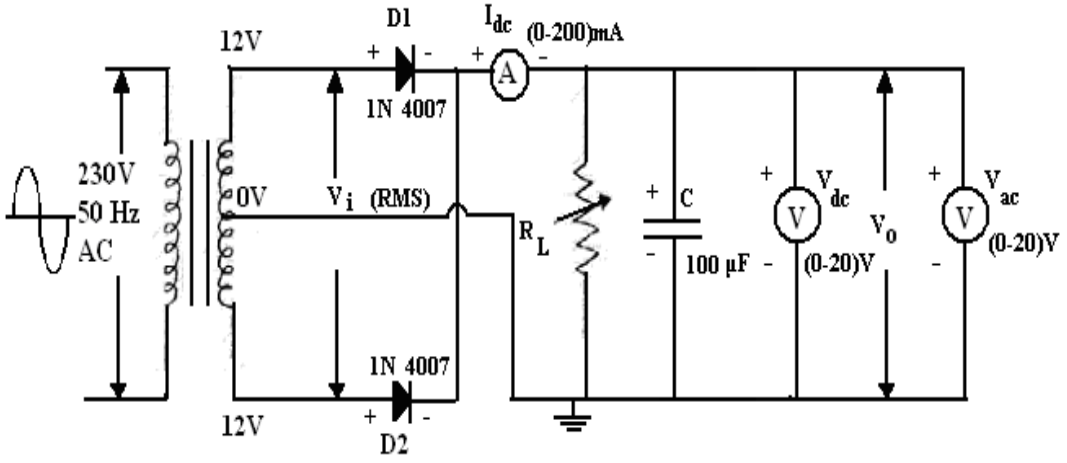
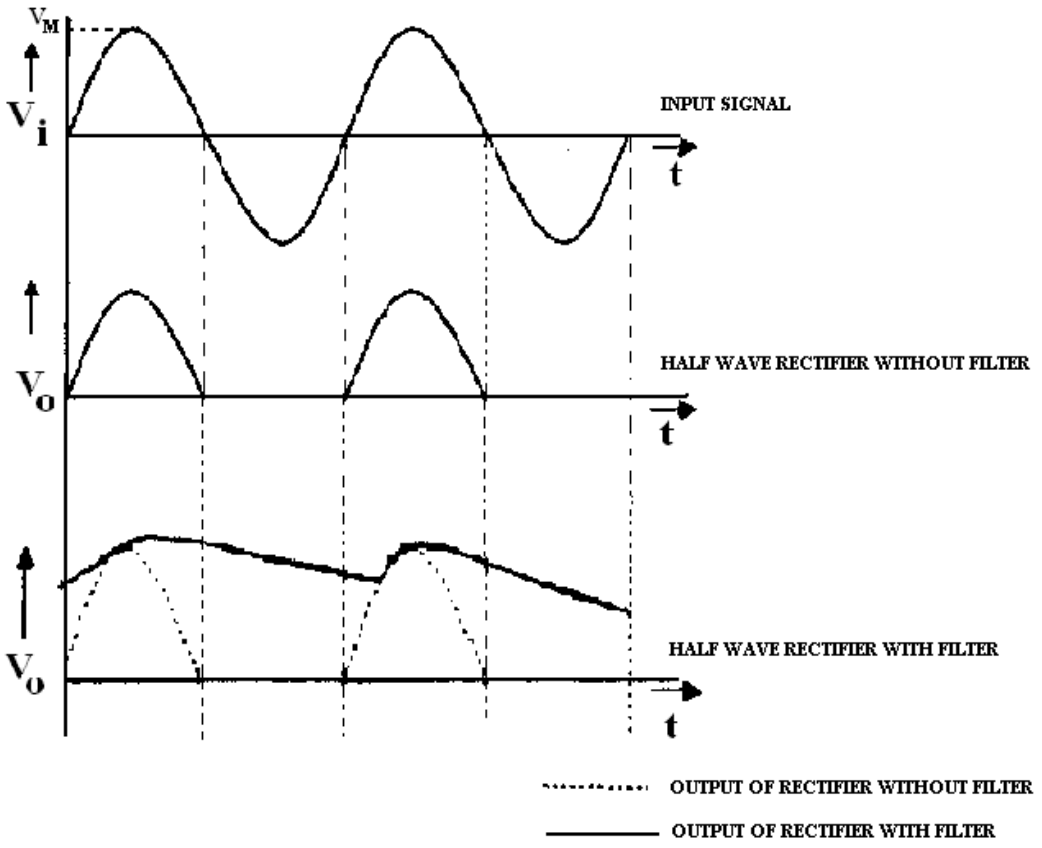
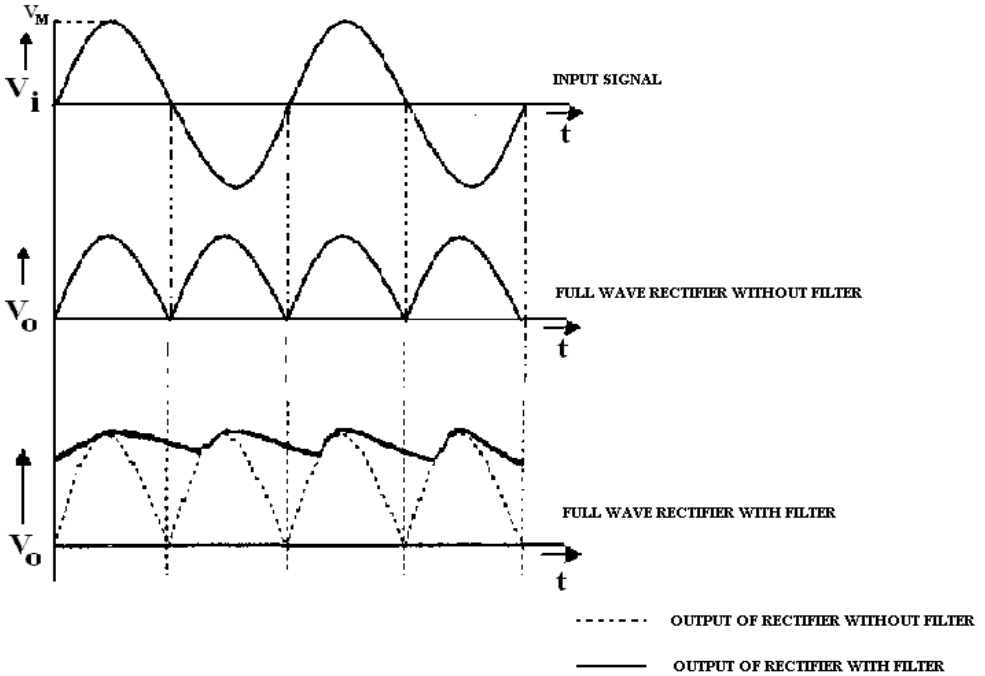


Figure (d): Full Wave Rectifier with Filter

3.6 EXPECTED GRAPHS



OUTPUT OF RECTIFIER WITH FILTER



3.7 PRECAUTIONS

1. No loose contacts at the junctions.
2. Meters of correct ranges must be used for precision

3.8 TABULAR COLUMNS

Half Wave Rectifier without Filter

S. N o	Load Resistance (R_L)	Input Voltage Peak (V_m)	Output Voltage Peak (V_o)	Average dc current (I_{dc})	Average Dc voltage (V_{dc})	RMS Voltage (V_{ac})	Ripple Factor (Γ)
1.	1KΩ						
2.	10KΩ						

Half Wave Rectifier with Filter C=100μF

S. N o	Load Resistanc e (R_L)	Input Voltage Peak	Output Voltage Peak (V_o)	Average dc current (I_{dc})	Average Dc voltage (V_{dc})	RMS Voltage (V_{ac})	Ripple Factor (Γ) ___
1.	1KΩ	(m					
2.	10KΩ						

Full wave Rectifier (Center-tap) Without Filter

S. No	Load Resistance (R_L)	Input Voltage Peak (V_m)	Output Voltage Peak (V_o)	Average dc current (I_{dc})	Average Dc voltage (V_{dc})	RMS Voltage (V_{ac})	Ripple Factor $\gamma=\frac{V_{ac}}{V_{Dc}}$
1	1KΩ						
2	10KΩ						

Full wave Rectifier (Center-tap) With Filter C = 100µF

S.No	Load Resistance (R_L)	Input Voltage Peak (V_m)	Output Voltage Peak (V_o)	Average dc current (I_{dc})	Average Dc voltage (V_{dc})	RMS Voltage (V_{ac})	Ripple Factor $\gamma = \frac{V_{ac}}{V_{Dc}}$
1	1KΩ						
2	10K						

3.12 RESULT

1. Input and Output waveforms of a half-wave and full wave rectifier with /without filter are
   observed and plotted.
2. For Half-wave rectifier without filter-

   γ, Ripple factor at
   1KΩ=
   10 KΩ=

3. For Half-wave rectifier with filter:-

   γ, Ripple factor at 1KΩ,
   100µF =
   10 KΩ, 100µF =

4. For Full-wave rectifier without filter-

   γ, Ripple factor at
   1KΩ=
   10 KΩ=

5. For Full-wave rectifier with filter:-

   γ, Ripple factor at 1KΩ, 100µF =
   10 KΩ, 100µF =

3.10 LAB ASSIGNMENT

Plot the wave forms of Half wave rectifier with RL=5000 ohms, C = 680µF.

3.11 LAB QUESTIONS

1. Draw the o/p wave form without filter?
2. Draw the o/p wave form with filter?
3. What is meant by ripple factor? For a good filter whether ripple factor should be high or low?
4. What happens to the o/p wave form if we increase the capacitor value?
5. What happens if we increase the capacitor value?

EXPERIMENT No 4

TRANSISTOR CE CHARACTERISTICS

4.1 AIM

Plot the input and output characteristics of a transistor connected in Common Emitter configuration.

Calculate the input resistance R_i at I_B= 20 µA, output resistance R_o at V_{CE}=10V and current gain at V_{CE} =10V.

4.2 COMPONENTS & EQUIPMENT REQUIRED

S.No	Device	Range /Rating	Quantity (in No.s)
1.	Transistor CE trainer Board Containing		
	a) DC Power Supply.	(0-12) V	2
	b) PNP Transistor	BC 107	1
	c) Carbon Film Resistor	470Ω, 1/2 W	1
		100KΩ,1/2 W	1
2.	a) DC Voltmeter	(0-1) V	1
	b)DC Voltmeter	(0-20) V	1
3.	DC Ammeter	(0-50) mA	1
		(0-200) µA	1
4.	Connecting wires	5A	12

4.3 THEORY

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals.

Therefore the emitter terminal is common to both input and output.

The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement I_B increases less rapidly with V_{BE} . Therefore input resistance of CE circuit is higher than that of CB circuit.

The output characteristics are drawn between I_c and V_{CE} at constant I_B. the collector current varies with V_{CE} unto few volts only. After this the collector current becomes almost constant, and

independent of $V_{CE.}$ The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_C is always constant and is approximately equal to $I_{B.}$

The current amplification factor of CE configuration is given by

$$B = \Delta I_C / \Delta I_B$$

4.4 PROCEDURE

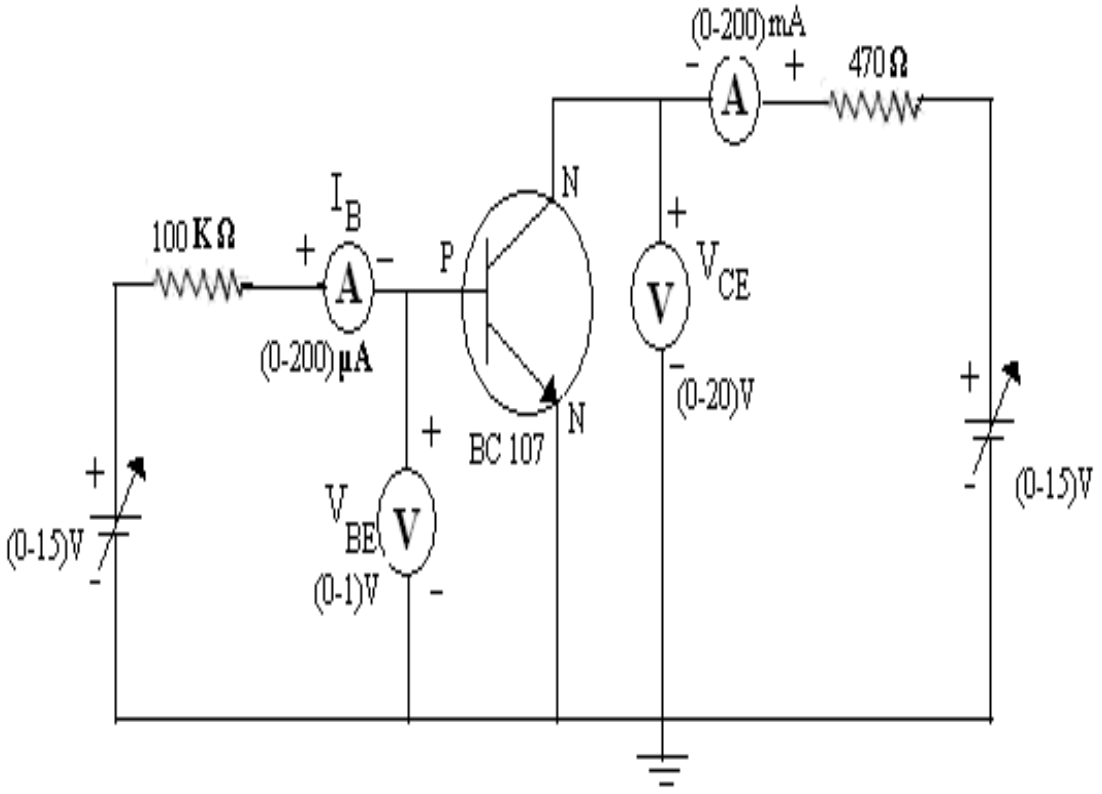
Input Characteristics:

1. Connect the transistor as shown in figure.
2. Keep the V_{CE} constant at 2V and 6V.
3. Vary the I_B in steps and note down the corresponding V_{EB} values as per tabular column.

Output Characteristics:

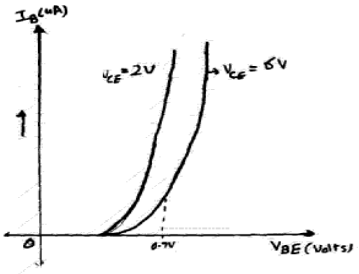
1. Keep the I_B constant at 20 μA and 40 μA.
2. Vary the V_{CE} in steps and note corresponding I_C values.
3. Readings are tabulated as shown in tabular column.

4.5 CIRCUIT DIAGRAM

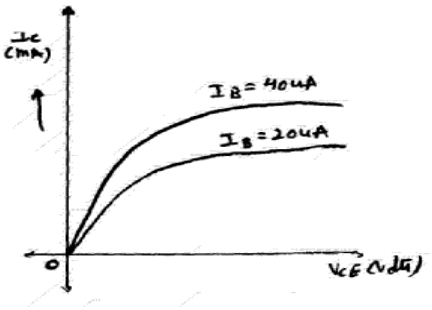


4.6 EXPECTED GRAPHS

Input Characteristics



Output Characteristics



4.7 PRECAUTIONS

1. Keep the knobs of supply voltages V_{BE} & V_{CE} at minimum positions when switching ON or switching OFF the power supply.
2. No loose contacts at the junctions.
3. Do not overload the meters above its rated ranges.

4.8 TABULAR COLUMN

Input Characteristics

V_{CB} = 2V		V_{CB} = 6V	
V_{BE} (Volts)	I_B (µA)	V_{BE} (Volts)	I_B (µA)

Output Characteristics

I_B = 20µA		I_B = 40µA	
V_{CE} (Volts)	I_C (mA)	V_{CE} (Volts)	I_C (mA)

4.9 CALCULATIONS

Input Resistance (I_B=20μA) = $\Delta V_{BE}/\Delta I_B$ =

At V_{CE} = 2V

Input Resistance (I_B =20μA) = $\Delta V_{BE}/\Delta I_B$ =

At V_{CE}= 6V

Output resistance (V_{CE}=10V) = $\Delta V_{CE}/\Delta I_C$ =

At I_B=20μA

Output resistance (V_{CE}=10V) = $\Delta V_{CE}/\Delta I_C$ =

At I_B=20μA

Current Amplification Factor „β"= $\Delta I_C/\Delta I_B$ =

4.10 RESULT

1. Input and Output curves are plotted.
2. R_i, Input Resistance:
    a. V_{CE} = 2V and I_B =20 μA, R_i =
    b. V_{CE} = 6V and I_B =20 μA, R_i =
3. R_o, Output Resistance:
    a. V_{CE}= 10V and I_B = 20μA, R_o =
    b. V_{CE} = 10V and I_B = 40μA, R_o =
4. Current Amplification factor

    „β" = (at V_{CE} =10V)

4.11 H-PARAMETER CALCULATIONS

$h_{ie} = \Delta V_{be} / \Delta I_b$ =

$h_{oe} = \Delta I_c / \Delta V_{ce}$ =

$h_{fe} = \Delta I_c / \Delta I_b$ =

$h_{re} = \Delta V_{be} / \Delta V_{ce}$

4.12 LAB ASSIGNMENT

Plot the I/O characteristics of CE configuration for Vcc = 10V, VBB = 4V, Rb= 200K ohms, Rc = 2K ohms, β = 200, Vbe = 0.7V.

4.13 LAB QUESTIONS

1. Define current gain in CE configuration?
2. Why CE configuration is preferred for amplification?
3. What is the phase relation between input and output?
4. Draw diagram of CE configuration for PNP transistor?
5. What is the power gain of CE configuration?
6. What are the applications of CE configuration?

EXPERIMENT No 5

TRANSISTOR CB CHARACTERISTICS

5.1 AIM

Plot the input and output characteristics of a transistor connected in Common Base configuration. Calculate the input resistance R_i at I_e= 12 mA, output resistance R_o at V_{CB}=8V and current gain at V_{CB}=6V.

5.2 COMPONENTS & EQUIPMENT REQUIRED

S.No	Device	Range /Rating	Quantity (in No.s)
1.	Transistor CB trainer Board Containing		
	a) DC Power Supply.	(0-12) V	2
	b) PNP Transistor	CK100	1
	c) Carbon Film Resistor	470Ω, 1/2 W	2
2.	a) DC Voltmeter	(0-1) V	1
	b) DC Voltmeter	(0-20) V	1
3.	DC Ammeter	(0-50) mA	2
4.	Connecting wires	5A	12

5.3 THEORY

A transistor is a three terminal active device. T he terminals are emitter, base, collector. In CB configuration, the base is common to both input (emitter) and output (collector). For normal operation, the E-B junction is forward biased and C-B junction is reverse biased.

In CB configuration, I_E is +ve, I_C is –ve and I_B is –ve.

So, $V_{EB}=f1\ (V_{CB},I_E)$ and $I_C=f2\ (V_{CB},I_B)$

With an increasing the reverse collector voltage, the space-charge width at the output junction increases and the effective base width „W" decreases. This phenomenon is known as "Early effect". Then, there will be less chance for recombination within the base region. With increase of charge gradient within the base region, the current of minority carriers injected across the emitter junction increases. The current amplification factor of CB configuration is given by,

$$\alpha = \Delta I_C / \Delta I_E$$

5.4 PROCEDURE

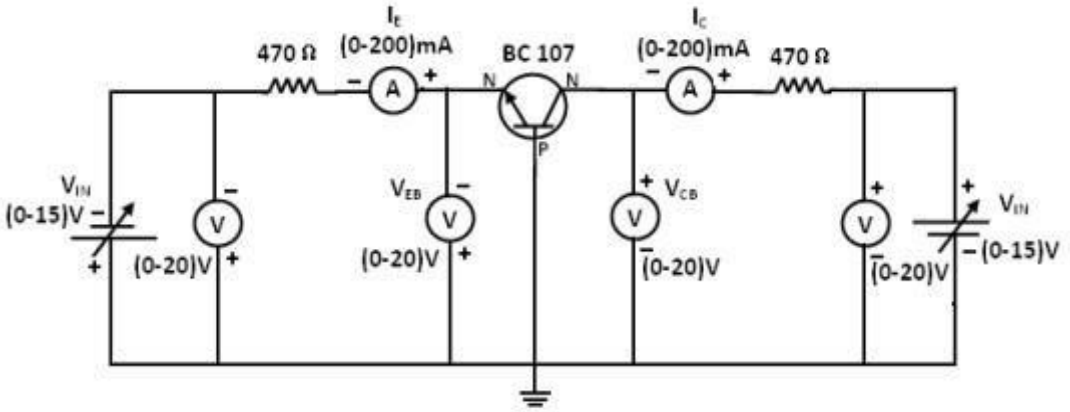
Input Characteristics:

1. Connect the transistor as shown in figure.
2. Keep the V_{CB} constant at 4V and 8V.Vary the V_{EB} in steps and note corresponding I_E values as per tabular form.

Output Characteristics:

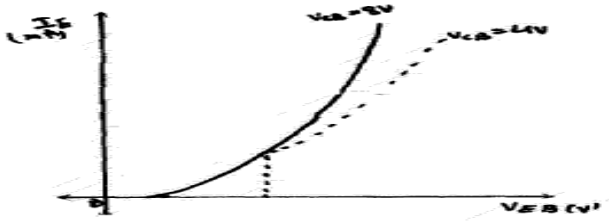
1. Keep the I_E constant at 4mA and 8mA.Vary the V_{CB} in steps and note corresponding I_C values.
2. Readings are tabulated as shown in tabular column.

5.5 CIRCUIT DIAGRAM

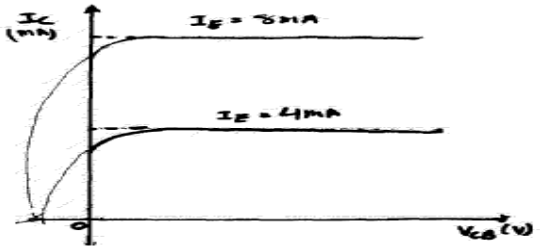


5.6 EXPECTED GRAPHS

Input Characteristics



Output characteristics



5.7 PRECAUTIONS

1. Keep the knobs of supply voltages V_{EB} & V_{CB} at minimum positions when switching ON or switching OFF the power supply.
2. No loose contacts at the junctions.
3. Do not overload the meters above its rated ranges.

5.8 TABULAR COLUMN

Input Characteristics

V_{CB} = -4V		V_{CB} = -8V	
V_{EB} (Volts)	I_E (mA)	V_{EB} (Volts)	I_E (mA)

Output Characteristics

I_E = 8mA		I_E = 4mA	
V_{CB} (Volts)	I_C (mA)	V_{CB}(Volts)	I_C(mA)

5.9 CALCULATIONS

Input Resistance (I_E =12 mA) = $\Delta V_{EB}/\Delta I_E$ =

At V_{EB} = 4V

Input Resistance (I_E =12 mA) = $\Delta V_{EB}/\Delta I_E$ =

At V_{EB} = 8V

Output resistance (I_E =8mA) = $\Delta V_{CB}/\Delta I_C$ =

At V_{CB} = -8V.

Output resistance (I_E =4mA) = $\Delta V_{CB}/\Delta I_C$ =

At V_{CB} = -8V.

Current Amplification Factor „α" = $\Delta I_C/\Delta I_E$ =

5.10 H-parameter calculations

$h_{ib} = \Delta V_{eb} / \Delta I_e =$

$h_{ob} = \Delta I_c / \Delta V_{cb} =$

$h_{fb} = \Delta I_c / \Delta I_e =$

$h_{rb} = \Delta V_{eb} / \Delta V_{cb} =$

5.14 RESULT

Input and output curves are plotted.

1. R_i Input Resistance:
   (i) V_{EB} = 4V and I_E =12 mA, R_i =
   (ii) V_{EB} = 8V and I_E =12 mA, R_i =
2. R_o Output Resistance:
   (i) V_{CB} = 8V and I_E = 8 mA, R_o =
   (ii) V_{CB} = 8V and I_E = 4 mA, R_o =
3. Current Amplification factor

„α" =

(at V_{CB} =6V)

5.12 LAB ASSIGNMENT

Plot the I/O characteristics of CB configuration for Vcc = 12V, VEE = 6V, RE= 100K ohms, Rc = 1K ohms, α =0.98, Vbe = 0.7V.

5.13 LAB QUESTIONS

1. What are the applications of CB configuration?
2. What are the input and output impedances of CB configuration?
3. Define α(alpha)?
4. What is EARLY effect?
5. What is the power gain of CB configuration

EXPERIMENT NO: 6

FREQUENCY RESPONSE CE AMPLIFIER

6.1 AIM

Plot the frequency response of CE amplifier and calculate gain bandwidth.

6.2 COMPONENTS & EQUIPMENTS REQUIRED

S.No	Device	Range/Rating	Quantity (in No.s)
1	CE Amplifier trainer Board with		
	(a) DC power supply	12V	1
	(b) DC power supply	5V	1
	(c) NPN transistor	BC 107	1
	(d) Carbon film resistor	100KΩ, 1/2W	1
	(e) Carbon film resistor	2.2KΩ, 1/2W	1
	(f) Capacitor	0.1μF	2
2	Function Generator	0.l Hz- 1MHz	1
3	Dual trace C.R.O	0-20MHz	1
4	Connecting Wires	5A	4

6.3 THEORY

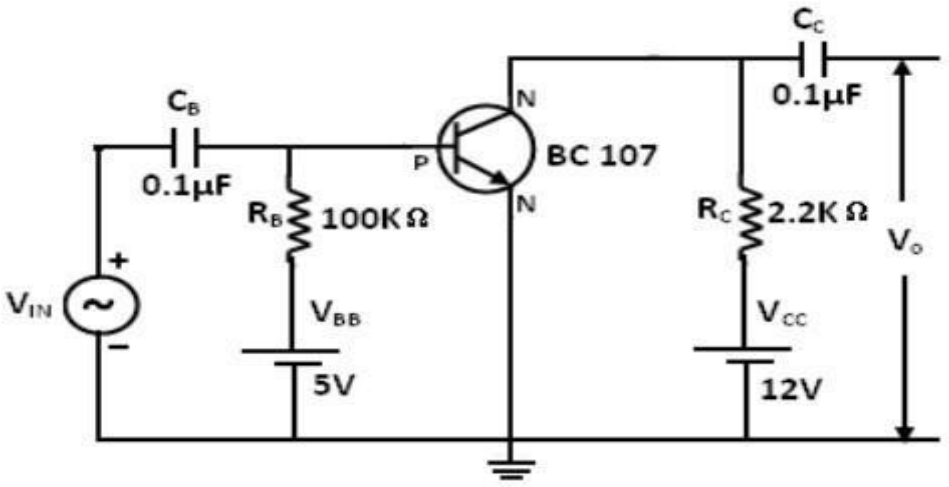
The CE amplifier provides high gain &wide frequency response. The emitter lead is common to both input & output circuits and is grounded. The emitter-base circuit is forward biased. The collector current is controlled by the base current rather than emitter current. The input signal is applied to base terminal of the transistor and amplifier output is taken across collector terminal. A very small change in base current produces a much larger change in collector current. When +VE half-cycle is fed to the input circuit, it opposes the forward bias of the circuit which causes the collector current to decrease, it decreases the voltage more –VE. Thus when input cycle varies through a -VE half-cycle, increases the forward bias of the circuit, which causes the collector current to increases thus the output signal is common emitter amplifier is in out of phase with the input signal.

$$\text{Bandwidth} = f_H - f_L$$

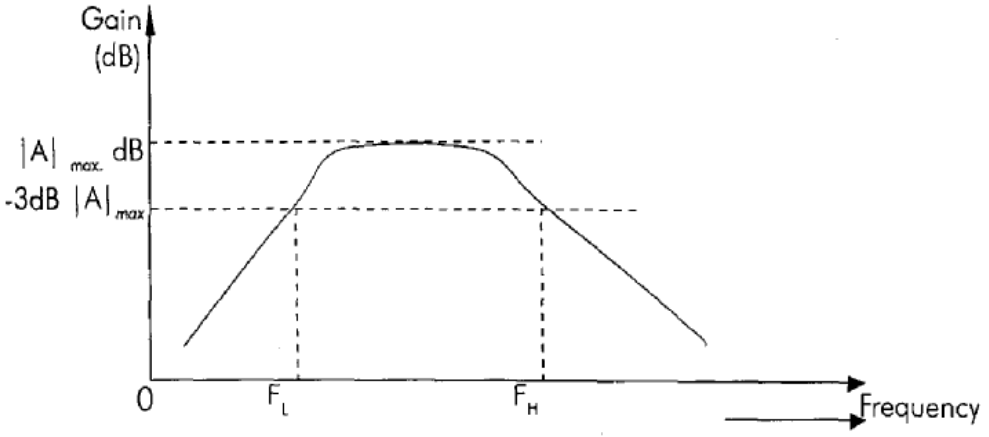
6.4 PROCEDURE

1. Connect the circuit diagram as shown in figure.
2. Adjust input signal amplitude in the function generator and observe an amplified voltage at the output without distortion.
3. By keeping input signal voltages at 50mV, vary the input signal frequency from 0 to 1MHz in steps as shown in tabular column and note the corresponding output voltage

6.5 CIRCUIT DIAGRAM



6.6 EXPECTED GRAPH



6.7 PRECAUTIONS

1. Oscilloscope probes negative terminal should be at equipotential points (i.e. ground voltage= 0), because both terminals are internally shorted in dual trace oscilloscope.
2. Ensure that output voltage is exactly an amplified version of input voltage without any distortion (adjust input voltage amplitude to that extent).
3. No loose connections at the junctions.

6.8 TABULAR COLUMN

Input voltage: $V_i = 50mV$

Frequency (in Hz)	**Output (V_o) (Peak to Peak)**	**Gain $A_V=V_0/Vi$**	**Gain (in dB) = 20 log $_{10}$ V_O/ V_i**
20			
600			
1K			
2K			
4K			
8K			
10K			
20K			
30K			
40K			
50K			
60K			
80K			
100K			
250K			
500K			
750K			
1000K			

6.9 RESULT

Frequency response of CE amplifier is

plotted. Gain, A_V = _____dB.

Bandwidth= f_H-f_L =_____

6.10 LAB ASSIGNMENT

Draw the frequency response of CE amplifier using R_B =1000 ohms , R_{CE} = 4000 ohms.

6.11 LAB QUESTIONS

1. How much phase shift for CE Amplifier?
2. What are the applications?
3. Draw the Equivalent circuit for low frequencies?

EXPERIMENT No. 7

BOOLEAN EXPRESSIONS USING GATES

7.1 AIM: To study and verify the truth table of basic Boolean expressions using logic gates.

7.2 LEARNING OBJECTIVE:

Identify various ICs and their specification.

7.3 COMPONENTS REQUIRED:

Logic gates (IC) trainer kit.

Connecting patch chords.

IC 7400, IC 7408, IC 7432, IC 7406, IC 7402, IC 7404, IC 7486

7.4 THEORY:

The basic logic gates are the building blocks of more complex logic circuits. These logic gates perform the basic Boolean functions, such as AND, OR, NAND, NOR, Inversion, Exclusive-OR, Exclusive-NOR. Fig. below shows the circuit symbol, Boolean function, and truth. It is seen from the Fig that each gate has one or two binary inputs, A and B, and one binary output, C. The small circle on the output of the circuit symbols designates the logic complement. The AND, OR, NAND, and NOR gates can be extended to have more than two inputs. A gate can be extended to have multiple inputs if the binary operation it represents is commutative and associative. These basic logic gates are implemented as small-scale integrated circuits (SSICs) or as part of more complex medium scale (MSI) or very large-scale (VLSI) integrated circuits. Digital IC gates are classified not only by their logic operation, but also the specific logic-circuit family to which they belong. Each logic family has its own basic electronic circuit upon which more complex digital circuits and functions are developed. The following logic families are the most frequently used.

TTL -Transistor-transistor logic

ECL -Emitter-coupled logic

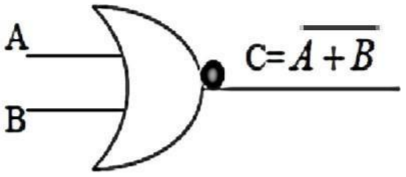
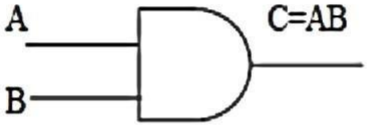
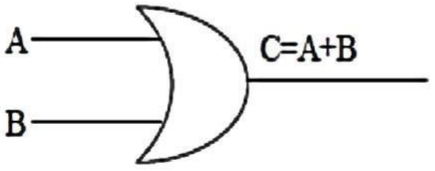
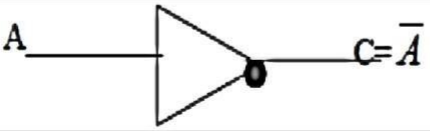
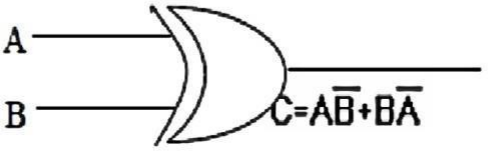
MOS-Metal-oxide semiconductor

CMOS-Complementary metal-oxide semiconductor

TTL and ECL are based upon bipolar transistors. TTL has a well-established popularity among logic families. ECL is used only in systems requiring high-speed operation. MOS and CMOS, are based on field effect transistors. They are widely used in large scale integrated circuits because of their high component density and relatively low power consumption. CMOS logic consumes far less power than MOS logic. There are various commercial integrated circuit chips available. TTL ICs are usually distinguished by numerical designation as the 5400 and 7400 series.

7.5 PROCEDURE:

1. Check the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make connections as shown in the circuit diagram.
4. Provide the input data via the input switches and observe the output on output LEDs

S.NO	GATE	SYMBOL	INPUTS		OUTPUT
			A	B	C
1.	NAND IC 7400		0	0	1
			0	1	1
			1	0	1
			1	1	0
2.	NOR IC 7402		0	0	1
			0	1	0
			1	0	0
			1	1	0
3.	AND IC 7408		0	0	0
			0	1	0
			1	0	0
			1	1	1
4.	OR IC 7432		0	0	0
			0	1	1
			1	0	1
			1	1	1
5.	NOT IC 7404		1	-	0
			0	-	1
6.	EX-OR IC 7486		0	0	0
			0	1	1
			1	0	1
			1	1	0

7.6 Result:

7.7 LAB QUESTIONS:

1. Why NAND & NOR gates are called universal gates?
2. Realize the EX – OR gates using minimum number of NAND gates.
3. Give the truth table for EX-NOR and realize using NAND gates?
4. What are the logic low and High levels of TTL IC"s and CMOS IC"s?
5. Compare TTL logic family with CMOS family?
6. Which logic family is fastest and which has low power dissipation?

EXPERIMENT No. 8

BOOLEAN EXPRESSIONS USING GATES

8.1 AIM: To study the realization of basic gates using universal gates. Understanding how to construct any combinational logic function using NAND or NOR gates only.

8.2 COMPONENTS REQUIRED:

IC 7402(NOR), IC 7400(NAND), 7404(NOT), 7408(AND), 7432(OR), KL 33002, power supply, connecting wires and Breadboard etc.

8.3 THEORY:

AND, OR, NOT are called basic gates as their logical operation cannot be simplified further. **NAND and NOR** are called universal gates as using only NAND or only NOR, any logic function can be implemented. Using NAND and NOR gates and **De Morgan's Theorems** different basic gates & EX-OR gates are realized.

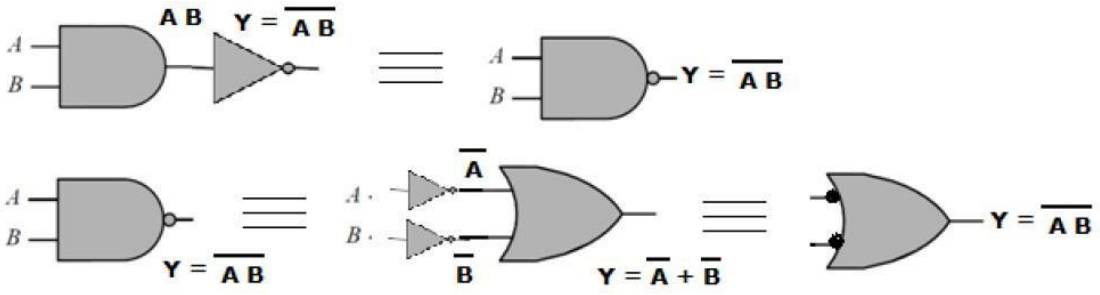
De Morgan`s Law:

In formal logic, De Morgan's laws are rules relating the logical operators "AND" and "OR" in terms of each other via negation. With two operands A and B:

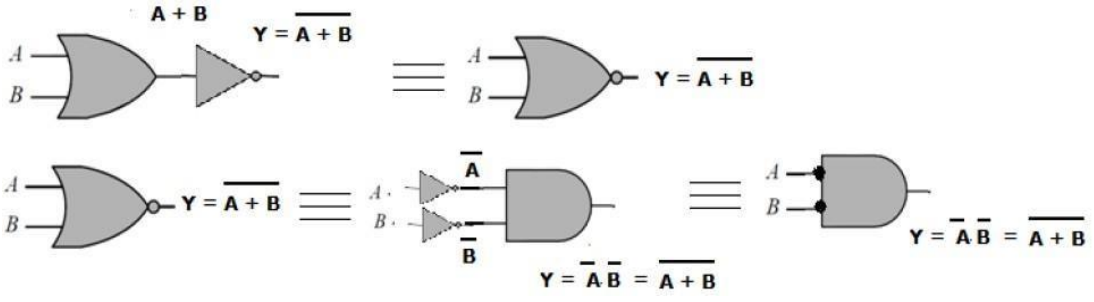
1. $\overline{A.B} = \overline{A} + \overline{B}$

2. $\overline{A+B} = \overline{A} . \overline{B}$

- The NAND gate is equivalent to an OR gate with the bubble at its inputs which are as shown.



- The NOR gate is equivalent to an AND gate with the bubble at its inputs which are as shown.

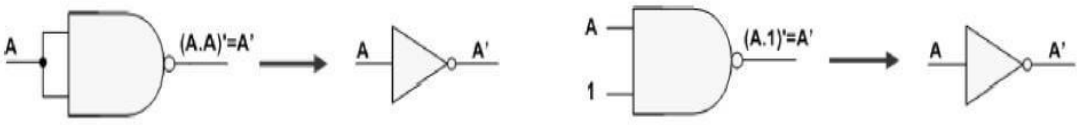


Designing the Solution:

❖ **NAND**

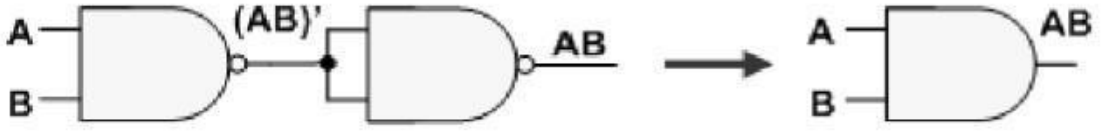
- **IMPLEMENTING INVERTER USING NAND GATE :**

The figure shows two ways in which a NAND gate can be used as an inverter (NOT gate).
1. All NAND input pins connect to the input signal A gives an output A'.
2. One NAND input pin is connected to the input signal A while all other input pins are connected to logic 1. The output will be A'.



- **IMPLEMENTING AND USING NAND GATE:**

An AND gate can be replaced by NAND gates as shown in the figure (The AND is replaced by a NAND gate with its output complemented by a NAND gate inverter).

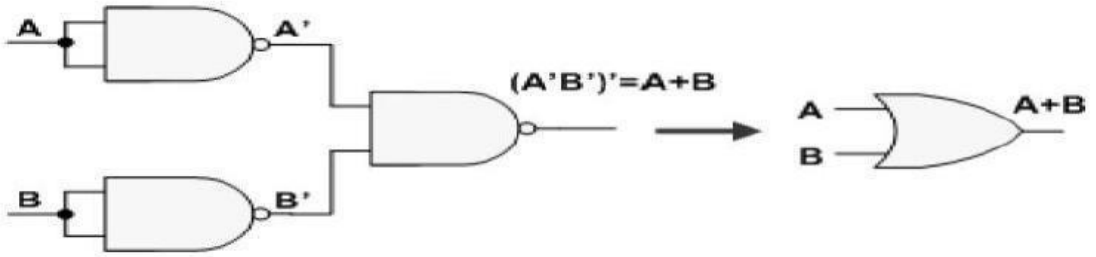


- **IMPLEMENTING OR USING NAND GATE :**

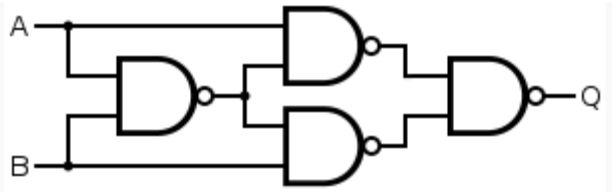
An OR gate can be replaced by NAND gates as shown in the figure (The OR gate is replaced by a NAND gate with all its inputs complemented by NAND gate inverters).

From De Morgan`s law we see that:

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$ Now invert the two sides we get: $$A+B = \overline{\overline{A} \cdot \overline{B}}$$

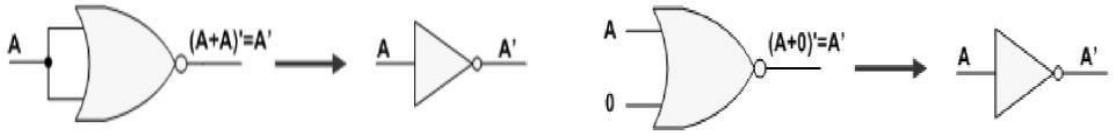


- **IMPLEMENTING XOR USING NAND GATE:**
  - $A \oplus B = A'B + AB'$

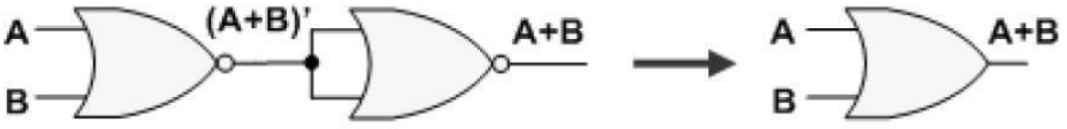


❖ **NOR**

- **IMPLEMENTING INVERTER USING NOR GATE:**
  - The figure shows two ways in which a NOR gate can be used as an inverter (NOT gate).
  - All NOR input pins connect to the input signal A gives an output A'.
  - One NOR input pin is connected to the input signal A while all other input pins are connected to logic 0. The output will be A'.
  -



- **IMPLEMENTING OR USING NOR GATE:**
  - An OR gate can be replaced by NOR gates as shown in the figure (The OR is replaced by a NOR gate with its output complemented by a NOR gate inverter)

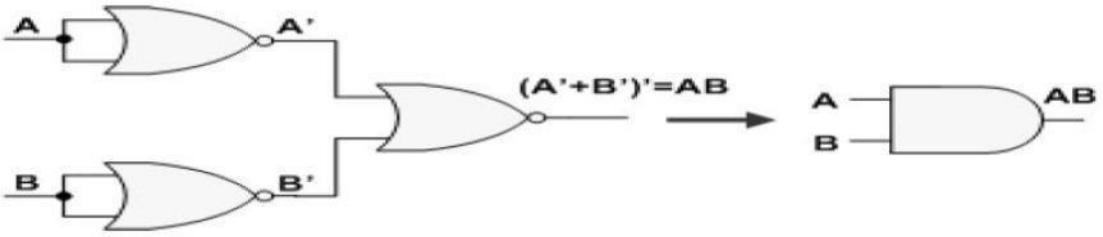


- **IMPLEMENTING AND USING NOR GATE:**

  - An AND gate can be replaced by NOR gates as shown in the figure (The AND gate is replaced by a NOR gate with all its inputs complemented by NOR gate inverters)

From De Morgan`s law we see that: $\overline{A \cdot B} = \overline{A} + \overline{B}$

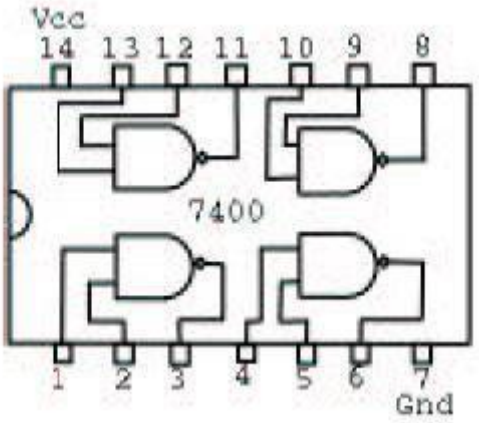
Now invert the two sides we get: $A \cdot B = \overline{\overline{A} + \overline{B}}$



8.4 IMPLEMENTATION:

Part 1: Implementation using NAND

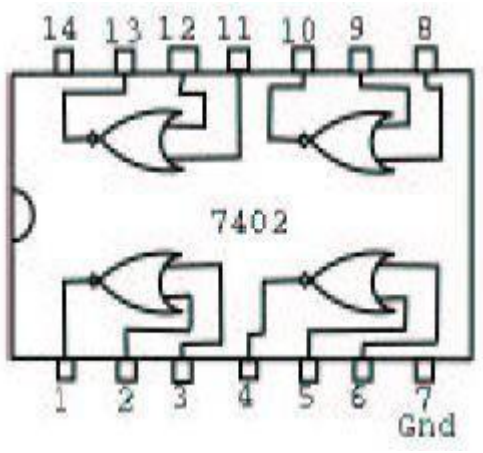
- Construct (inv, AND, OR, XOR) gates and check its truth table using NAND ICs(7400) only.



- Repeat using KL 33002 block b.

Part 2: Implementation using NOR

- Construct (inv, OR, AND) gates and check its truth table using NOR ICs(7402) only.



- Repeat using KL 33002 block a.

8.5. RESULT:

8.6 LAB QUESTIONS:

a) Construct X-NOR gate using a NOR gate.

b) Build an inverter using XOR gate.

c) Implement the following function with NAND gates only: F=

$$\bar{x}y + x\bar{y} + z$$

EXPERIMENT No. 9

NAND/NOR GATES

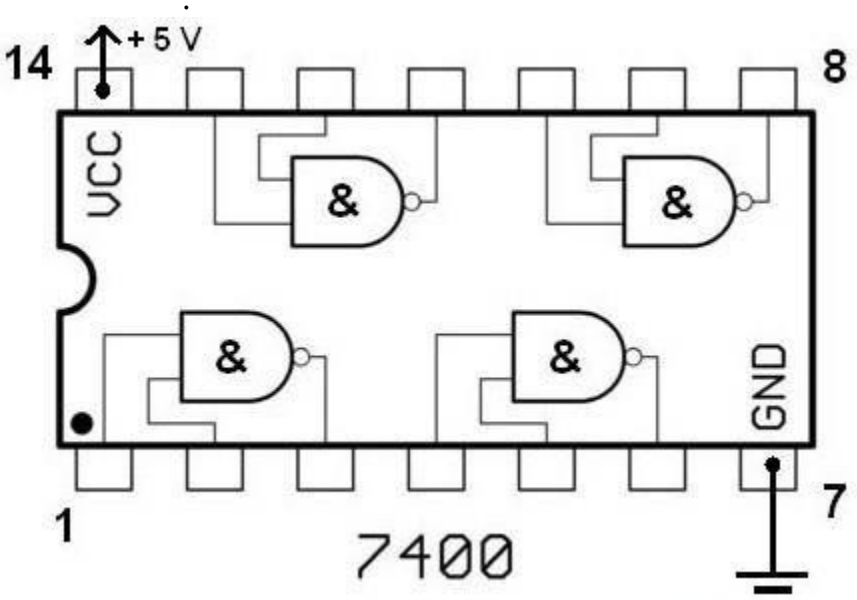
9.1 AIM: To realize clock generator using NAND/NOR gates.

9.2 COMPONENTS REQUIRED:

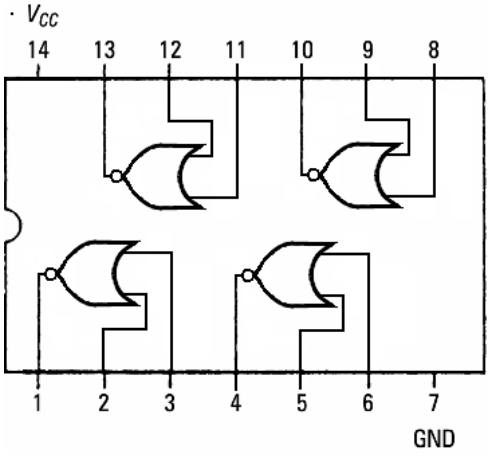
IC 7400, IC 7402, 1K Resistor, 100 mu F capacitor, Patch Cords & IC Trainer Kit.

9.3 THEORY:

7400 IC: This IC is a combination of 4 NAND gates. This circuit in combination with Resistor and capacitor are used to generate clock pulses

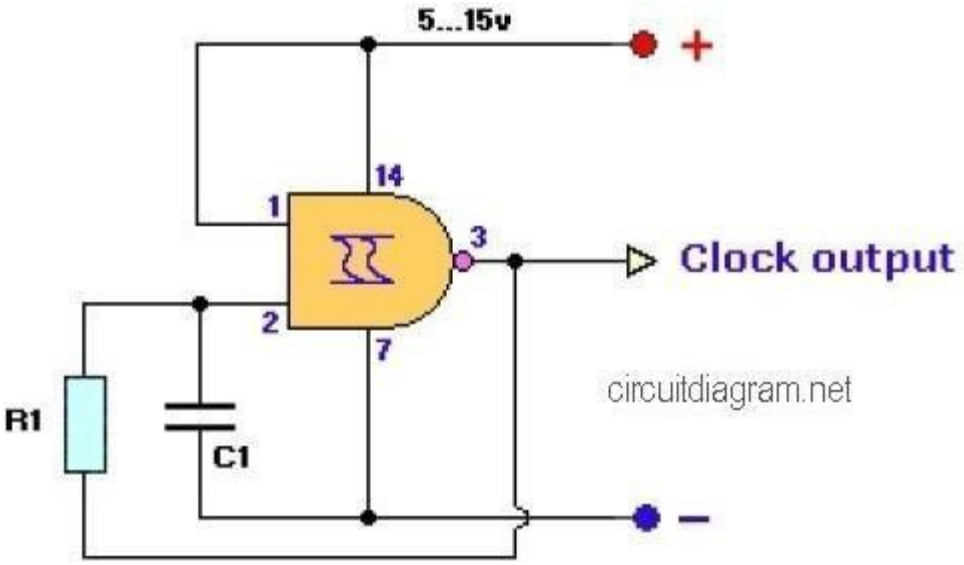


7402 IC: This IC is a combination of 4 NOR gates. This circuit in combination with Resistor and capacitor are used to generate clock pulses.



9.4 PROCEDURE:

1. Connect the circuit as shown in the circuit diagram below and observe the generation of clock pulses.
2. Repeat the procedure for 7402 IC and observe the clock pulses.



9.5 RESULT:

9.6 LAB QUESTIONS:

1. What is a clock pulse?
2. What are characteristics of clock pulse?
3. What is negative triggered clock pulse?
4. What is positive triggered clock pulse?

EXPERIMENT No. 10

ADDERS AND SUBTRACTORS

10.1 AIM: To realize

i) Half Adder and Full Adder

ii) Half Subtractor and Full Subtractor by using Basic gates and NAND gates

10.2 LEARNING OBJECTIVE:

To realize the adder and subtractor circuits using basic gates and universal gates

To realize full adder using two half adders

To realize a full subtractor using two half subtractors

10.3 COMPONENTS REQUIRED:

IC 7400, IC 7408, IC 7486, IC 7432, Patch Cords & IC Trainer Kit.

10.4 THEORY:

Half-Adder: A combinational logic circuit that performs the addition of two data bits, A and B, is called a half-adder. Addition will result in two output bits; one of which is the sum bit, S, and the other is the carry bit, C. The Boolean functions describing the half-adder are:

$S = A \oplus B$ $\qquad\qquad$ $C = A\,B$

Full-Adder: The half-adder does not take the carry bit from its previous stage into account. This carry bit from its previous stage is called carry-in bit. A combinational logic circuit that adds two data bits, A and B, and a carry-in bit, Cin , is called a full-adder. The Boolean functions describing the full-adder are:

$S = (x \oplus y) \oplus Cin$ $\qquad\qquad$ $C = xy + Cin\,(x \oplus y)$

Half Subtractor: Subtracting a single-bit binary value B from another A (i.e. A -B) produces a difference bit D and a borrow out bit B-out. This operation is called half subtraction and the circuit to realize it is called a half subtractor. The Boolean functions describing the half-Subtractor are:

$S = A \oplus B$ $\qquad\qquad$ $C = A'\,B$

Full Subtractor: Subtracting two single-bit binary values, B, Cin from a single-bit value A produces a difference bit D and a borrow out Br bit. This is called full subtraction. The Boolean functions describing the full-subtractor are:

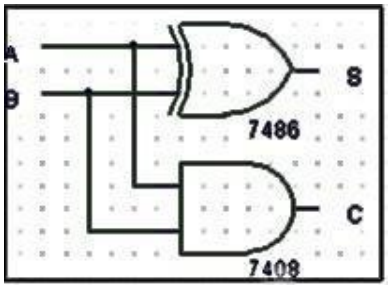
$D = (x \oplus y) \oplus Cin$ $\qquad\qquad$ $Br = A'B + A'(Cin) + B(Cin)$

10.5 PROCEDURE:

- Check the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

10.6 CIRCUIT DIAGRAM:

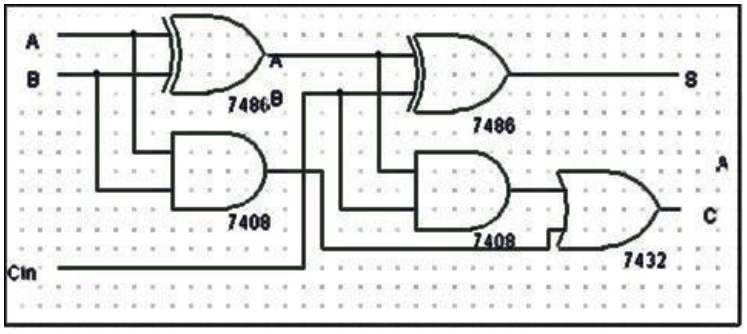
Half Adder:



Truth Table:

INPUTS		OUTPUTS	
A	**B**	**S**	**C**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

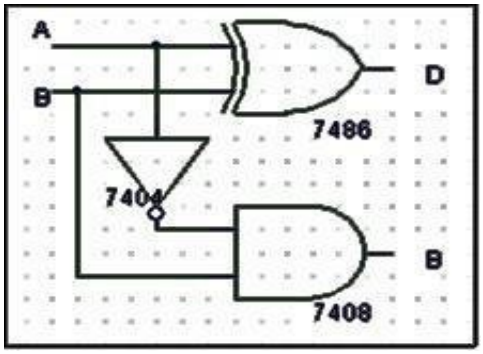
Full Adder using basic gates:



TRUTH TABLE

INPUTS			OUTPUTS	
A	**B**	**Cin**	**S**	**C**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Half Subtractor using basic gates:

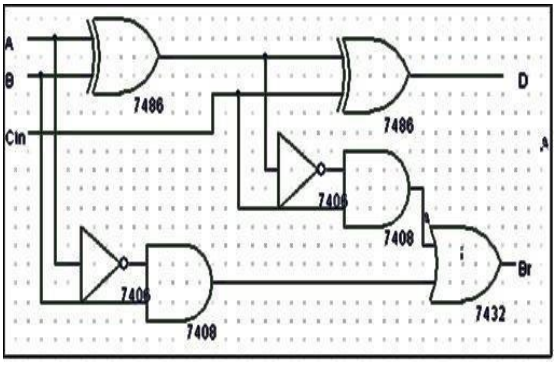


Truth Table

INPUTS		OUTPUTS	
A	B	D	Br
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Full Subtractor:

Truth Table:



INPUTS			OUTPUTS	
A	B	Cin	D	Br
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

10.7 RESULT:

10.8 VIVA QUESTIONS:

1) What is a half adder?
2) What is a full adder?
3) What are the applications of adders?
4) What is a half subtractor?
5) What is a full subtractor?

EXPERIMENT No. 11

BINARY TO GRAY CODE CONVERTER

11.1 AIM: To realize Binary to Gray code converter.

11.2 LEARNING OBJECTIVE:

To learn the importance of non-weighted code
To learn to generate gray code

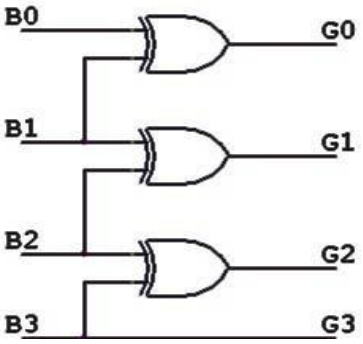
11.3 COMPONENTS REQUIRED:

IC 7400, IC 7486, and IC 7408, Patch Cords & IC Trainer Kit

11.4 PROCEDURE:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

11.5 Circuit Diagram:



Binary to Gray Code Using Ex-Or Gates

Binary				Gray			
B3	**B2**	**B1**	**B0**	**G3**	**G2**	**G1**	**G0**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

11.6 RESULT:

11.7 VIVA QUESTIONS:

1. What are code converters?
2. What is the necessity of code conversions?
3. What is gray code?
4. Realize the Boolean expressions for
   a) Binary to gray code conversion
   b) Gray to binary code conversion

EXPERIMENT No. 12

VERIFICATION OF TRUTH TABLES AND EXCITATION TABLES

12.1 AIM: Truth Table verification of

1) RS Flip Flop
2) T type Flip Flop.
3) D type Flip Flop.
4) JK Flip Flop.
5) JK Master Slave Flip Flop.

12.2 LEARNING OBJECTIVE:

To learn about various Flip-Flops
To learn and understand the working of Master slave FF
To learn about applications of FFs
Conversion of one type of Flip flop to another

12.3 COMPONENTS REQUIRED:

IC 7408, IC 7404, IC 7402, IC 7400, Patch Cords & IC Trainer Kit.

12.4 THEORY:

Logic circuits that incorporate memory cells are called *sequential logic circuits*; their output depends not only upon the present value of the input but also upon the previous values.

Sequential logic circuits often require a timing generator (a clock) for their operation. The latch (flip-flop) is a basic bi-stable memory element widely used in sequential logic circuits. Usually there are two outputs, Q and its complementary value. Some of the most widely used latches are listed below.

SR LATCH:

An S-R latch consists of two cross-coupled NOR gates. An S-R flip-flop can also be design using cross-coupled NAND gates as shown. The truth tables of the circuits are shown below.

A clocked S-R flip-flop has an additional clock input so that the S and R inputs are active only when the clock is high. When the clock goes low, the state of flip-flop is latched and cannot change until the clock goes high again. Therefore, the clocked S-R flip-flop is also called "enabled" S-R flip-flop.

A D latch combines the S and R inputs of an S-R latch into one input by adding an inverter. When the clock is high, the output follows the D input, and when the clock goes low, the state is latched.

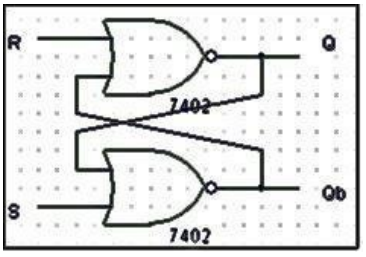
A S-R flip-flop can be converted to T-flip flop by connecting S input to Qb and R to Q.

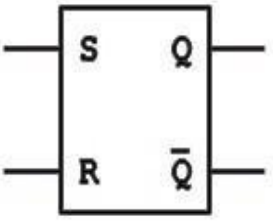
12.5 PROCEDURE:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

12.6 CIRCUIT DIAGRAM:

1) S-R LATCH:



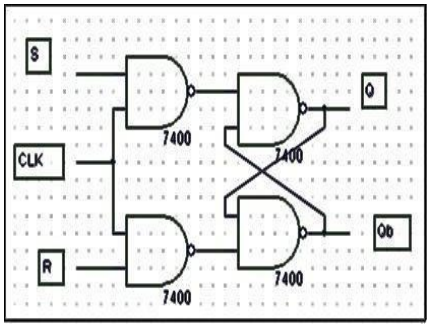


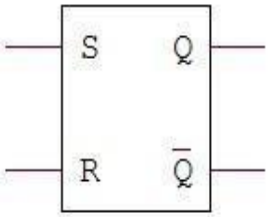
(A) LOGIC DIAGRAM **(B) SYMBOL**

TRUTH TABLE

S	R	Q+	*Q*b+
0	0	Q	*Q*b
0	1	0	1
1	0	1	0
1	1	0*	0*

2) SR-FLIP FLOP:





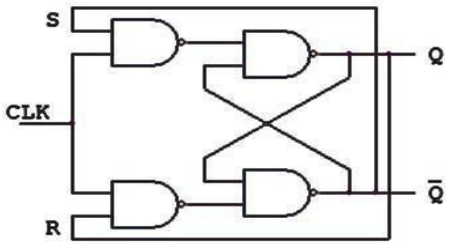
(A) LOGIC DIAGRAM **(B) SYMBOL**

TRUTH TABLE

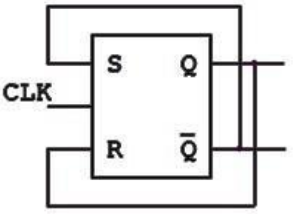
S	**R**	**Q+**	***Q*b+**
0	0	Q	*Q*b
0	1	0	1
1	0	1	0
1	1	0*	0*

3) CONVERSION OF SR-FLIP FLOP TO T-FLIP FLOP

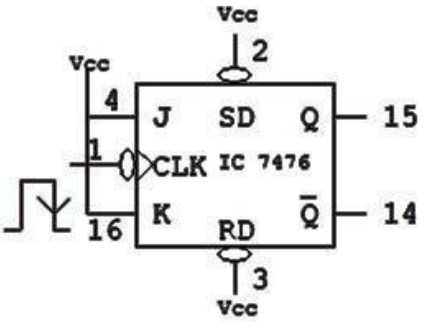
(Toggle) LOGIC DIAGRAM



SYMBOL



T FLIP FLOP USING IC 7476

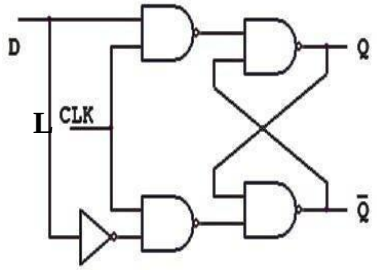


TRUTH TABLE

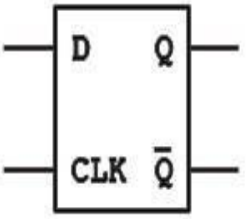
T	Qn + 1
0	Qn
1	$\overline{Qn}$

4) CONVERSION OF SR-FLIP FLOP TO D-FLIP FLOP

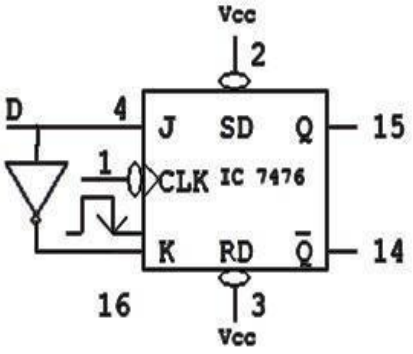
: LOGIC DIAGRAM



SYMBO



D FLIP FLOP USING IC 7476

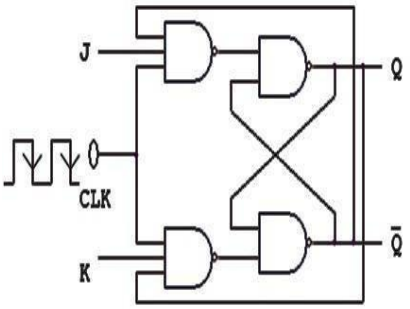


TRUTH TABLE

CLOCK	D	Q+	Q+
0	X	Q	Q
1	0	0	1
1	1	1	0

5) CONVERSION OF SR-FLIP FLOP TO JK-FLIP FLOP

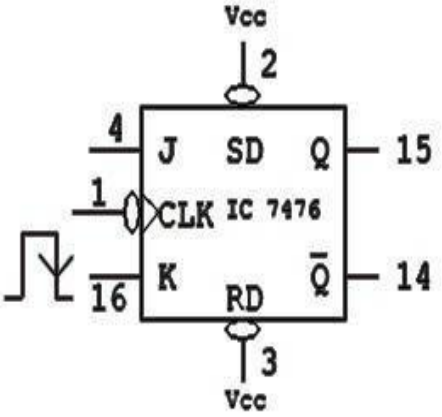
LOGIC DIAGRAM



TRUTH TABLE

Clock	J	K	Q+	Q'+	Comment
1	0	0	Q	Q"	No Change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Q"	Q	Toggle

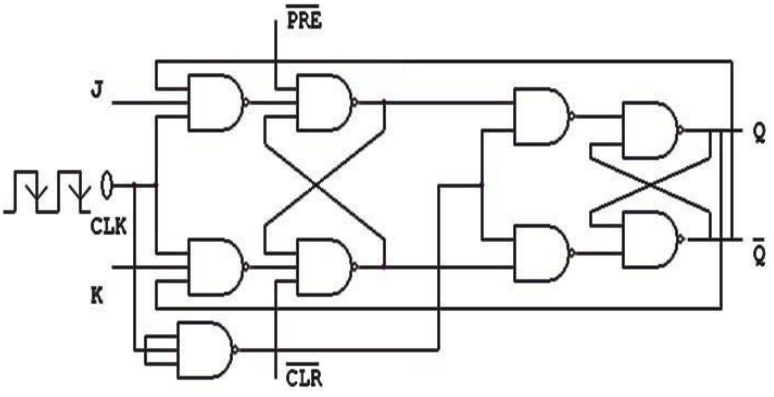
LOGIC DIAGRAM



TRUTH TABLE

	RD	Clock	J	K	Q	Q'	Comment
0	0	Not Allowed					
0	1	X	X	X	1	0	Set
1	0	X	X	X	0	1	Reset
1	1	1	0	0	NC	NC	Memory
1	1	1	0	1	0	1	Reset
1	1	1	1	0	1	0	Set
1	1	1	1	1	Q"	Q	Toggle

6) JK MASTER SLAVE FLIP FLOP



LOGIC DIAGRAM

TRUTH TABLE

$\overline{PRE}$ = $\overline{CLR}$ = 1

Clock	**J**	**K**	**Q+**	**Q'+**	**Comment**
1	0	0	Q	Q¨	No Change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Race Around		

12.7 Result:

12.8 LAB QUESTIONS:

1. What is the difference between Flip-Flop & latch?
2. Give examples for synchronous & asynchronous inputs?
3. What are the applications of different Flip-Flops?
4. What is the advantage of Edge triggering over level triggering?
5. What is the relation between propagation delay & clock frequency of flip-flop?
6. What is race around in flip-flop & how to overcome it?
7. Convert the J K Flip-Flop into D flip-flop and T flip-flop?
8. List the functions of asynchronous inputs?

EXPERIMENT No. 13

SHIFT REGISTERS

13.1 AIM: To realize and study of Shift Register.

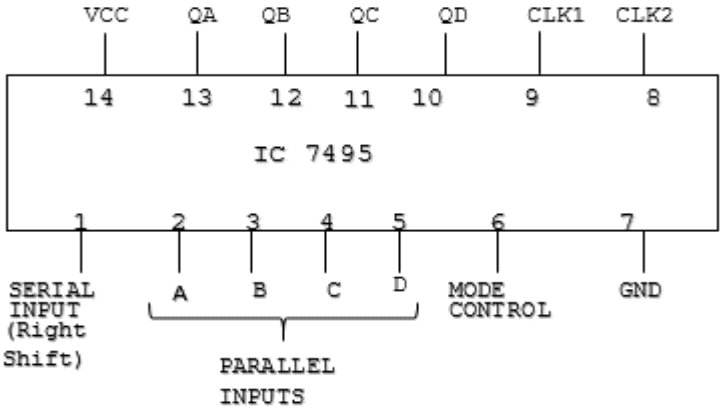
1. SISO (Serial in Serial out)
2. SIPO (Serial in Parallel out)
3. PIPO (Parallel in Parallel out)
4. PISO (Parallel in Serial out)

13.2 COMPONENTS REQUIRED: IC 7495, Patch Cords & IC Trainer Kit.

13.3 PROCEDURE:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

13.4 PIN DIAGRAM:



1) SERIAL IN SERIAL OUT (SISO) (Right Shift)

Serial i/p data	Shift Pulses	Q_A	Q_B	Q_C	Q_D
-	-	X	X	X	X
0	t1	0	X	X	X
1	t2	1	0	X	X
0	t3	0	1	0	X
1	t4	1	0	1	0
X	t5	X	1	0	1
X	t6	X	X	1	0
X	t7	X	X	X	1
X	t8	X	X	X	X

2) SERIAL IN PARALLEL OUT (SIPO)

Serial i/p data	Shift Pulses	Q_A	Q_B	Q_C	Q_D
-	-	X	X	X	X
0	t1	0	X	X	X
1	t2	1	0	X	X
0	t3	0	1	0	X
1	t4	**1**	**0**	**1**	**0**

3) PARALLEL IN PARALLEL OUT (PIPO)

Clock Input Terminal	Shift Pulses	Q_A	Q_B	Q_C	Q_D
-	-	X	X	X	X
CLK_2	t1	1	0	1	0

4) PARALLEL IN SERIAL OUT (PISO)

Clock Input Terminal	Shift Pulses	Q_A	Q_B	Q_C	Q_D
-	-	X	X	X	X
CLK_2	t1	1	0	1	0
CLK_2	t2	X	1	0	1
0	t3	X	X	1	0
1	t4	X	X	X	1
X	t5	X	X	X	X

13.5 RESULT:

EXPERIMENT No. 14

MULTIPLEXER

14.1 AIM:

To design and set up the following circuit

4:1 Multiplexer (MUX) using only NAND gates.

14.2 LEARNING OBJECTIVE:

To learn about various applications of multiplexer

To learn and understand the working of IC 74153 and IC 74139

To learn to realize any function using Multiplexer

14.3 THEORY:

Multiplexers are very useful components in digital systems. They transfer a large number of information units over a smaller number of channels, (usually one channel) under the control of selection signals. Multiplexer means many to one. A multiplexer is a circuit with many inputs but only one output. By using control signals (select lines) we can select any input to the output. Multiplexer is also called as data selector because the output bit depends on the input data bit that is selected. The general multiplexer circuit has 2^n input signals, n control/select signals and 1 output signal.

De-multiplexers perform the opposite function of multiplexers. They transfer a small number of information units (usually one unit) over a larger number of channels under the control of selection signals. The general de-multiplexer circuit has 1 input signal, n control/select signals and 2^n output signals. De-multiplexer circuit can also be realized using a decoder circuit with enable.

14.4 COMPONENTS REQUIRED:

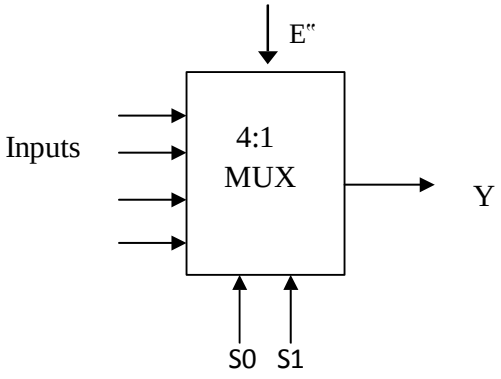
IC 7400, IC 7410, IC 7420, IC 7404, IC 74153, IC 74139, Patch Cords & IC Trainer Kit.

14.5 PROCEDURE:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

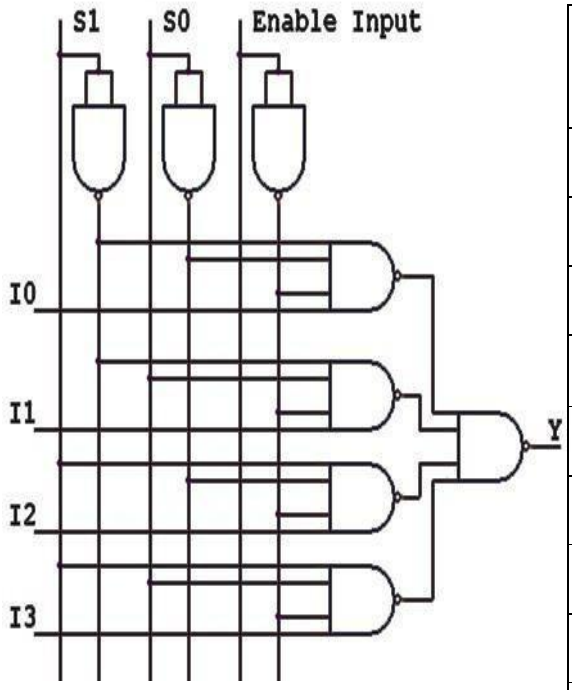
5.6 CIRCUIT DIAGRAM:

4:1 MULTIPLEXER



Output Y= E‟S1‟S0‟I0 + E‟S1‟S0I1 + E‟S1S0‟I2 + E‟S1S0I3

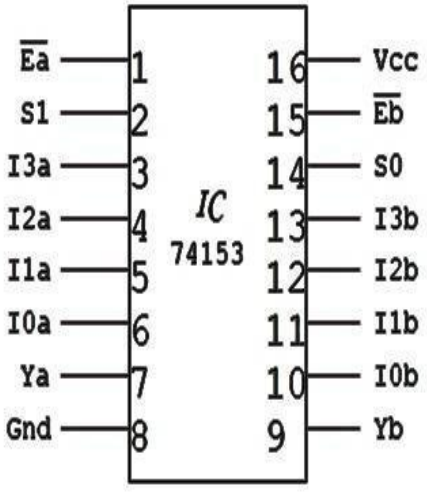
Realization Using NAND Gates



TRUTH TABLE

Select Inputs		Enable Input	Inputs				Out puts
S_1	**S_0**	**E**	**I_0**	**I_1**	**I_2**	**I_3**	**Y**
X	X	1	X	X	X	X	0
0	0	0	0	X	X	X	0
0	0	0	1	X	X	X	1
0	1	0	X	0	X	X	0
0	1	0	X	1	X	X	1
1	0	0	X	X	0	X	0
1	0	0	X	X	1	X	1
1	1	0	X	X	X	0	0
1	1	0	X	X	X	1	1

VERIFY IC 74153 MUX (DUAL 4:1 MULTIPLEXER)



14.7 RESULT:

14.8 VIVA QUESTIONS:

1) What is a multiplexer?
2) What is a de-multiplexer?
3) What are the applications of multiplexer and de-multiplexer?
4) Derive the Boolean expression for multiplexer and de-multiplexer. 5) How do you realize a given function using multiplexer 6) What is the difference between multiplexer & demultiplexer?

EXPERIMENT No. 15

COMPARATORS

15.1 AIM: To realize One & Two Bit Comparator and study of 7485 magnitude comparator.

15.2 LEARNING OBJECTIVE:

To learn about various applications of comparator
To learn and understand the working of IC 7485 magnitude comparator
To learn to realize 8-bit comparator using 4-bit comparator

15.3 THEORY:

Magnitude Comparator is a logical circuit, which compares two signals A and B and generates three logical outputs, whether A > B, A = B, or A < B. IC 7485 is a high speed 4-bit Magnitude comparator, which compares two 4-bit words. The A = B Input must be held high for proper compare operation.

15.4 COMPONENTS REQUIRED:

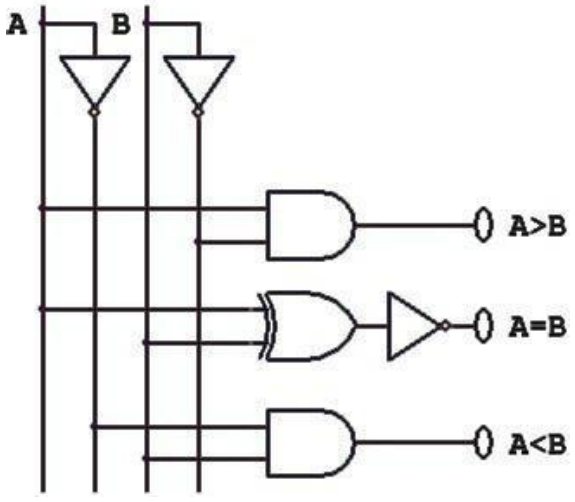
IC 7400, IC 7410, IC 7420, IC 7432, IC 7486, IC 7402, IC 7408, IC 7404, IC 7485, Patch Cords & IC Trainer Kit.

15.5 PROCEDURE:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

15.6 CIRCUIT DIAGRAM:

1-BIT COMPARATOR



Boolean Expression;

$A>B = A\bar{B}$

$A<B = \bar{A}B$

$A=B = \bar{A}\,\bar{B} + AB$

TRUTH TABLE

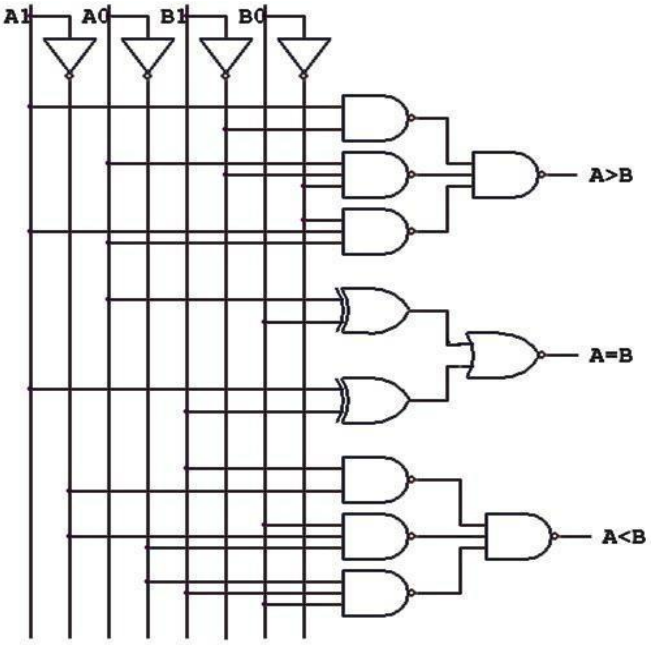
INPUTS		OUTPUTS		
A	B	A > B	A = B	A < B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

2- BIT COMPARATOR

Boolean Expression:

(A> B) = A1 $\bar{B}$1+$A0\bar{B}1\bar{B}0$ +$\bar{B}0A1A0$
(A=B) = (A0 ⊕ B0) (A1⊕ B1)

(A<B) = $\bar{B}$1A1+$\bar{B}0\bar{A}1\bar{A}0$+A0B1B0

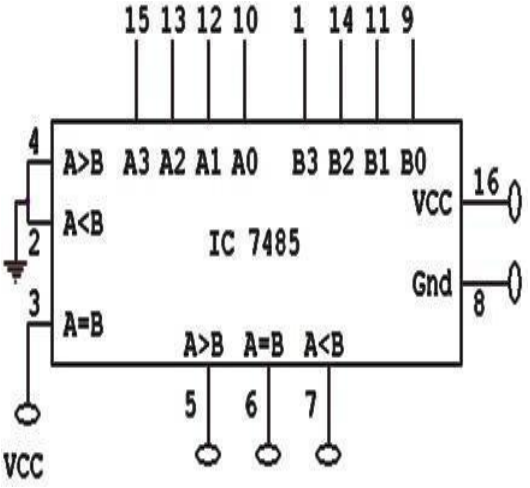


2-bit comparator circuit diagram

TRUTH TABLE

INPUTS				OUTPUTS		
A_1	A_0	B_1	B_0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

TO COMPARE THE GIVEN DATA USING 7485 CHIP.



A				B				Result
A3	**A2**	**A1**	**A0**	**B3**	**B2**	**B1**	**B0**	
0	0	0	1	0	0	0	0	**A > B**
0	0	0	1	0	0	0	1	**A = B**
0	0	0	0	0	0	0	1	**A < B**

15.7 RESULT:

15.8 LAB QUESTIONS:

1. What is a comparator?
2. What are the applications of comparator?
3. Derive the Boolean expressions of one-bit comparator and two bit comparators.
4. How do you realize a higher magnitude comparator using lower bit comparator?
5. Design a 2 bit comparator using a single Logic gates?
6. Design an 8 bit comparator using a two numbers of IC 7485?