INTEGRATED CIRCUITS APPLICATIONS LABORATORY

LAB MANUAL

Course Code : AEC106
Regulations : IARE – R16
Class : V Semester
Branch : ECE

Prepared by

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Electronics & Communication Engineering

Program Outcomes	
PO1	**Engineering Knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems
PO2	**Problem Analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences
PO3	**Design/Development of Solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations
PO4	**Conduct Investigations of Complex Problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions
PO5	**Modern Tool Usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations
PO6	**The Engineer And Society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice
PO7	**Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development
PO8	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice
PO9	**Individual and Team Work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings
PO10	**Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions
PO11	**Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.
PO12	**Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments

Program Specific Outcomes	
PSO1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.
PSO2	**Problem-solving skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.
PSO3	**Modern Tools in Electrical Engineering:** Comprehend the technologies like PLC, PMC, process controllers, transducers and HMI and design, install, test, maintain power systems and industrial applications

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Electronics & Communication Engineering

ATTAINMENT OF PROGRAM OUTCOMES & PROGRAM SPECIFIC OUTCOMES

S. No.	Experiment	Program Outcomes Attained	Program Specific Outcomes Attained
1	INVERTING, NON-INVERTING AND DIFFERENTIAL AMPLIFIERS	PO1, PO 12	PSO1, PSO2
2	INTEGRATOR AND DIFFERENTIATOR USING IC741 OP-AMP	PO1, PO2,PO 12	PSO1, PSO2
3	ACTIVE LOW PASS & HIGH PASS BUTTERWORTH FILTERS (2^{nd} ORDER)	PO1,PO2,PO 12	PSO1, PSO2
4	ASTABLE MULTIVIBRTATOR USING IC555 TIMER	PO1, PO5,PO 12	PSO1, PSO2
5	MONOSTABLE MULTIVIBRATOR USING IC555 TIMER	PO1, PO5,PO 12	PSO1, PSO2
6	SCHMITT TRIGGER CIRCUITS USING IC555 &IC 741	PO1, PO5,PO 12	PSO1, PSO2
7	IC 565 PLL APPLICATIONS	PO1, PO2, PO11	PSO1, PSO2
8	INSTRUMENTATION AMPLIFIER USING IC 741	PO1, PO2, PO11	PSO1, PSO2
9	MULTIPLEXER AND DEMULTIPLEXER	PO1, PO5,PO 12	PSO1, PSO2
10	ENCODERS AND DEODERS	PO1, PO2, PO11	PSO1, PSO2
11	REALISATION OF DIFFERENT FLIP-FLOPS USING LOGIC GATES	PO1, PO2, PO11	PSO1, PSO2
12	4-BIT COUNTERS	PO1, PO2, PO11	PSO1, PSO2
13	REALISATION OF SHIFT REGISTERS	PO1, PO2, PO11	PSO1, PSO2
14	DECADE COUNTER	PO1, PO2, PO11	PSO1, PSO2

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Certificate

This is to Certify that it is a bonafied record of Practical work done by Sri/Kum. _____ bearing the Roll No. _____ of _____ Class _____ Branch in the _____ laboratory during the Academic year _____ under our supervision.

Head of the Department **Lecture In-Charge**

External Examiner **Internal Examiner**

Course Overview:

This course provides practical handson exposure to be acquainted to principles and characteristics of op-amp and apply the techniques for the design of comparators, instrumentation amplifier, integrator, differentiator, multivibrators, waveform generators, log and anti-log amplifiers. Analyze and design filters, timer, analog to digital and digital to analog Converters. Understand the functionality and characteristics of commercially available digital integrated circuits

Course Objectives (COs):

I. Implement different circuits and verify circuit concepts.
II. Study the concepts of multivibrators and filters.
III. Verify the operations of the 555 timers and PLLs and their applications.
IV. Design and verify combinational and sequential circuits

Course Learning Outcomes (CLOs):

1. Illustrate the block diagram, classifications, package types, temperature range specifications and characteristics of Op-Amp.
2. Discuss various types of configurations in differential amplifier with balanced and unbalanced outputs.
3. Evaluate DC and AC analysis of dual input balanced output configuration and discuss the properties of differential amplifier and discuss the operation of cascaded differential amplifier.
4. Analyze and design linear applications like inverting amplifier, non-inverting amplifier, instrumentation amplifier and etc. using Op-Amp.
5. Analyze and design non linear applications like multiplier, comparator, log and anti log amplifiers, waveform generators and etc, using Op-Amp.
6. Discuss various active filter configurations based on frequency response and construct using 741 OpAmp.

7. Design bistable, monostable and astable multivibrators operation by using IC 555 timer and study their applications.
8. Determine the lock range and capture range of PLL and use in various applications of communications.
9. Understand the classifications, characteristics and need of data converters such as ADC and DAC.
10. Analyze the digital to analog converter technique such as weighted resistor DAC, R-2R ladder DAC, inverted R-2R ladder DAC and IC 1408 DAC.
11. Analyze the analog to digital converter technique such as integrating, successive approximation and flash converters.
12. Design adders, multiplexers, demultiplexers, decoders, encoders by using TTL/CMOS integrated circuits and study the TTL and CMOS logic families.
13. Design input/output interfacing with transistor – transistor logic or complementary metal oxide semiconductor integrated circuits.
14. Understand the operation of SR, JK, T and D flip-flops with their truth tables and characteristic equations. Design TTL/CMOS sequential circuits
15. Design synchronous, asynchronous and decade counter circuits and also design registers like shift registers and universal shift registers.
16. Apply the concept of Integrated circuits to understand and analyze the real time applications.
17. Acquire the knowledge and develop capability to succeed national and international level competitive examinations.

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Electrical & Electronics Engineering

INSTRUCTIONS TO THE STUDENTS

1. Students are required to attend all labs.
2. Students should work individually in the hardware and software laboratories.
3. Students have to bring the lab manual cum observation book, record etc along with them whenever they come for lab work.
4. Should take only the lab manual, calculator (if needed) and a pen or pencil to the work area.
5. Should learn the prelab questions. Read through the lab experiment to familiarize themselves with the components and assembly sequence.
6. Should utilize 3 hour's time properly to perform the experiment and to record the readings. Do the calculations, draw the graphs and take signature from the instructor.
7. If the experiment is not completed in the stipulated time, the pending work has to be carried out in the leisure hours or extended hours.
8. Should submit the completed record book according to the deadlines set up by the instructor.
9. For practical subjects there shall be a continuous evaluation during the semester for 25 sessional marks and 50 end examination marks.
10. Out of 25 internal marks, 15 marks shall be awarded for day-to-day work and 10 marks to be awarded by conducting an internal laboratory test.

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INTEGRATED CIRCUITS APPLICATIONS LABORATORY

SYLLABUS

Recommended Systems/Software Requirements:

To Design any Integrated Circuit, We need Analog and Digital Integrated Circuit Trainer kit with Dual DC Regulated Supply (0-30v) and Function Generator.

To observe we need to use Cathode Ray Oscilloscope.

We need to use different types of IC's like IC555, IC741, IC565, IC7402, IC7408, etc.

S. No	List of Experiments	Page No.	Date	Remarks
1.	INVERTING, NON-INVERTING AND DIFFERENTIAL AMPLIFIERS			
2.	INTEGRATOR AND DIFFERENTIATOR USING IC741 OP-AMP			
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4.	ASTABLE MULTIVIBRTATOR USING IC555 TIMER			
5.	MONOSTABLE MULTIVIBRATOR USING IC555 TIMER			
6.	SCHMITT TRIGGER CIRCUITS USING IC555 & IC 741			
7.	IC 565 PLL APPLICATIONS			
8.	INSTRUMENTATION AMPLIFIER USING IC 741			
9.	MULTIPLEXER AND DEMULTIPLEXER			
10.	ENCODERS AND DEODERS			
11.	REALISATION OF DIFFERENT FLIP-FLOPS USING LOGIC GATES			
12.	4-BIT COUNTERS			
13.	REALISATION OF SHIFT REGISTERS			
14.	DECADE COUNTER			

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Electrical & Electronics Engineering

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13	REALISATION OF SHIFT REGISTERS	PO1, PO2, PO11	PSO1, PSO2
14	DECADE COUNTER	PO1, PO2, PO11	PSO1, PSO2

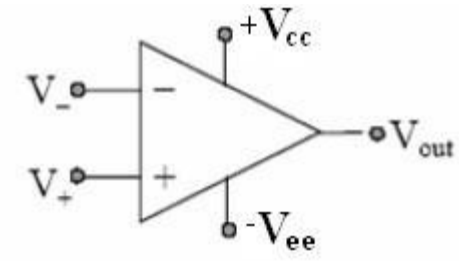
INTRODUCTION OF IC 741 & IC 555

Linear Integrated circuits are being used in a number of electronic applications such as in fields like audio and radio communication, medical electronics, instrumentation control, etc. An important Linear IC is operational amplifier.

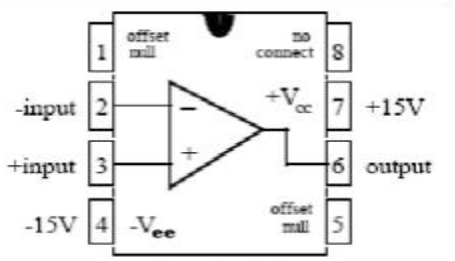
IC741: (Operational Amplifier)

The circuit schematic of an op-amp is a triangle. It has two input terminals and one output terminal. The terminal with a (-) sign is called inverting input terminal and the terminal with (+) sign is called the non-inverting input terminal.

Symbol:



Pin Configuration



Pinout for the 741 op amp.

Specifications:

Supply Voltage	18V
Internal Power Dissipation	310mw
Differential input voltage	30V
Input Voltage	15V
Operating temperature range	0ºC to 70ºC

Applications:

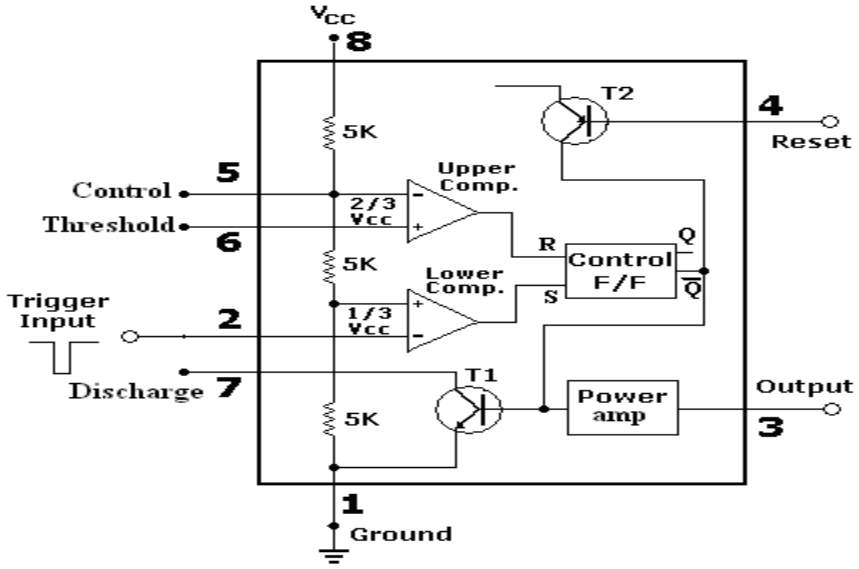
- Non-inverting amplifier
- Inverting amplifier
- Integrator
- Differentiator
- Low Pass, High Pass, Band pass and Band Reject Filters

Features:

- No External frequency compensation is required Short circuit Protection
- Off Set Null Capability
- Large Common mode and differential Voltage ranges Low Power Dissipation
- No-Latch up Problem
- 741 is available in three packages: 8-pin metal can, 10-pin flat pack and 8 or 14-pin DIP

IC 555: (Timer) Pin Configuration

Functional block diagram:



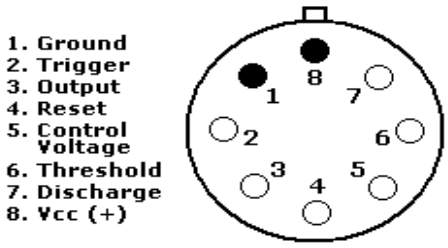


fig. 1. 8-pin T package

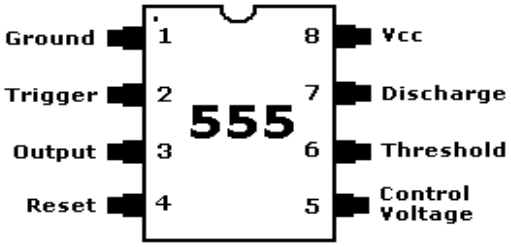


fig. 2. 8-pin V package

Specifications:

Supply Voltage	5V to 18V
Maximum Current rating	200mA
Minimum Triggering Voltage	- (1/3) VCC
Operating temperature range	0ºC to 70ºC

Applications:

- Astable Multivibrator, Schmitt trigger, Free running ramp Generator, etc.,
- Mono stable Multivibrator, Frequency divider, Pulse structure

Features:

555 timers are reliable, easy to use and low cost. The device is available as an 8 pin circular style, an 8–pin mini DIP or a 14 Pin DIP

Pre Lab Questions:

1. What is an Integrated circuit?
2. List the manufactures of IC?
3. Define linear IC and Digital IC?
4. Mention the advantages of IC Technology?
5. What is the use of negative feedback for an amplifier?
6. What is an differential amplifier?
7. What is common mode differential amplifier?
8. What is difference mode differential amplifier?
9. What is monolithic technology?

EXPERIMENT NO: 1

INVERTING, NON-INVERTING AND DIFFERENTIAL AMPLIFIERS

1.1 AIM:

To study the operation of the inverting, non-inverting and differential amplifiers using op-amp and trace the output.

1.2 COMPONENTS & EQUIPMENT REQUIRED: -

S.No	Device	Range / Rating	Quantity (in No's)
1	Bread Board	-	1
2	IC741	-	1
3	Regulated power supply	0-30v	1
4	Resistors	1-100kΩ	4
5	Digital Multimeter	-	1
6	Probes, Connecting Wires	-	required

1.3 THEORY:

Inverting and Non-Inverting Amplifier:

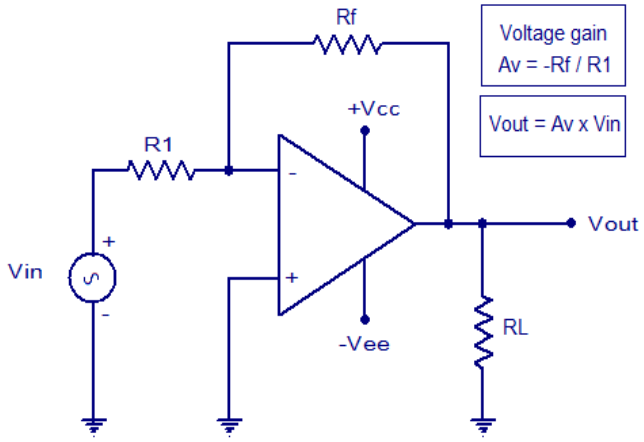
In this configuration, the input voltage signal, (V_{IN}) is applied directly to the non-inverting (+) input terminal which means that the output gain of the amplifier becomes "Positive" in value in contrast to the "Inverting Amplifier"circuit whose output gain is negative.

Differential Amplifier:

A Differential Amplifier is a circuit that gives the difference of the two inputs, Vo =V2-V1, Where V1 and V2 are the inputs. By connecting one input voltage V1 to inverting terminal and another input voltage V2 to the non – inverting terminal, we get the resulting circuit as the Differential Amplifier. This is also called as Subtractor using op-amps. Output of a differential amplifier (subtractor) is given as Vo = (-Rf/R1) (V1-V2)

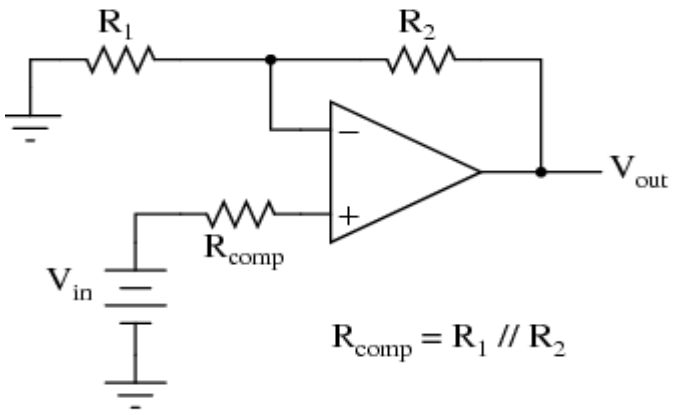
If all external resistors are equal in value, then the gain of the amplifier is equal to -1. The output voltage of the differential amplifier with a gain of -1 is Vo = (V2-V1)

Thus the output voltage Vo is equal to the voltage V2 applied to the non – inverting terminal minus the voltage V1 applied to the inverting terminal. Hence the circuit also called a Subtractor.



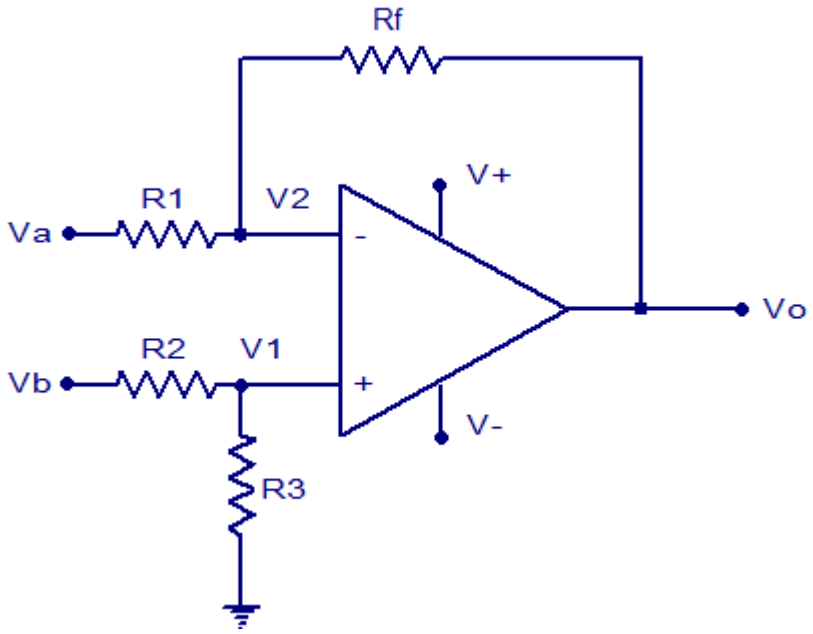
Inverting Amplifier using IC 741Op-Amp

Vcc=12V, Vee= -12V, R1=Rf=10kOhms



Differential Amplifier Using OP_AMP

R1=R2=10KOhms



R1=R2=R3=Rf=10KOhms

1.5 PROCEDURE:

Inverting and Non inverting Amplifier:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Apply dc voltages at each input terminal for V1 and V2 from the dc supply and check the output voltage Vo at the output terminal.
4. Tabulate 3 different sets of readings by repeating the above step.
5. Compare practical Vo with the theoretical output voltage Vo =V1+V2.

Differential Amplifier:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Apply dc voltages at each input terminal for V1 and V2 from the dc supply and check the output voltage Vo at the output terminal.
4. Tabulate 3 different sets of readings by repeating the above step.
5. Compare practical Vo with the theoretical output voltage Vo =V2-V1.

1.6 TABLE:

Inverting Amplifier:

S.No.	V1 Volts	Theoretical Vo	Practical Vo Volts

Non Inverting Amplifier:

S.No.	V1 Volts	Theoretical Vo	Practical Vo Volts

Differential Amplifier:

S.No.	V1 Volts	V2 Volts	Theoretical Vo=V2-V1	Practical Vo Volts

1.8 RESULT:

1.9 PRE LAB QUESTIONS

1. What are Op amp applications?
2. What is need of feedback?
3. What is closed loop operation operation of op amp?
4. What is open loop operation of op amp?
5. What is virtual ground?
6. Define a) passive integrator b) active integrator?
7. Define a) passive differentiator b) active differentiator?
8. What is the difference b/w ideal active integrator and ideal active differentiator?
9. What is -3db frequency?
10. Mention the disadvantages of ideal integrator?
11. Mention the disadvantages of ideal differentiator?

1.10 POST LAB QUESTIONS:

1. What is the other name for adder?
2. Draw the circuit diagram of 3 input adder.
3. Draw the circuit diagram of a Differential Amplifier.
4. Which amplifier acts as a Subtractor?
5. How many basic input parameters are required for a comparator?
6. Draw the circuit diagram of a non-inverting comparator and inverting comparator.
7. What is the output of a non-inverting comparator and inverting comparator if the input is sinusoidal?
8. What are the differences between the Inverting and Non–Inverting comparator?
9. What is the name of the comparator if the reference voltage is 0V?
10. Draw the circuit diagram and the output waveform of a Zero Crossing Detector if the input is sinusoidal?
11. What is the name of a regenerative comparator?
12. Draw an op- amp circuit whose output Vo is V1+ V2 – V3 –V.

EXPERIMENT NO: 2

INTEGRATOR AND DIFFERENTIATOR USING IC741 OP-AMP

2.1 AIM: To study the operation of the Integrator & differentiator using op-amp and trace the output wave forms for sine and square wave inputs.

2.2 COMPONENTS & EQUIPMENT REQUIRED: -

S.No	Device	Range / Rating	Quantity (in No's)
1	Bread Board	-	1
2	IC741	-	1
3	Capacitors	µF	3
4	Function Generator	0-1MHZ	1
5	Resistors	1-100KΩ	4
6	CRO	0-20MHz	1
7	Probes, Connecting Wires	-	required

2.3 THEORY:

2.3.1 Integrator

A circuit in which the output voltage is the integration of the input voltage is called an integrator**.**

In the practical integrator to reduce the error voltage at the output, a resistor RF is connected across the feedback capacitor CF. Thus, RF limits the low-frequency gain and hence minimizes the variations in the output voltage.

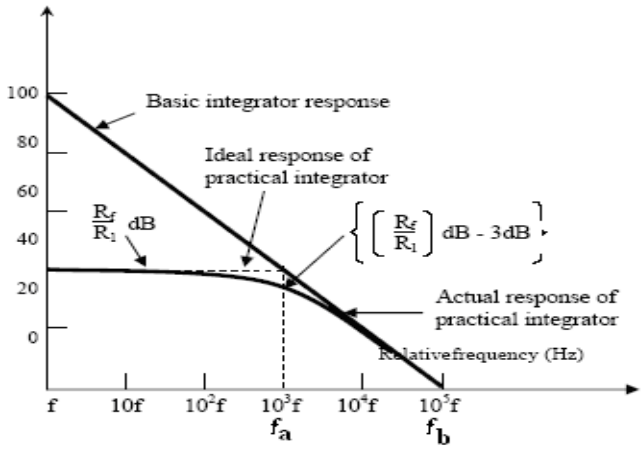


Fig 2.1 Frequency Response of Integrator

$$V_o = -\frac{1}{R_1 C_f} \int V_{in}\, dt \qquad \text{——} \quad (1)$$

Frequency response of the integrator is shown in the fig. 2.1. fb is the frequency at which the gain is 0 dB and is given by

$$f_b = 1/2R1Cf.$$

In this fig. there is some relative operating frequency, and for frequencies from f to fa the gain RF/R1 is constant. However, after fa the gain decreases at a rate of 20 dB/decade. In other words, between fa and fb the circuit of fig. 2.1 acts as an integrator. The gain- limiting frequency fa is given by

$$f_a = 1/2RfCf$$

Normally fa<fb. From the above equation, we can calculate Rf by assuming fa & Cf. This is very important frequency. It tells us where the useful integration range starts.

If fin < fa - circuit acts like a simple inverting amplifier and no integration results, If fin = fa - integration takes place with only 50% accuracy results,
If fin = 10fa - integration takes place with 99% accuracy results.

In the circuit diagram of Integrator, the values are calculated by assuming fa as 50 Hz. Hence the input frequency is to be taken as 500Hz to get 99% accuracy results.

Integrator has wide applications in

- Analog computers used for solving differential equations in simulation arrangements.
- A/D Converters
- Signal wave shaping
- Function Generators.

2.3.2 Differentiator:

As the name suggests, the circuit performs the mathematical operation of differentiation, i.e. the output voltage is the derivative of the input voltage.

$$\mathbf{V_o = - R_f C_1 \frac{dV_{in}}{dt}}$$

Both the stability and the high-frequency noise problems can be corrected by the addition of two components: R1 and Cf, as shown in the circuit diagram. This circuit is a practical differentiator. The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to RfC1. That is, T>= RfC1

Differentiator can be designed by implementing the following steps.

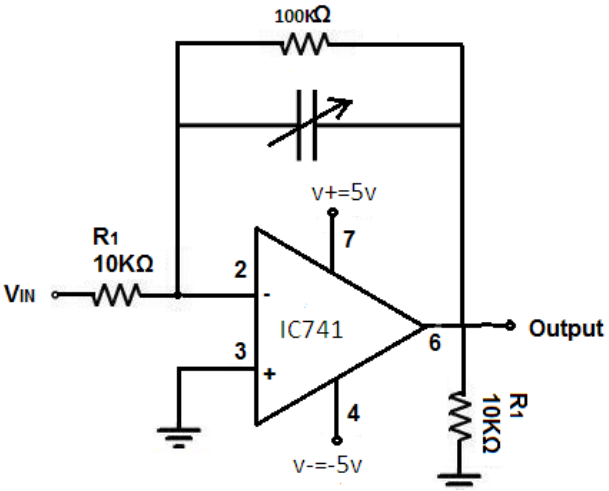
1. Select fa equal to the highest frequency of the input signal to be differentiated. Then, assuming a value of C1<1 F, calculate the value of Rf
2. Calculate the values of R1and Cf so that R1C1=RfCf
3. Select fa equal to the highest frequency of the input signal to be differentiated. Then, assuming a value of C1<1 F, calculate the value of Rf
4. Calculate the values of R1and Cf so that R1C1=RfCf

Differentiator has wide applications in

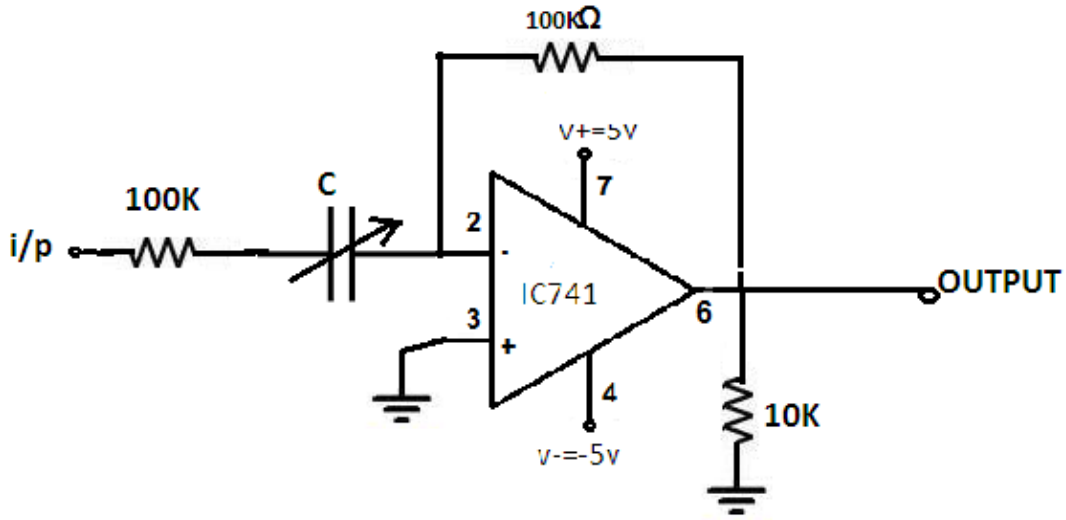
1. Monostable Multi vibrator
2. Signal wave shaping
3. Function Generators.

2.4 CIRCUIT DIAGRAM:

Integrator:



Differentiator:



2.5 PROCEDURE:

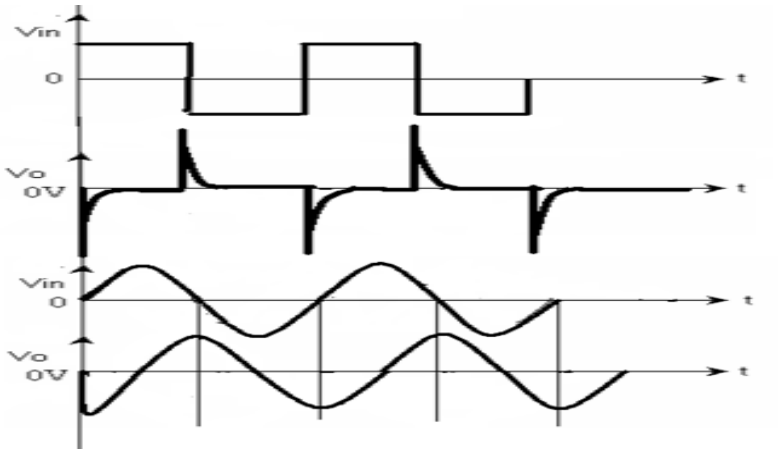
Integrator:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Apply sine wave at the input terminals of the circuit using function Generator.
4. Connect channel-1 of CRO at the input terminals and channel-2 at the output terminals.
5. Observe the output of the circuit on the CRO which is a cosine wave (90o phase shifted from the sine wave input) and note down the position, the amplitude and the time period of Vin & Vo.
6. Now apply the square wave as input signal.
7. Observe the output of the circuit on the CRO which is a triangular wave and note down the position, the amplitude and the time period of Vin &Vo.
8. Plot the output voltages corresponding to sine and square wave inputs.

Differentiator:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Apply sine wave at the input terminals of the circuit using function Generator.
4. Connect channel-1 of CRO at the input terminals and channel-2 at the output terminals.
5. Observe the output of the circuit on the CRO which is a cosine wave (90o phase shifted from the sine wave input) and note down the position, the amplitude and the time period of VIN & V_O
6. Now apply the square wave as input signal.
7. Observe the output of the circuit on the CRO which is a spike wave and note down the position, the amplitude and the time period of VIN & V_O
8. Plot the output voltages corresponding to sine and square wave inputs.

2.6 EXPECTED WAVEFORMS



2.7 RESULT:

2.8 PRE LAB QUESTIONS:

1. Define filter?
2. What is Active filter and Passive filter?
3. What is Frequency scaling
4. Mention the design steps of active low pass filter?
5 . Mention the design steps of active high pass filter?
6. What are the advantages of butter worth filter?
7. List the different types of filters?
8. What is the twin T network?

2.9 POST LAB QUESTIONS:

1. What is an Integrator?
2. Draw the circuit of the Integrator using op-amp IC741.
3. Write down the expression for Vo of an Integrator.
4. Draw the frequency response of the Integrator and explain.
5. Draw the output waveform of the Integrator when the input is a Square wave.
6. What is the purpose behind the connection of Rf in the feedback path of Integrator?
7. What are the applications of Integrator?
8. Why Rcomp is used in both Integrator and Differentiator circuits?
9. What is a Differentiator?
10. Draw the circuit of the Differentiator using op-amp IC741.
11. Write down the expression for Vo of a Differentiator.
12. Draw the output waveform of the Differentiator when the input is a Sine wave.
13. Why R1 and Cf are connected in the circuit of the Differentiator?

EXPERIMENT NO: 3

ACTIVE LOW PASS & HIGH PASS BUTTERWORTH FILTERS (2nd ORDER)

3.1 AIM: To plot the frequency response of Butterworth LPF and HPF and to find the cut-off frequencies.

3.2 COMPONENTS & EQUIPMENT REQUIRED: -

S.No	Device	Range / Rating	Quantity (in No's)
1	Bread Board	-	1
2	IC741	-	1
3	Capacitors	µF	1
4	Function Generator	0-1MHz	1
5	Resistors	1-100kΩ	1
6	CRO	0-20MHz	1
7	Probes, Connecting Wires	-	1

3.3 THEORY:

Filters are classified as follows:

Based on components used in the circuit

- Active filters – Use active elements like transistor or op-amp(provides gain) in addition to passive elements
- Passive filters – Use only passive elements like resistors, capacitors and inductors, hence no gain here.

Based on frequency range

- Low pass filter(LPF) – Allows low frequencies
- High pass filter(HPF) – Allows high frequencies
- Band pass filter(BPF) – Allows band of frequencies
- Band reject filter(BRF) – Rejects band of frequencies All pass filter – Allows all frequencies but with a phase shift

Active Filter is often a frequency – selective circuit that passes a specified band of frequencies and blocks or attenuates signals of frequencies outside this band.
These Active Filters are most extensively used in the field of communications and signal processing. They are employed in one form or another in almost all sophisticated electronic systems such as Radio, Television, Telephone, Radar, Space Satellites, and Bio- Medical Equipment

3.3.1 HPF:

The basic electrical operation of an **Active High Pass Filter** (HPF) is exactly the same as we saw for its equivalent RC passive high pass filter circuit, except this time the circuit has an operational amplifier or op-amp included within its filter design providing amplification and gain control.

A first-order (single-pole) **Active High Pass Filter** as its name implies, attenuates low frequencies and passes high frequency signals. It consists simply of a passive filter section followed by a non-inverting operational amplifier. The frequency response of the circuit is the same as that of the passive filter, except that the amplitude of the signal is increased by the gain of the amplifier and for a non-inverting amplifier the value of the pass band voltage gain is given as 1 + R2/R1, the same as for the low pass filter circuit.

Gain for an Active High Pass Filter

$$\text{Voltage Gain, (Av)} = \frac{\text{Vout}}{\text{Vin}} = \frac{A_F\left(\frac{f}{fc}\right)}{\sqrt{1+\left(\frac{f}{fc}\right)^2}}$$

Where:

- A_F = the Pass band Gain of the filter, (1 + R2/R1)
- f = the Frequency of the Input Signal in Hertz, (Hz)
- fc = the Cut-off Frequency in Hertz, (Hz)

Just like the low pass filter, the operation of a high pass active filter can be verified from the frequency gain equation above as:

1. At very low frequencies, $f < fc$ $\frac{\text{Vout}}{\text{Vin}} < A_F$
2. At the cut-off frequency, $f = fc$ $\frac{\text{Vout}}{\text{Vin}} = \frac{A_F}{\sqrt{2}} = 0.707\,A_F$
3. At very high frequencies, $f > fc$ $\frac{\text{Vout}}{\text{Vin}} \cong A_F$

Then, the **Active High Pass Filter** has a gain A_F that increases from 0Hz to the low frequency cut-off point, f_C at 20dB/decade as the frequency increases. At f_C the gain is $0.707A_F$, and after f_C all frequencies are pass band frequencies so the filter has a constant gain A_F with the highest frequency being determined by the closed loop bandwidth of the op-amp.

3.3.2 LPF:

First-order low pass active filter, consists simply of a passive RC filter stage providing a low frequency path to the input of a non-inverting operational amplifier. The amplifier is configured as a voltage-follower (Buffer) giving it a DC gain of one, Av = +1 or unity gain as opposed to the previous passive RC filter which has a DC gain of less than unity.

The advantage of this configuration is that the op-amps high input impedance prevents excessive loading on the filters output while its low output impedance prevents the filters cut-off frequency point from being affected by changes in the impedance of the load.

The frequency response of the circuit will be the same as that for the passive RC filter, except that the amplitude of the output is increased by the pass band gain, A_F of the amplifier. For a non-inverting amplifier circuit, the magnitude of the voltage gain for the filter is given as a function of the feedback resistor (R_2) divided by its corresponding input resistor (R_1) value and is given as:

$$\text{DC gain} = \left(1 + \frac{R_2}{R_1}\right)$$

Therefore, the gain of an active low pass filter as a function of frequency will be:

Gain of a first-order low pass filter

$$Voltage\ Gain, (Av) = \frac{Vout}{Vin} = \frac{A_F}{\sqrt{1 + \left(\frac{f}{fc}\right)^2}}$$

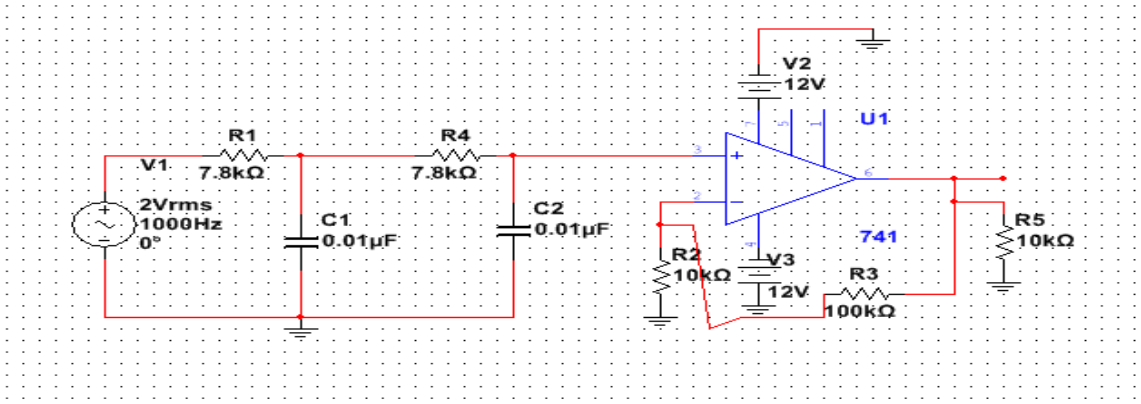
Where:

- A_F = the pass band gain of the filter, (1 + R2/R1)
- f = the frequency of the input signal in Hertz, (Hz)
- fc = the cut-off frequency in Hertz, (Hz)

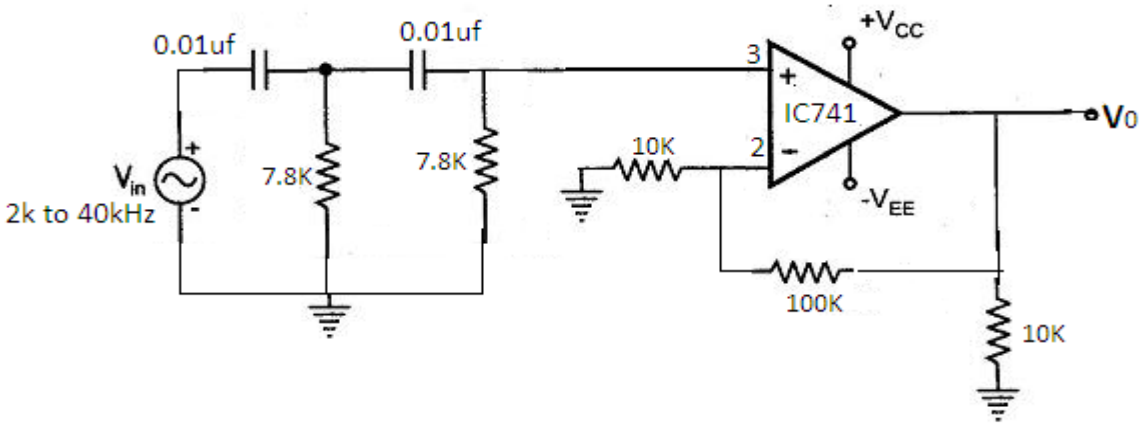
Thus, the operation of a low pass active filter can be verified from the frequency gain equation above as:

1. At very low frequencies, $f < f$c
2. At the cut-off frequency, $f = f$c
3. At very high frequencies, $f > f$c

3.4 CIRCUIT DIAGRAM FOR LPF:



CIRCUIT DIAGRAM FOR HPF:



3.5 PROCEDURE:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Connect channel -1 of CRO to input terminals (Vin) and channel -2 to output terminals (Vo).
4. Set Vin = 1V & fin=10Hz using function generator.
5. By varying the input frequency in regular intervals, note down the output voltage.
6. Calculate the gain (Vo/Vin) and Gain in dB = 20 log (Vo/Vin) at every frequency.
7. Plot the frequency response curve (taking frequency on X-axis & Gain in dB on Y- axis) using Semi log Graph.
8. Find out the high cut-off frequency, fH (at Gain= Constant Gain, Af – 3 dB) from the frequency response plotted.

9. Verify the practical (fH from graph) and the calculated theoretical cut-off frequency(fH=1/2ΠRC).

3.6 TABLE:

3.6.1 FREQUINCY RESPONSE OF HPF

Vin = 1V

S.No.	Input Frequency f(Hz)	Output Voltage Vo (V)	Gain Magnitude | Vo/Vin |	Gain in dB = 20log| Vo/Vin |

3.6.2 FREQUINCY RESPONSE OF LPF

Vin = 1V

S.No.	Input Frequency f(Hz)	Output Voltage Vo (V)	Gain Magnitude | Vo/Vin |	Gain in dB = 20log| Vo/Vin |

3.7 CALCULATIONS:

THEORETICAL Cut-off frequency:

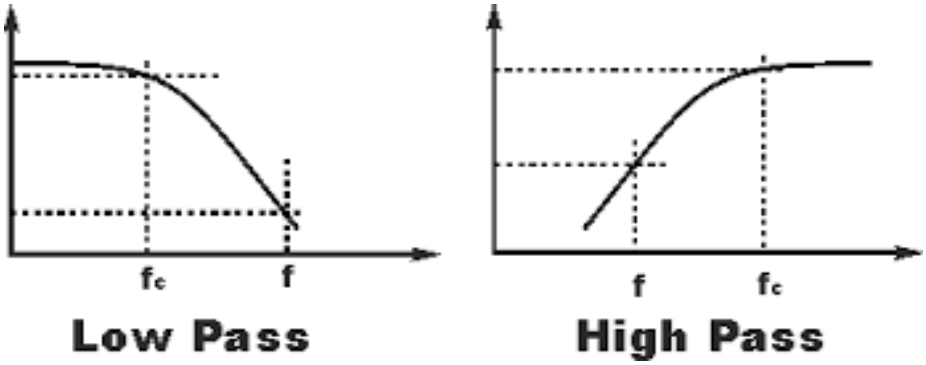
$f_H = 1 / (2\pi RC)$ = high cut-off frequency of the Low pass filter.

PRACTICAL Cut-off frequency (from Graph) :

f_H = high cut-off frequency of the Low pass filter

= 3dB cut-off frequency =

EXPECTED GRAPH:



3.8 RESULT:

3.9 PRE LAB QUESTIONS:

1. What is a Function generator?
2. What is the function of IC741 in function generator?
3. What are advantages of function generator?
4. What is the maximum frequency a function generator can work?
5. What is the function of IC555 in function generator?
6. What is the use of variable resistor in sine wave generator?

3.10 POST LAB QUESTIONS:

1. How filters are classified? Give one example for each classification.
2. What is an active filter and why it is called so?
3. How an active filter differs from a passive filter?
4. What are the advantages of active filters over passive filters?
5. Draw the circuit diagrams of active filters LPF and HPF.
6. Draw the frequency response of all filters (LPF, HPF, BPF, BRF and All-pass).
7. What is the gain roll off rate for a 1st order and 2nd order filter?
8. What is the formula for cut-off frequency?
9. What is a 3 dB frequency and why it is called so?
10. What are the other names for 3 dB frequency?

EXPERIMENT NO: 4

ASTABLE MULTIVIBRTATOR USING IC555 TIMER

4.1 AIM:

To design a Astable Multivibrator using IC555 and compare it is theoretical and practical pulse width and Duty Cycle

4.2 COMPONENTS & EQUIPMENT REQUIRED: -

S.No	Device	Range / Rating	Quantity (in No's)
1	Bread Board	-	1
2	IC555	-	1
3	Capacitors	µF	1
4	Function Generator	0-1MHz	1
5	Resistors	1-100kΩ	1
6	CRO	0-20MHz	1
7	Probes, Connecting Wires	-	1

4.3 THEORY:

4.3.1 ASTABLE MULTIVIBRATOR:

The **555 Oscillator** is another type of relaxation oscillator for generating stabilized square wave output waveforms of either a fixed frequency of up to 500kHz or of varying duty cycles from 50 to 100%.

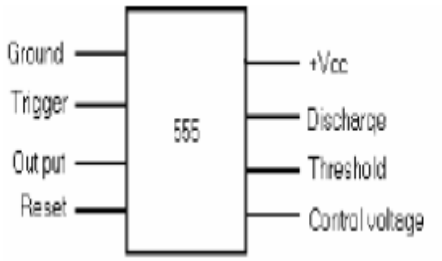
In order to get the 555 Oscillator to operate as an astable multivibrator it is necessary to continuously re-trigger the 555 IC after each and every timing cycle.

This re-triggering is basically achieved by connecting the *trigger* input (pin 2) and the *threshold* input (pin 6) together, thereby allowing the device to act as an astable oscillator. Then the 555 Oscillator has no stable states as it continuously switches from one state to the other. Also the single timing resistor of the previous monostable multivibrator circuit has been split into two separate resistors, R1 and R2 with their junction connected to the *discharge* input (pin 7) .

4.4 PROCEDURE:

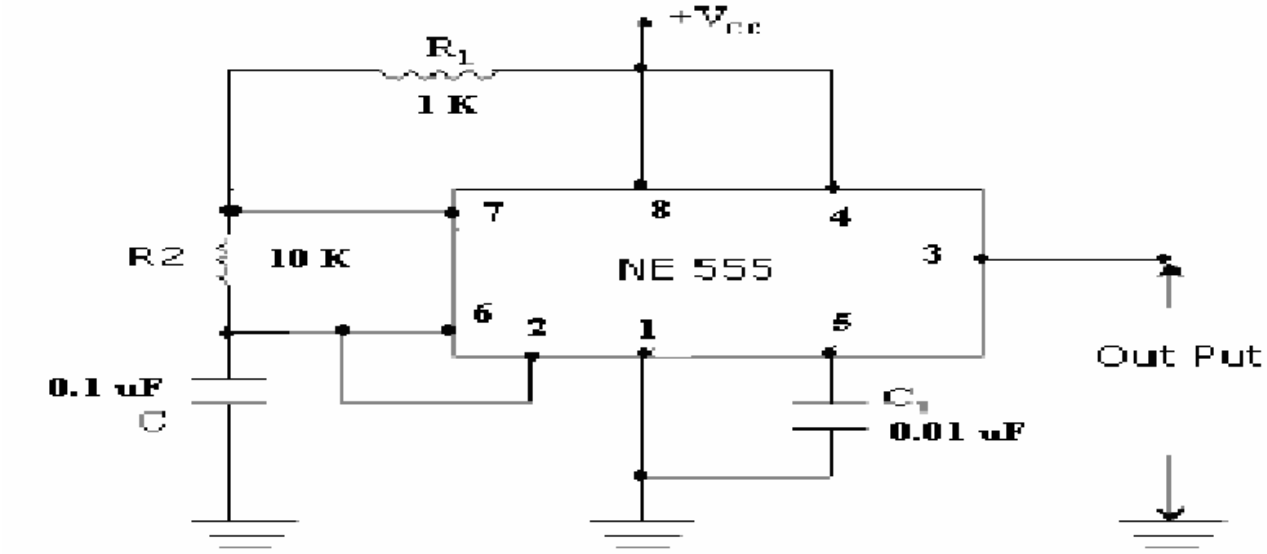
ASTABLE:

1. Connect the components/equipment as shown in the circuit diagram.
2. Observe the square wave output at pin 3 on CRO.
3. Calculate Duty cycle from the output waveform & compare with theoretical value.
4. Plot the output waveforms.

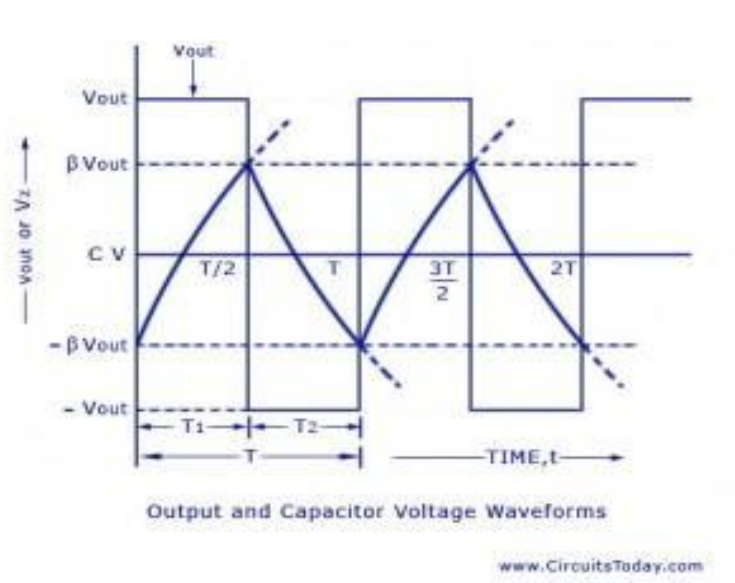


4.5 CIRCUIT DIAGRAM

ASTABLE MULTIVIBRATOR:



4.6 EXPECTED WAVEFORMS:



4.7 Output and Capacitor Voltage Waveforms

CALCULATIONS

$$t_1 = 0.693(R_1 + R_2).C$$

and

$$t_2 = 0.693 \times R_2 \times C \qquad T = t_1 + t_2 = 0.693(R_1 + 2R_2).C$$

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2).C}$$

$$\text{Duty Cycle} = \frac{T_{ON}}{T_{OFF} + T_{ON}} = \frac{R_1 + R_2}{(R_1 + 2R_2)} \%$$

4.8 RESULT:

4.9 PRE LAB QUESTIONS:

1. What are the applications of IC555?
2. Why feedback is not used in Schmitt trigerr?
3. What is the output of Schmitt trigger for different inputs?
4. How output of Schmitt trigger varies to +Vsat and – Vsat?
5. Why positive feedback is used in Schmitt trigger?

4.10 POST LAB QUESTIONS:

1. What is the other name for Astable multivibrator (MSMV)?
2. When MSMV is in stable state, what is the output level?
3. Why trigger is required in the case of MSMV?
4. Which type of trigger pulse is required for MSMV?
5. What is the formula for the output pulse width of MSMV?
6. How long MSMV stays in unstable state?

EXPERIMENT NO: 5

MONOSTABLE MULTIVIBRATOR USING IC555 TIMER

5.1 AIM:

To design a Monostable Multivibrator using IC555 and compare it is theoretical and practical pulse width.

5.2 COMPONENTS & EQUIPMENT REQUIRED: -

S.No	Device	Range / Rating	Quantity (in No's)
1	Bread Board		1
2	IC555		1
3	Capacitors		1
4	Function Generator		1
5	Resistors		1
6	CRO		1
7	Probes, Connecting Wires		1

5.3 THEORY:

5.3.1 MONOSTABLE MULTIVIBRATOR:

Monostable multivibrator is also called as one–shot Multivibrator. When the output is low, the circuit is in stable state, transistor T1 is ON and Capacitor C is shorted to the ground. However, upon application of a negative trigger pulse to Pin–2, transistor T1 is turned OFF, which releases short circuit across the external capacitor and drives the output High. The capacitor C now starts charging up toward VCC through R. However when the voltage across the external capacitor equals 2/3 VCC, upper comparator‟s output switches from low to high which in turn derives the output to its low state. And the output of the flip flop turns transistor T1 ON, and hence the capacitor C rapidly discharges through the transistor. The output of the Monostable remains low until a trigger pulse is again applied.

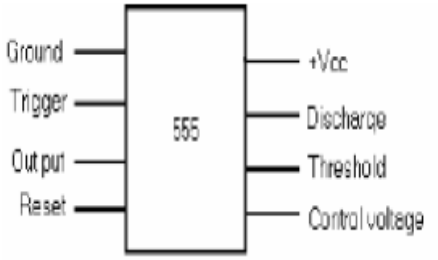
Then the cycle repeats. The time during which the output remains high is given by

$$\mathbf{tp = 1.1\ RC}$$

5.4 PROCEDURE:

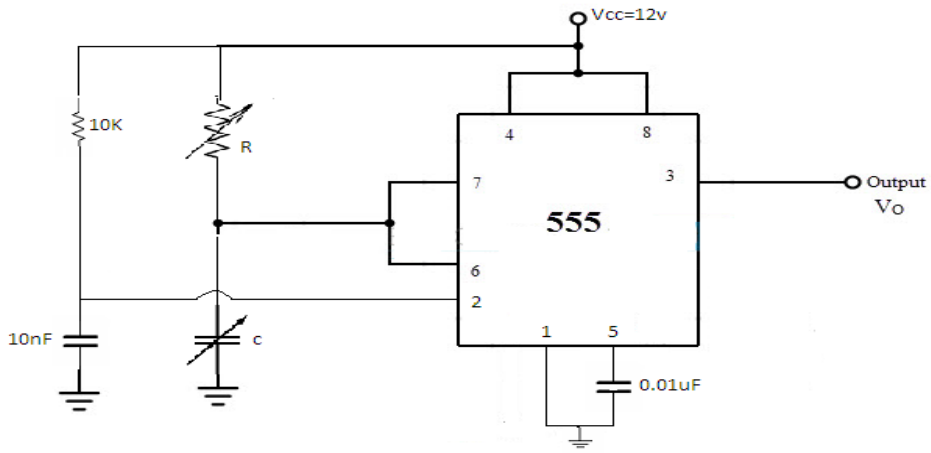
MONOSTABLE:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Connect function generator at the trigger input.
4. Connect channel-1 of CRO to the trigger input and channel-2 of CRO to the output (Pin 3).
5. Using Function Generator, apply 1 KHz square wave with amplitude of approx. equal to 9 Vpp at the trigger input.
6. Observe the output voltage with respect to input and note down the pulse width and amplitude.
7. Now connect channel-2 of CRO across capacitor and observe the voltage across the capacitor and note it down.
8. Compare the practical pulse width noted in the step above with its theoretical value (tp=1.1 RC)



5.5 CIRCUIT DIAGRAM

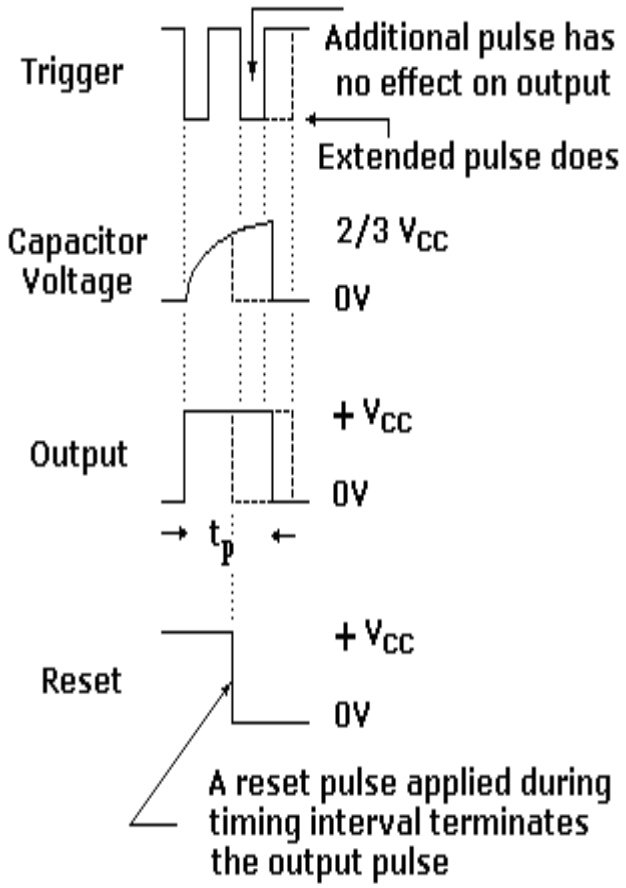
MONOSTABLE MULTIVIBRATOR:



R	C	Theoretical Time period T_{ON}=1.1 RC	Practical Time period	$V_{o(p-p)}$
47kΩ	0.1 µF			
22KΩ	0.1 µF			
10KΩ	0.1µF			

5.6 EXPECTED WAVEFORMS:

MONOSTABLE:



5.7 CALCULATIONS:

MONOSTABLE:

Theoretical Pulse width

$$tp = 1.1\ RC$$

Practical Pulse width

$$tp = 1.1\ RC$$

5.8 RESULT:

5.9 PRE LAB QUESTIONS:

1. What are the applications of IC741?
2. Why feedback is not used in Schmitt trigerr?
3. What is the output of Schmitt trigger for different inputs?
4. How output of Schmitt trigger varies to +Vsat and – Vsat?
5. Why positive feedback is used in Schmitt trigger?

5.10 POST LAB QUESTIONS:

1. What is the other name for monostable multivibrator (MSMV)?
2. When MSMV is in stable state, what is the output level?
3. Why trigger is required in the case of MSMV?
4. Which type of trigger pulse is required for MSMV?
5. What is the formula for the output pulse width of MSMV?
6. How long MSMV stays in unstable state?

EXPERIMENT NO: 6

SCHMITT TRIGGER CIRCUITS USING IC555 & IC 741

6.1 AIM:

To study the Schmitt trigger characteristics by using IC741& IC 555 and compare theoretical and practical values of the Upper Threshold voltage, VUT and the Lower Threshold voltage, VLT.

6.2 COMPONENTS & EQUIPMENT REQUIRED: -

S.No	Device	Range / Rating	Quantity (in No's)
1	Bread Board	-	1
2	IC741 & IC 555	-	1
3	Capacitors	µF	1
4	Function Generator	0-1MHz	1
5	Resistors	1-100kΩ	1
6	CRO	0-20MHz	1
7	Probes, Connecting Wires	-	1

6.3 THEORY:

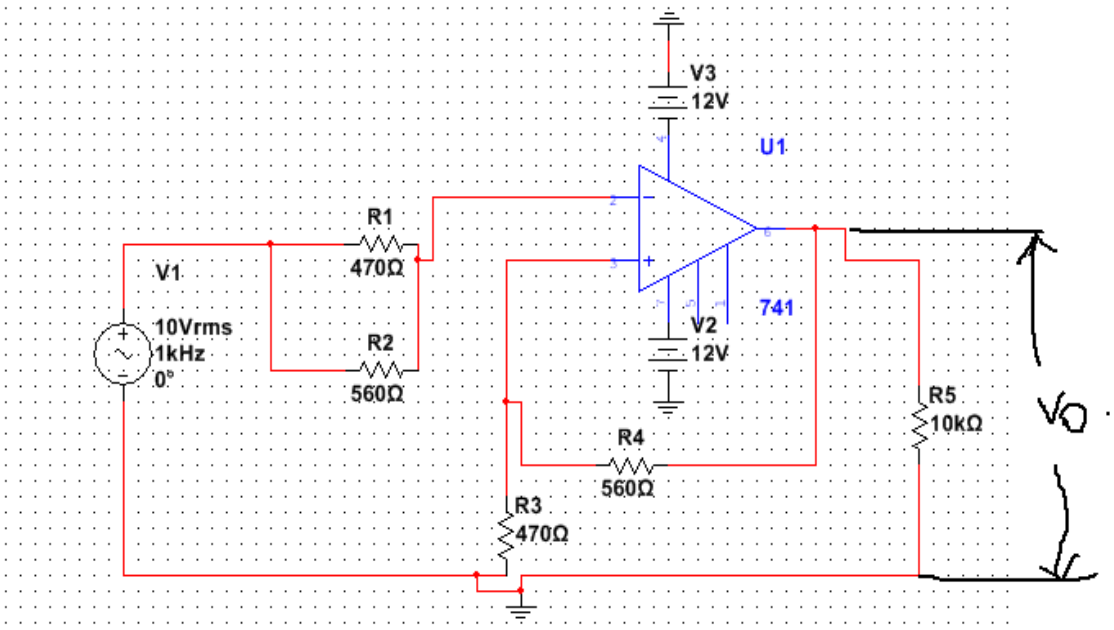
Circuit shows an inverting comparator with positive feedback. This circuit converts an irregular shaped waveform to square wave or pulse. This circuit is known as Schmitt trigger or Regenerative comparator or Squaring circuit. The input voltage Vin triggers (changes the state of) the output Vo every time it exceeds certain voltage levels called Upper threshold voltage, VUT and Lower threshold voltage, VLT. The hysteresis width is the difference between these two threshold voltages i.e. VUT – VLT. These threshold voltages are calculated as follows.

$$VUT = (R1/R1+R2)\ Vsat \text{when } Vo= Vsat$$

$$VLT = (R1/R1+R2)\ (-Vsat) \text{when } Vo= -Vsat$$

The output of Schmitt trigger is a square wave when the input is sine wave or triangular wave, where as if the input is a saw tooth wave then the output is a pulse wave.

6.4 CIRCUIT DIAGRAM:



schmitt trigger using IC 741

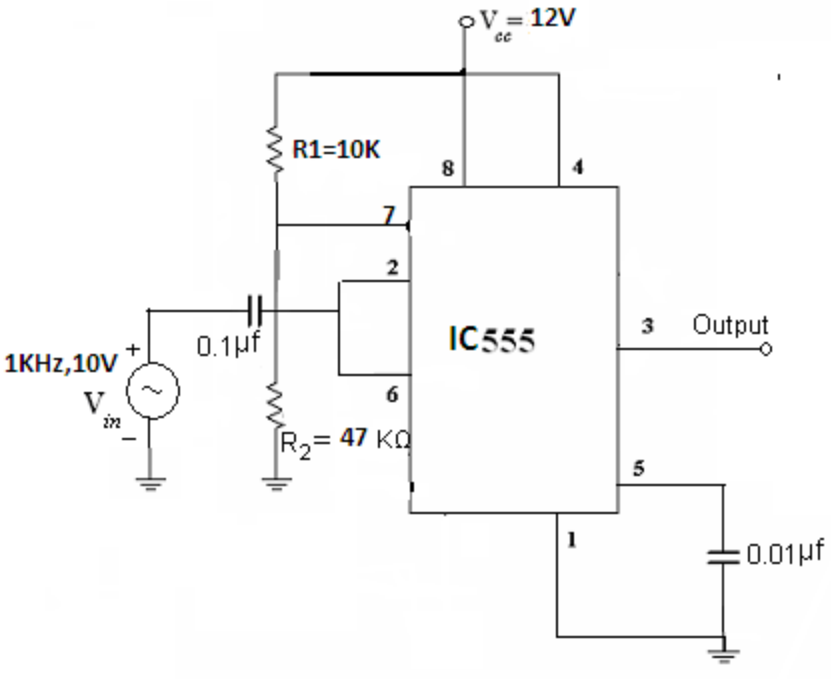
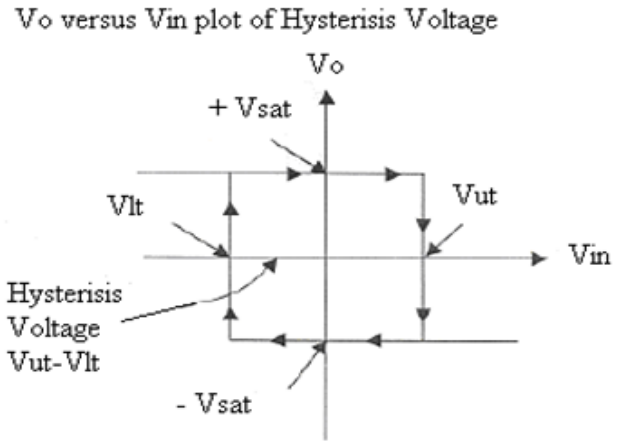


Fig: Schmitt Trigger using IC555

6.5 PROCEDURE:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Apply the input sine wave using function generator.
4. Connect the channel–1 of CRO at the input terminals and Channel-2 at the output terminals.
5. Observe the output square waveform corresponding to input sinusoidal signal.
6. Overlap both the input and output waves and note down voltages at positions on sine wave where output changes its state. These voltages denote the Upper threshold voltage and the Lower threshold voltage (see expected waveforms below).
7. Verify that these practical threshold voltages are almost same as the theoretical threshold voltages calculated using formulas given in the theory section above.
8. Sketch the waveforms by noting down the amplitude and the time period of the input Vin and the output Vo.

6.6 EXPECTED WAVEFORMS:



6.7 TABLE:

	V_{UTP}	V_{LTP}	V_H	T_{on}	T_{off}	$V_{o(p-p)}$
IC741						
IC 555						

6.8 RESULT:

6.9 PRE LAB QUESTIONS:

1. what is a output of Schmitt trigger if input varies?
2. Give the formulae for hysteresis voltage?
3. What is the other name for Schmitt trigger?
4. Give the formulae for Upper Threshold Point?
5. Give the formulae for Lower Threshold Point?
6. What are the application of emitter coupled Bistable MV?

6.10 POST LAB QUESTIONS:

1**.** what is a output of Schmitt trigger if input varies?
2. Define hysteresis voltage?
3. What is the other name for Schmitt trigger?
4. What is UTP?
5. What is LTP?
6. What are the application of emitter coupled Bistable MV?

EXPERIMENT NO: 7

IC 565 PLL APPLICATIONS

7.1 AIM:

To study the operation of NE565 PLL
To use NE565 as multiplier

7.2 COMPONENTS & EQUIPMENT REQUIRED: -

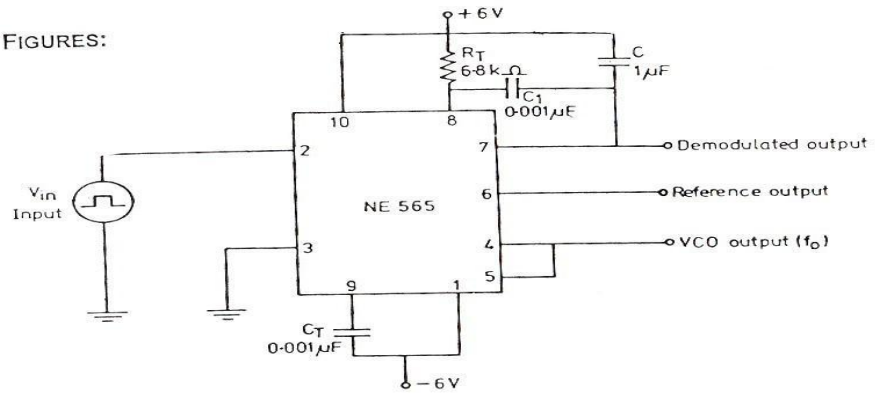
S.No	Device	Range / Rating	Quantity (in No's)
1	Bread Board	-	1
2	IC565	-	1
3	Capacitors	0.001 F, 0.1 F Capacitor	2, 1
4	Function Generator	0-1MHz	1
5	Resistors	6.8 kΩ	1
6	CRO	0-20MHz	1
7	Probes, Connecting Wires	-	

7.3 THEORY:

The 565 is available asa14-pin DIP package.It is produced by signatic corporation.
The output frequency of the VCO can be rewritten as Where RT and CTare the external resistor and capacitor connected to pin8 and pin9. A value between 2k and 20k is recommended for RT .The VCO free running frequency is adjusted with RTand CT to be at the centre for the input frequency range.

7.4 CIRCUIT DIAGRAM:

FIGURES:



7.5 PROCEDURE:

1. Connect the circuit using the component values as shown in the figure
2. Measure the free running frequency of VCO at pin4 with the input signal Vinset=Zero. Compare it with the calculated value=0.25/RTCT
3. Now apply the input signal of 1Vpp squarewaveata1kHz to pin2
4. Connect1 channel of the scope to pin2 and display this signal on the scope
5. Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency f1 gives the lower ends of the capture range. Go on increase the input frequency, till PLL tracks the input signal, say to a frequency f2.This frequency f2 gives the upper end of the lock range. If the input frequency is increased further the loop will get unlocked.
6. Now gradually decrease the input frequency till the PLL is a gain locked. This is the frequency f3, the upper end of the capture range .Keep on decreasing the input frequency until the loop is unlocked. This frequency f4 gives the lower end of the lock range
7. The lock rangefL=(f2– f4) compare with the calculated value. Also the capture range is fc=(f3– f1). Compare it with the calculated value of capture range.
8. To use PLL as a multiplier, make connections as show in fig. The circuit uses a 4-bit binary counter 7490 used as a divide-by-5circuit.
9. Set the input signal at1Vpp square wave at500Hz
10. Vary the VCO frequency by adjusting the 20K potentiometer till the PLL is locked. Measure the output frequency.
11. Repeat step 9 and10 for input frequency of 1kHz and1.5kHz.

7.6 OBSERVATIONS:

fo =

fL=

fC=

7.8 CALCULATIONS:

$$f_L=(f_2-f_4)=\frac{7.8fo}{12}$$

$$f_c=(f_3-f_1)=\frac{f_L}{(2)(3.6)(10^3)xC}^{1/2}$$

7.8 RESULT :

7.9 PRE LAB QUESTIONS:

1. What does u mean by PLL?
2. List the applications of 565 PLL
3. Define lock range in PLL
4. Define capture range in PLL.
5. Define pull-in time in PLL.

7.10 POST LAB QUESTIONS:

1. What is the function of low pass filter in phase-locked loop.
2. At which state the phase-locked loop tracks any change in input frequency.
3. At what range the PLL can maintain the lock in the circuit.
4. Write formulae lock range in PLL.
5. Write formulae capture range in PLL.

EXPERIMENT NO: 8

INSTRUMENTATION AMPLIFIER USING IC 741

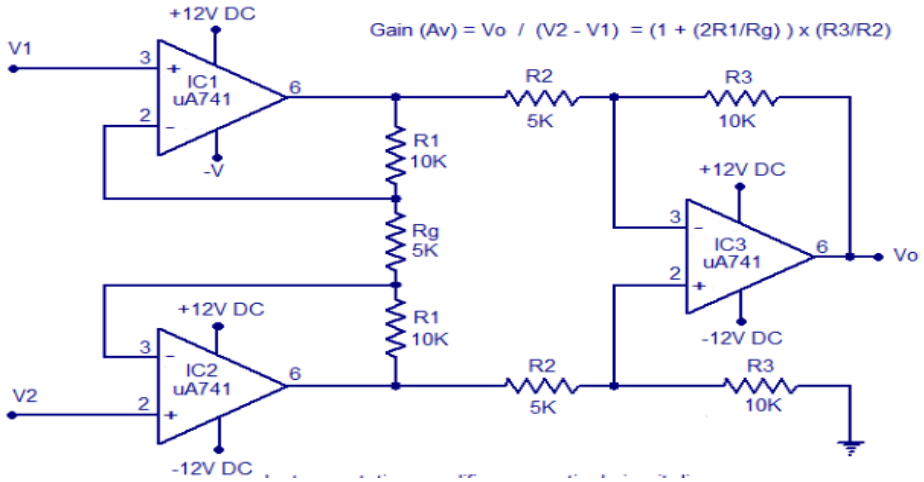
8.1 AIM:

To analyse the output of instrumentation amplifier using IC 741

8.2 COMPONENTS & EQUIPMENT REQUIRED: -

S.No	Device	Range / Rating	Quantity (in No's)
1	Bread Board	-	1
2	IC 741	-	1
3	Resistors	1-100kΩ	7
4	CRO	0-20MHz	1
5	Probes, Connecting Wires	-	
6	Regulated Power supply	0-12V	1

7.9 CIRCUIT DIAGRAM:



7.10 THEORY:

Instrumentation amplifier is a kind of differential amplifier with additional input buffer stages. The addition of input buffer stages makes it easy to match (impedance matching) the amplifier with the preceding stage. Instrumentation are commonly used in industrial test and measurement application. The instrumentation amplifier also has some useful features like low offset voltage, high CMRR (Common mode rejection ratio), high input resistance, high gain etc. In the circuit diagram, opamps labelled A1 and A2 are the input buffers. Anyway the gain of these buffer stages are not unity because of the presence of

R1 and Rg. Op amp labelled A3 is wired as a standard differential amplifier. R3 connected from the output of A3 to its non inverting input is the feedback resistor. R2 is the input resistor. The voltage gain of the instrumentation amplifier can be expressed by using the equation below.

$$\text{Voltage gain (Av)} = Vo/(V2-V1) = (1 + 2R1/Rg) \times R3/R2$$

8.5 PROCEDURE:

- Connect the circuit as shown in fig
- The amplifier operates from +/-12V DC and has a gain 10.
- If you need a variable gain, then replace Rg with a 5K POT.
- Measure the Voltage gain by using given formulae.

8.6 RESULT:

EXPERIMENT NO: 9

MULTIPLEXER AND DEMULTIPLEXER

9.1 AIM:

To design and set up the following circuit

i. 4:1 Multiplexer (MUX) using only NAND gates.
ii. 1:4 Demultiplexer (DE-MUX) using only NAND gates.

9.2 LEARNING OBJECTIVE:

To learn about various applications of multiplexer and de-multiplexer
To learn and understand the working of IC 74153 and IC 74139
To learn to realize any function using Multiplexer

9.3 THEORY:

Multiplexers are very useful components in digital systems. They transfer a large number of information units over a smaller number of channels, (usually one channel) under the control of selection signals. Multiplexer means many to one. A multiplexer is a circuit with many inputs but only one output. By using control signals (select lines) we can select any input to the output. Multiplexer is also called as data selector because the output bit depends on the input data bit that is selected. The general multiplexer circuit has 2^n input signals, n control/select signals and 1 output signal.

De-multiplexers perform the opposite function of multiplexers. They transfer a small number of information units (usually one unit) over a larger number of channels under the control of selection signals. The general de-multiplexer circuit has 1 input signal, n control/select signals and 2^n output signals. De-multiplexer circuit can also be realized using a decoder circuit with enable.

9.4 COMPONENTS REQUIRED:

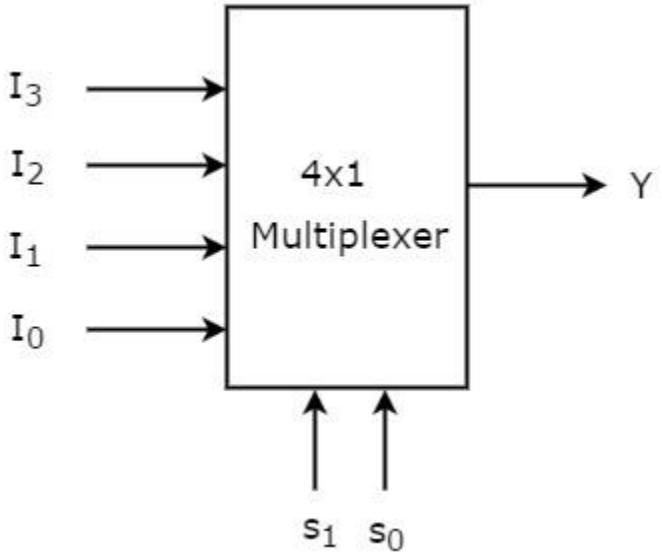
IC 7400, IC 7410, IC 7420, IC 7404, IC 74153, IC 74139, Patch Cords & IC Trainer Kit.

9.5 PROCEDURE:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

9.6 CIRCUIT DIAGRAM:

4:1 MULTIPLEXER

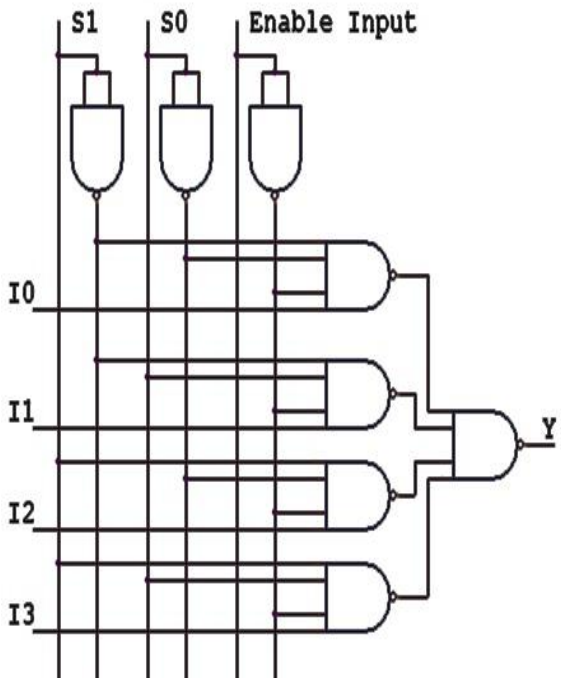


Output Y= E'S1'S0'I0 + E'S1'S0I1 + E'S1S0'I2 + E'S1S0I3

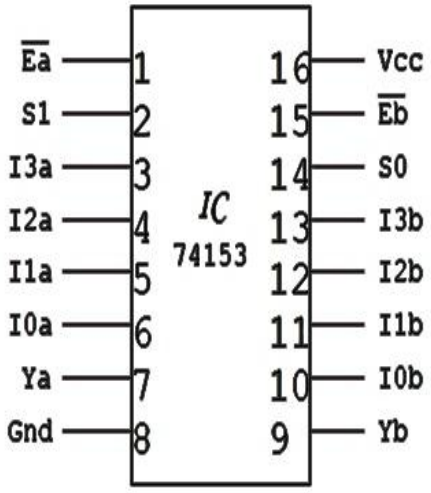
TRUTH TABLE

Select Inputs		Enable Input	Inputs				Out puts
S_1	**S_0**	**E**	**I_0**	**I_1**	**I_2**	**I_3**	**Y**
X	X	1	X	X	X	X	0
0	0	0	0	X	X	X	0
0	0	0	1	X	X	X	1
0	1	0	X	0	X	X	0
0	1	0	X	1	X	X	1
1	0	0	X	X	0	X	0
1	0	0	X	X	1	X	1
1	1	0	X	X	X	0	0
1	1	0	X	X	X	1	1

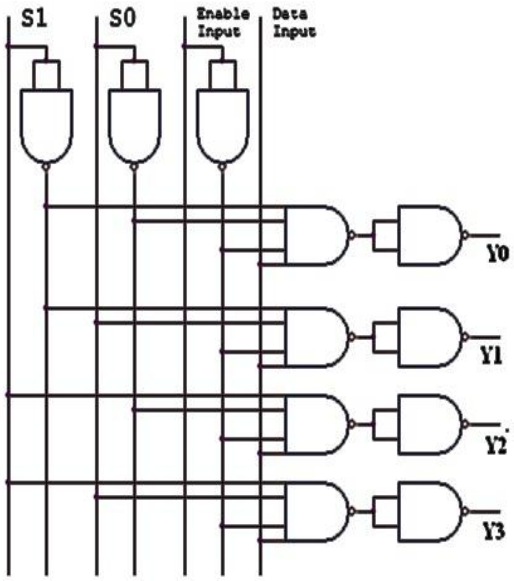
Realization Using NAND Gates TRUTH TABLE



VERIFY IC 74153 MUX (DUAL 4:1 MULTIPLEXER)



DE-MUX USING NAND GATES:

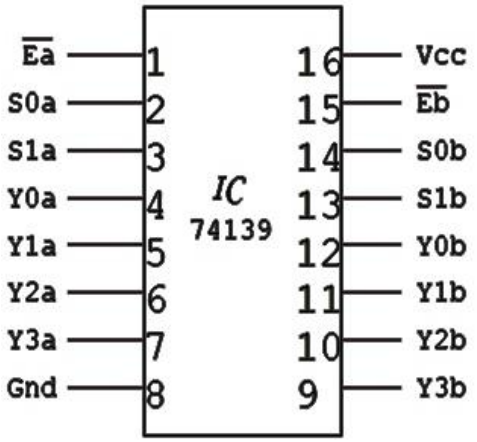


Enable Inputs	Data Input	Select Inputs		Outputs			
E	**D**	**S_1**	**S_0**	**Y_3**	**Y_2**	**Y_1**	**Y_0**
1	0	X	X	X	X	X	X
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	1	0	0
0	1	1	1	1	0	0	0

VERIFICATION OF IC 74139 (DEMUX)

TRUTH TABLE

Inputs			Outputs			
Ea	**S_1**	**S_0**	**Y_3**	**Y_2**	**Y_1**	**Y_0**
1	X	X	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1



9.7 RESULT:

9.8 PRE LAB QUESTIONS:

1. What is a multiplexer?
2. What is a de-multiplexer?
3. What are the applications of multiplexer and de-multiplexer?
4. Derive the Boolean expression for multiplexer and de-multiplexer.
5. How do you realize a given function using multiplexer

9.9 POST LAB QUESTIONS:

1. What is the difference between multiplexer & demultiplexer?
2. In 2n to 1 multiplexer how many selection lines are there?
3. How to get higher order multiplexers?
4. Implement an 8:1 mux using 4:1 mux?

EXPERIMENT NO: 10

ENCODER AND DECODER

10.1 AIM:

To set up a circuit of Decimal-to-BCD Encoder using IC 74147.
To realize a decoder circuit using basic gates and to verify IC 74LS139

10.2 LEARNING OBJECTIVE:

- To learn about various applications of Encoders and Decoder.
- To learn and understand the working of IC 74147, IC 74LS139.
- To learn to do code conversion using encoders.

10.3 COMPONENTS REQUIRED:

IC 74147, IC 74LS139, Patch chords & IC Trainer Kit

10.4 THEORY:

An encoder performs a function that is the opposite of decoder. It receives one or more signals in an encoded format and output a code that can be processed by another logic circuit. One of the advantages of encoding data, or more often data addresses in computers, is that it reduces the number of required bits to represent data or addresses. For example, if a memory has 16 different locations, in order to access these 16 different locations, 16 lines (bits) are required if the addressing signals are in 1 out of *n* format. However, if we code the 16 different addresses into a binary format, then only 4 lines (bits) are required. Such a reduction improves the speed of information processing in digital systems.

A decoder is a combinational circuit that connects the binary information from 'n' input lines to a maximum of 2^n unique output lines. Decoder is also called a min-term generator/maxterm generator. A min-term generator is constructed using AND and NOT gates. The appropriate output is indicated by logic 1 (positive logic). Max-term generator is constructed using NAND gates. The appropriate output is indicated by logic 0 (Negative logic). The IC 74139 accepts two binary inputs and when enable provides 4 individual active low outputs. The device has 2 enable inputs (Two active low).

10.5 PROCEDURE:

Encoder:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

Decoder:

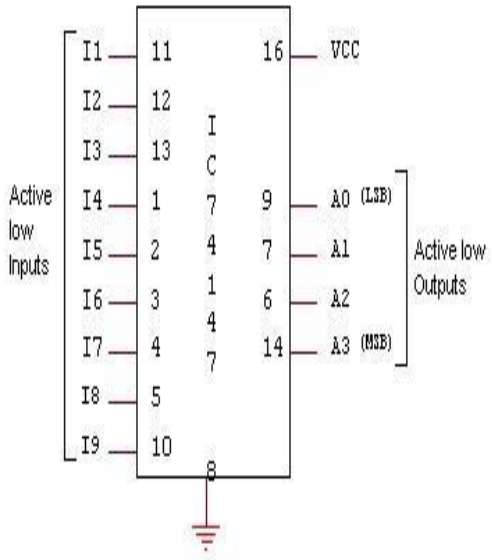
- Make the connections as per the circuit diagram.
- Change the values of G1, G2A, G2B, A, B, and C, using switches.
- Observe status of Y0, to Y7 on LED's.
- Verify the truth table.

10.6 CIRCUIT DIAGRAM:

DECIMAL-TO BCD ENCODER USING IC 74147.

TRUTH TABLE

INPUTS									OUTPUTS			
I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	A_3	A_2	A_1	A_0
1	1	1	1	1	1	1	1	0	0	1	1	0
X	X	X	X	X	X	X	0	1	0	1	1	1
X	X	X	X	X	X	0	1	1	1	0	0	0
X	X	X	X	X	0	1	1	1	1	0	0	1
X	X	X	X	0	1	1	1	1	1	0	1	0
X	X	X	0	1	1	1	1	1	1	0	1	1
X	X	0	1	1	1	1	1	1	1	1	0	0
X	0	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1



2:4 DECODER (MIN TERM GENERATOR):

TRUTH TABLE:

INPUT		OUTPUT			
A	**B**	**Y0**	**Y1**	**Y2**	**Y3**
0	**0**	**1**	**0**	**0**	**0**
0	**1**	**0**	**1**	**0**	**0**
1	**0**	**0**	**0**	**1**	**0**
1	**1**	**0**	**0**	**0**	**1**

BOOLEAN EXPRESSION:

$Y0 = \overline{AB}$

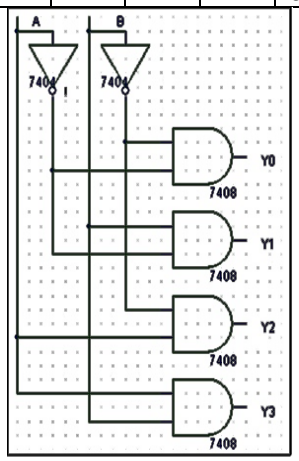
$Y1 = \overline{A}B$

$Y2 = A\overline{B}$

$Y3 = AB$

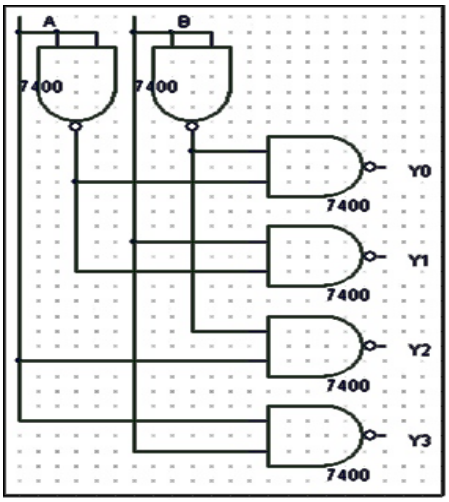
TRUTH TABLE

INPUT		OUTPUT			
A	**B**	**Y0**	**Y1**	**Y2**	**Y3**
0	**0**	**0**	**1**	**1**	**1**
0	**1**	**1**	**0**	**1**	**1**
1	**0**	**1**	**1**	**0**	**1**
1	**1**	**1**	**1**	**1**	**0**



2:4 DECODER (MAX TERM GENERATOR):

CIRCUIT DIAGRAM:



10.7 RESULT:

10.8 PRE LAB QUESTIONS:

1. What is a priority encoder?
2. What is the role of an encoder in communication?
3. What is the advantage of using an encoder?
4. What are the uses of validating outputs?
5. What are the applications of decoder?

10.9 POST LAB QUESTIONS:

1. What is the difference between decoder & encoder.
2. What are code converters.
3. What is the difference between decoder and de-mux.

EXPERIMENT NO: 11

REALISATION OF DIFFERENT FLIP-FLOPS USING LOGIC GATES

11.1 AIM: Truth Table verification of

1) RS Flip Flop
2) T type Flip Flop.
3) D type Flip Flop.
4) JK Flip Flop.
5) JK Master Slave Flip Flop.

11.2 LEARNING OBJECTIVE:

To learn about various Flip-Flops
To learn and understand the working of Master slave FF
To learn about applications of FFs
Conversion of one type of Flip flop to another

11.3 COMPONENTS REQUIRED:

IC 7408, IC 7404, IC 7402, IC 7400, Patch Cords & IC Trainer Kit.

11.4 THEORY:

Logic circuits that incorporate memory cells are called *sequential logic circuits*; their output depends not only upon the present value of the input but also upon the previous values.

Sequential logic circuits often require a timing generator (a clock) for their operation. The latch (flip-flop) is a basic bi-stable memory element widely used in sequential logic circuits. Usually there are two outputs, Q and its complementary value. Some of the most widely used latches are listed below.

SR LATCH:

An S-R latch consists of two cross-coupled NOR gates. An S-R flip-flop can also be design using cross-coupled NAND gates as shown. The truth tables of the circuits are shown below.

A clocked S-R flip-flop has an additional clock input so that the S and R inputs are active only when the clock is high. When the clock goes low, the state of flip-flop is latched and cannot change until the clock goes high again. Therefore, the clocked S-R flip-flop is also called "enabled" S-R flip-flop.

A D latch combines the S and R inputs of an S-R latch into one input by adding an inverter. When the clock is high, the output follows the D input, and when the clock goes low, the state is latched.

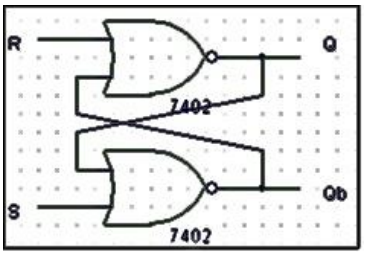
A S-R flip-flop can be converted to T-flip flop by connecting S input to Qb and R to Q.

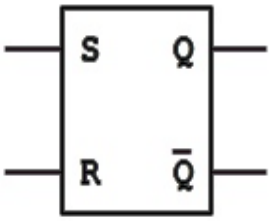
11.5 PROCEDURE:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.
-

11.6 CIRCUIT DIAGRAM:

1) S-R LATCH:



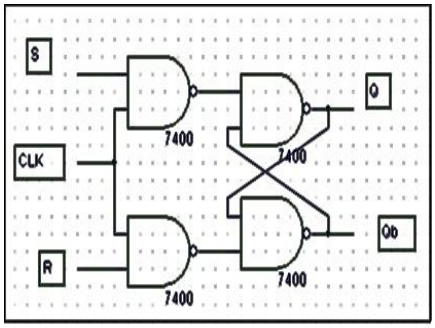


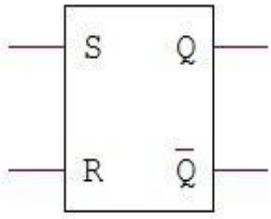
(A) LOGIC DIAGRAM **(B) SYMBOL**

TRUTH TABLE

S	R	Q+	*Q*b+
0	0	Q	*Q*b
0	1	0	1
1	0	1	0
1	1	0*	0*

2) SR-FLIP FLOP:





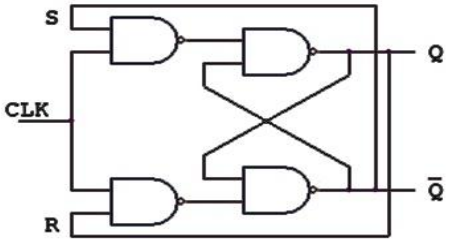
(A) LOGIC DIAGRAM **(B) SYMBOL**

TRUTH TABLE FOR SR- FF

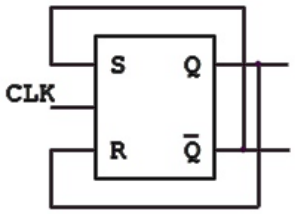
S	**R**	**Q+**	***Q*n+**
0	0	Q	*Q*n
0	1	0	1
1	0	1	0
1	1	0*	0*

3) CONVERSION OF SR-FLIP FLOP TO T-FLIP FLOP (Toggle)

LOGIC DIAGRAM



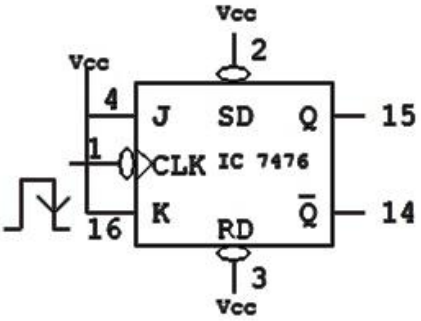
SYMBOL



T FLIP FLOP USING IC 7476

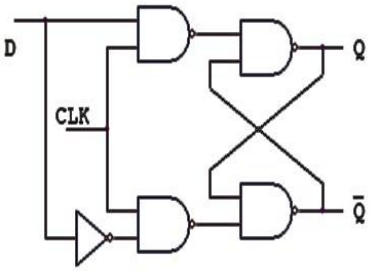
TRUTH TABLE FOR T - FF

T	Qn + 1
0	Qn
1	Qn

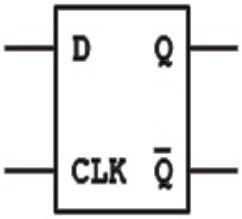


4) CONVERSION OF SR-FLIP FLOP TO D-FLIP FLOP :

LOGIC DIAGRAM



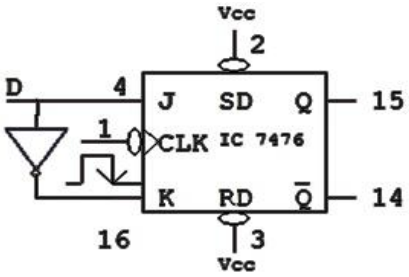
SYMBOL



TRUTH TABLE

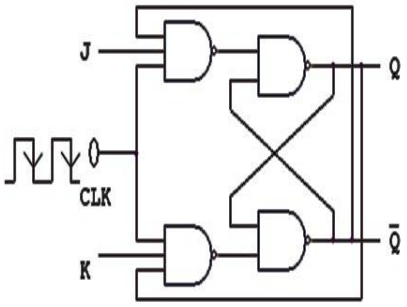
CLOCK	D	Q+	Q+
0	X	Q	Q
1	0	0	1
1	1	1	0

D FLIP FLOP USING IC 7476



5) CONVERSION OF SR-FLIP FLOP TO JK-FLIP FLOP

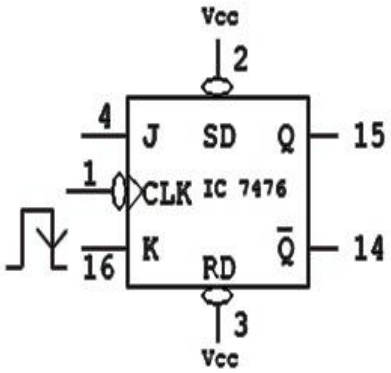
LOGIC DIAGRAM



TRUTH TABLE

Clock	J	K	Q+	Q'+	Comment
1	0	0	Q	Q'	No Change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Q'	Q	Toggle

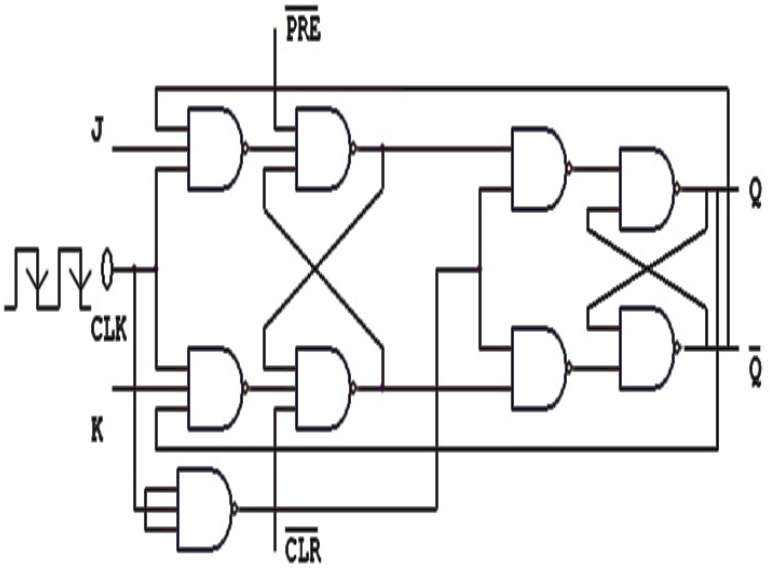
LOGIC DIAGRAM



TRUTH TABLE

	RD	Clock	J	K	Q	Q'	Comment
0	0	Not Allowed					
0	1	X	X	X	1	0	Set
1	0	X	X	X	0	1	Reset
1	1	1	0	0	NC	NC	Memory
1	1	1	0	1	0	1	Reset
1	1	1	1	0	1	0	Set
1	1	1	1	1	Q'	Q	Toggle

6) JK MASTER SLAVE FLIP FLOP



TRUTH TABLE

PRE' = CLR' = 1

Clock	J	K	Q+	Q'+	Comment
1	0	0	Q	Q'	No Change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Race Around		

11.7 RESULT:

11.8 PRE LAB QUESTIONS:

1. What is the difference between Flip-Flop & latch?
2. Give examples for synchronous & asynchronous inputs?
3. What are the applications of different Flip-Flops?
4. What is the advantage of Edge triggering over level triggering?

11.9 POST LAB QUESTIONS:

1. What is the relation between propagation delay & clock frequency of flip-flop?
2. What is race around in flip-flop & how to overcome it?
3. Convert the J K Flip-Flop into D flip-flop and T flip-flop?

EXPERIMENT NO: 12
4-BIT COUNTERS

12.1 AIM:

To design IC 74193 as a up/down counter

12.2 LEARNING OBJECTIVE:

To learn about presettable Counter and its application

12.3 COMPONENTS REQUIRED:

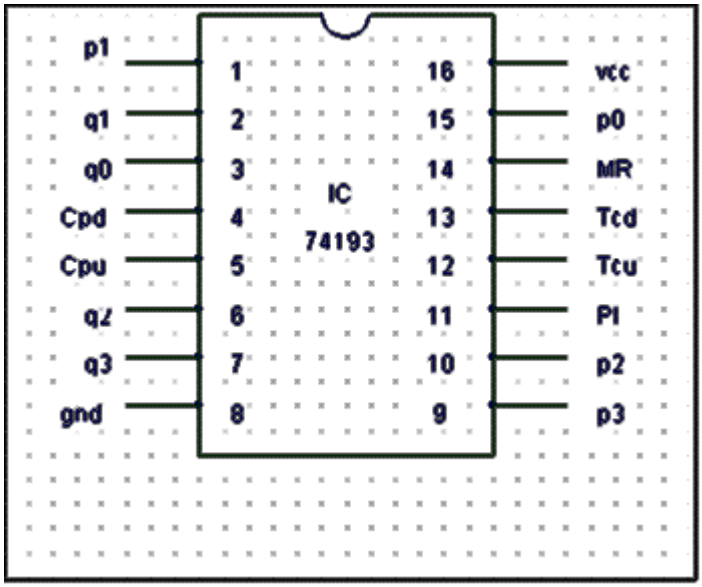
IC 74193, Patch Cords & IC Trainer Kit

12.4 PROCEDURE:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

12.5 CIRCUIT DIAGRAM:

PIN DETAILS OF IC 74193



1. p0, p1, p2 and p3are parallel data inputs
2. q0, q1, q2 and q3 are flip-flop outputs
3. MR: Asynchronous master reset
4. PL: Asynchronous parallel load(active low) input
5. Tcd : Terminal count down output
6. Tcu : Terminal count up output

Up counter

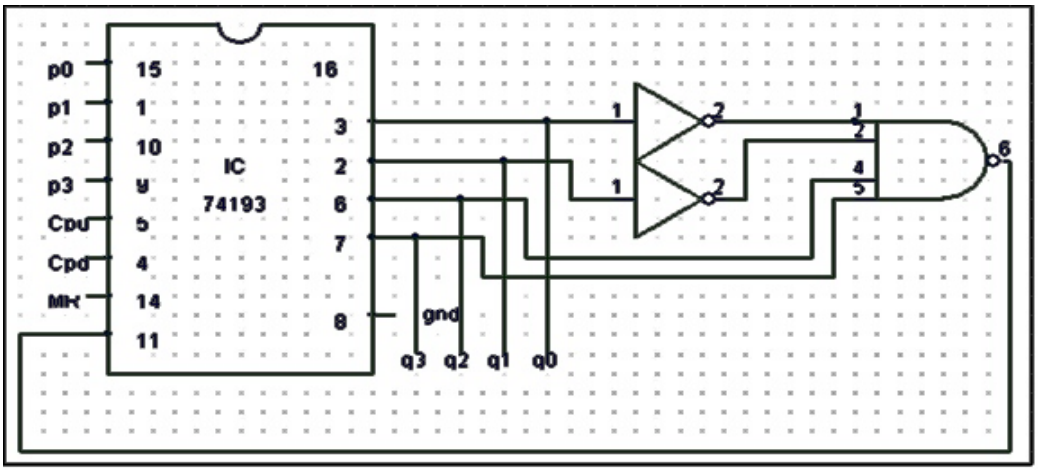
CLK	Q_D	Q_C	Q_B	Q_A
0	1	1	1	1
1	1	1	1	0
2	1	1	0	1
3	1	1	0	0
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	1	0	0	0
8	0	1	1	1
9	0	1	1	0
10	0	1	0	1
11	0	1	0	0
12	0	0	1	1
13	0	0	1	0
14	0	0	0	1
15	0	0	0	0
16	1	1	1	1

Down counter

CLK	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0

b) Design up counter for preset value 0010 and N=10

CIRCUIT DIAGRAM

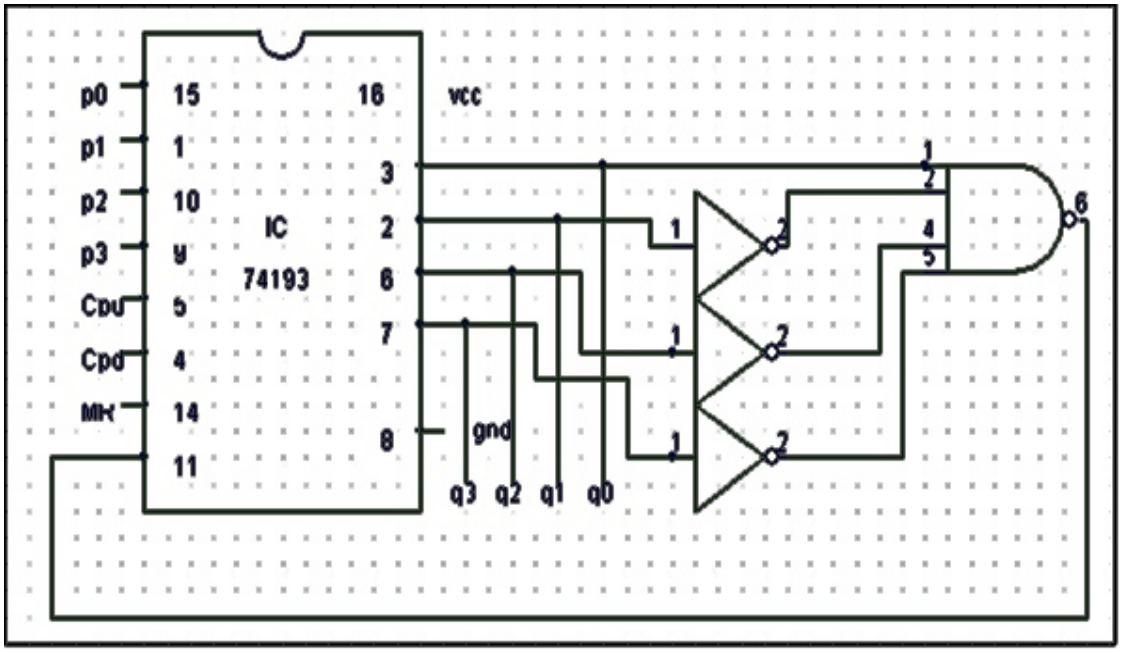


TRUTH TABLE

CLK	Q_D	Q_C	Q_B	Q_A
1	0	0	1	0
2	0	0	1	1
3	0	1	0	0
4	0	1	0	1
5	0	1	1	0
6	0	1	1	1
7	1	0	0	0
8	1	0	0	1
9	1	0	1	0
10	1	0	1	1
11	1	1	0	0
12	0	0	1	0

c) Design of down counter for preset value 1011 and N=10

CIRCUIT DIAGRAM



TRUTH TABLE

CLK	Q_D	Q_C	Q_B	Q_A
1	1	0	1	1
2	1	0	1	0
3	1	0	0	1
4	1	0	0	0
5	0	1	1	1
6	0	1	1	0
7	0	1	0	1
8	0	1	0	0
9	0	0	1	1
10	0	0	1	0
11	0	0	0	1
12	1	0	1	1

12.6 RESULT:

12.7 PRE LAB QUESTIONS:

1. What is a presettable counter?
2. What are the applications of presettable counters?
3. Explain the working of IC 74193
4. Write the circuit for preset value of 0100 and N=5 (up counter)

12.8 POST LAB QUESTIONS:

1. What is the relation between propagation delay & clock frequency of flip-flop?
2. What is race around in flip-flop & how to overcome it?
3. Convert the J K Flip-Flop into D flip-flop and T flip-flop?

EXPERIMENT NO: 13

REALISATION OF SHIFT REGISTERS

13.1 AIM:

To realize and study of Shift Register.

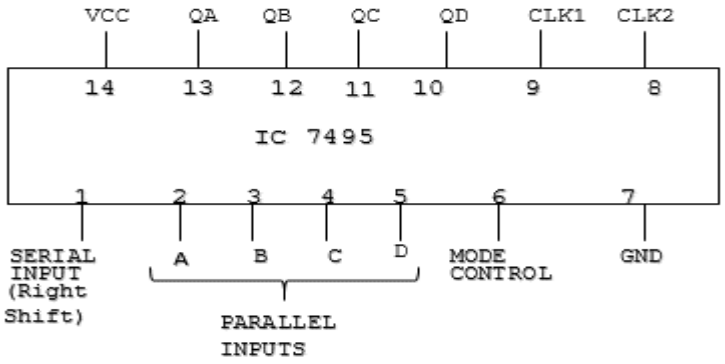
1) SISO (Serial in Serial out)
2) SIPO (Serial in Parallel out)
3) PIPO (Parallel in Parallel out)
4) PISO (Parallel in Serial out)

13.2 COMPONENTS REQUIRED: IC 7495, Patch Cords & IC Trainer Kit.

13.3 PROCEDURE:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

13.4 PIN DIAGRAM:



1) **SERIAL IN SERIAL OUT (SISO) (Right Shift)**

Serial i/p data	Shift Pulses	Q_A	Q_B	Q_C	Q_D
-	-	X	X	X	X
0	t1	0	X	X	X
1	t2	1	0	X	X
0	t3	0	1	0	X
1	t4	1	0	1	0
X	t5	X	1	0	1
X	t6	X	X	1	0
X	t7	X	X	X	1

X	t8	X	X	X	X

2) **SERIAL IN PARALLEL OUT (SIPO)**

Serial i/p data	Shift Pulses	Q_A	Q_B	Q_C	Q_D
-	-	X	X	X	X
0	t1	0	X	X	X
1	t2	1	0	X	X
0	t3	0	1	0	X
1	t4	**1**	**0**	**1**	**0**

3) **PARALLEL IN PARALLEL OUT (PIPO)**

Clock Input Terminal	Shift Pulses	Q_A	Q_B	Q_C	Q_D
-	-	X	X	X	X
CLK_2	t1	1	0	1	0

4) **PARALLEL IN SERIAL OUT (PISO)**

Clock Input Terminal	Shift Pulses	Q_A	Q_B	Q_C	Q_D
-	-	X	X	X	X
CLK_2	t1	1	0	1	0
CLK_2	t2	X	1	0	1
0	t3	X	X	1	0
1	t4	X	X	X	1
X	t5	X	X	X	X

13.5 RESULT:

13.6 PRE LAB QUESTIONS:

1. What is a recirculating register?
2. What type of register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time?
3. What is a shift register that will accept a parallel input, or a bidirectional serial load and internal shift features, called?
4. What is universal shift register?

13.7 POST LAB QUESTIONS:

1. What are the basic shift register functions?
2. What is shift register and its types?
3. How does a bidirectional shift register work?

EXPERIMENT NO: 14

DECADE COUNTER

14.1 AIM:

To design IC 7490 as a decade counter with BCD count sequence

14.2 LEARNING OBJECTIVE:

To learn about decade Counter

To use it as a divide by N counter [N<=10, say N=7, N=5]

14.3 COMPONENTS REQUIRED:

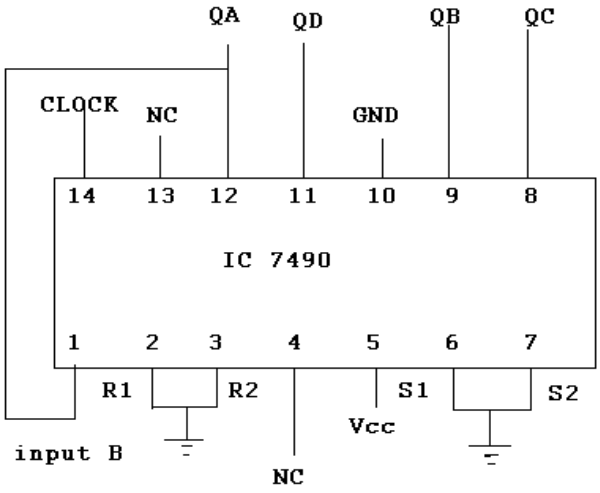
IC 7490, Patch Cords & IC Trainer Kit

14.3 PROCEDURE:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

14.4 CIRCUIT DIAGRAM:

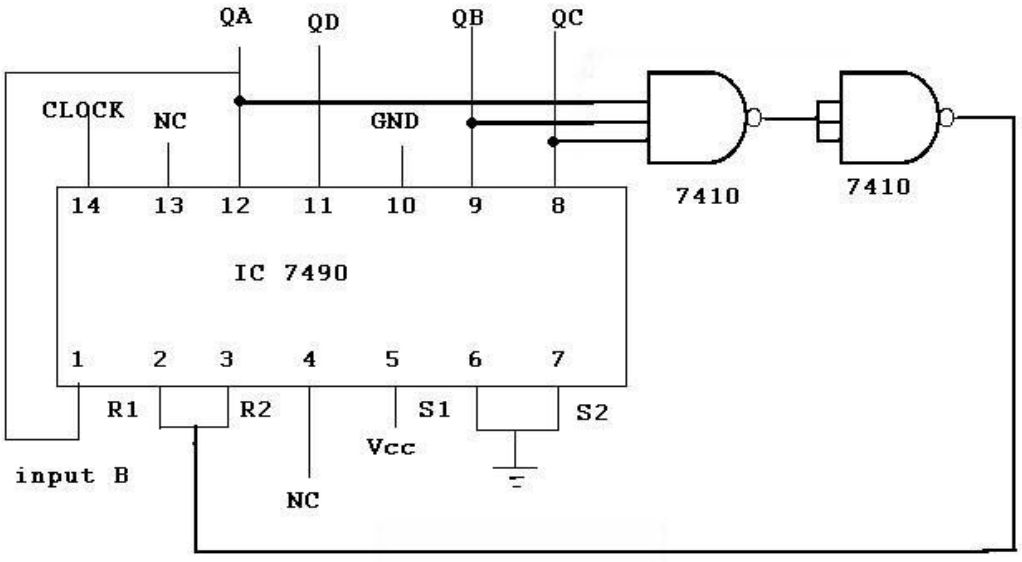
DECADE COUNTER:



TRUTH TABLE

Q_D	Q_C	Q_B	Q_A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
0	0	0	0

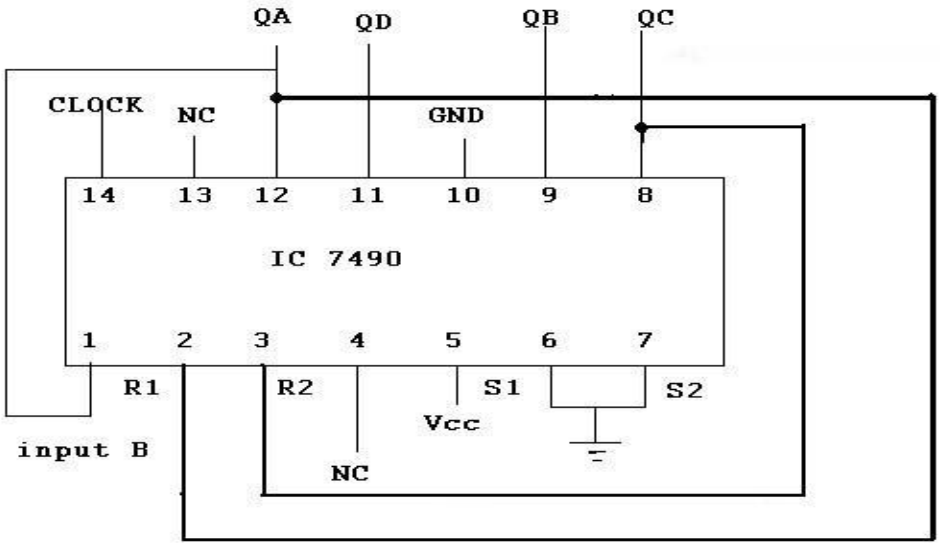
7490 AS A DIVIDE BY N COUNTER (N=7):



TRUTH TABLE

Q_D	Q_C	Q_B	Q_A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	0	0	0

DIVIDE BY 5 COUNTER:



TRUTH TABLE

Q_D	Q_C	Q_B	Q_A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	0	0	0

14.5 RESULT:

14.6 PRE LAB QUESTIONS:

1. What is a decade counter?
2. What do you mean by a ripple counter?
3. Explain the design of Modulo-N counter (N ≤ 9) using IC 7490

14.7 POST LAB QUESTIONS:

1. What is a counter?
2. What do you mean by a ripple counter USING JK FLIPFLOP ?
3. Explain the design of Modulo-N counter (N ≤ 4)