DIGITAL SYSTEM DESIGN LABORATORY

III Semester: ECE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
AECB10	Core	0	0	2	1	30	70	100
Contact Classes: Nil	Tutorial Classes: 24	Practical Classes: 45				Total Classes: 69		

OBJECTIVES:

The course should enable the students to:

I. Design of combinational circuits using Verilog Hardware Description Language.

II. Implementation of Sequential circuits using Verilog Hardware Description Language.

III. Demonstration of different case studies for Verilog HDL implementation.

COURSE LEARNING OUTCOMES:

1. Understand number systems, binary addition and subtraction, 2's complement Representation and operations with this representation and understand the different binary codes.
2. Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.
3. Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method.
4. Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder
5. Understand Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder.
6. Analyze Barrel shifter and ALU
7. Understand bi-stable elements like latches, flip-flop and illustrate the excitation tables of different flip flops.
8. Analyze and apply the design procedures of small sequential circuits to build the gated latches.
9. Understand the concept of Shift Registers and implement the bidirectional and universal shift registers.
10. Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
11. Implement the Asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
12. Analyze TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out.
13. Implement Tristate TTL, ECL, CMOS families and their interfacing, Memory elements.
14. Understand Concept of Programmable logic devices like FPGA. Logic implementation using Programmable Devices.
15. Design entry: Schematic, FSM & HDL, different modeling styles in VHDL,

16. Understand Data types and objects, Dataflow, Behavioral and Structural Modeling,
17. Analyze Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits.

LIST OF EXPERIMENTS

WEEK - l	**REALIZATION OF A BOOLEAN FUNCTION**

Design and simulate the HDL code to realize three and three variable Boolean functions

WEEK-2	**DESIGN OF DECODER AND ENCODER**

Design and simulate the HDL code for the following combinational circuits
a. 3 to 8 Decoder
b. 8 to 3 Encoder (With priority and without priority)

WEEK-3	**DESIGN OF MULTIPLEXER AND DEMULTIPLEXER**

Design and simulate the HDL code for the following combinational circuits
a. Multiplexer
b. De-multiplexer

WEEK -4	**DESIGN OF CODE CONVERTERS**

Design and simulate the HDL code for the following combinational circuits
a. 4 - Bit binary to gray code converter
b. 4 - Bit gray to binary code converter
c. Comparator

WEEK -5	**FULL ADDER AND FULL SUBTRACTOR DESIGN MODELING**

Write a HDL code to describe the functions of a full Adder and full subtractor using three modeling styles

WEEK -6	**DESIGN OF 8-BIT ALU**

Design a model to implement 8-bit ALU functionality

WEEK -7	**HDL MODEL FOR FLIP FLOPS**

Write HDL codes for the flip-flops - SR, D, JK, T

WEEK -8	**DESIGN OF COUNTERS**

Write a HDL code for the following counters
a. Binary counter
b. BCD counter (Synchronous reset and asynchronous reset)

WEEK-9	**HDL CODE FOR UNIVERSAL SHIFT REGISTER**

Design and simulate the HDL code for universal shift register

WEEK-l0	**HDL CODE FOR CARRY LOOK AHEAD ADDER**
Design and simulate the HDL code for carry look ahead adder	
WEEK-l1	**HDL CODE TO DETECT A SEQUENCE**
Write a HDL code to detect the sequence 1010101 and simulate the code	
WEEK-l2	**CHESS CLOCK CONTROLLER FSM USING HDL**
Design a chess clock controller FSM using HDL and simulate the code	
WEEK-l3	**TRAFFIC LIGHT CONTROLLER USING HDL**
Design a traffic light controller using HDL and simulate the code	
WEEK-l4	**ELEVATOR DESIGN USING HDL CODE**
Write HDL code to simulate Elevator operations and simulate the code	

Text Books:

1. J Bhaskar , "VHDL Primer", 3rd edition.

Reference Books:

1. Samir Palnitkar , "Verilog HDL: "A Guide to Digital Design and Synthesis", Sun Microsystems Press, 2nd Edition, 2003.
2. T.R. Padmanabhan, B. Bala Tripura Sundari, "Design Through Verilog HDL", New Jersey, Wiley- IEEE Press, 2009. ISBN: 978-0-471-44148-9
3. Zainalabedin Navabi, "Verilog Digital System Design", TMH, 2nd Edition, 2008.
4. Peter Minns, Ian Elliott, " FSM-based Digital Design using Verilog HDL", John Wiley & Sons Ltd, 2008.

Web References:

1. https://inst.eecs.berkeley.edu/~cs150/fa06/Labs/verilog-ieee.pdf
2. http://www.asic-world.com/ www.sxecw.edu.in

SOFTWARE AND HARDWARE REQUIREMENTS FOR A BATCH OF 36 STUDENTS:

HARDWARE: Desktop Computer Systems 36 nos

SOFTWARE: Xilinx

HOD, ECE