INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad -500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE DESCRIPTOR

Course Title	**DIGITAL SYSTEM DESIGN LABORATORY**				
Course Code	AEC103				
Programme	B.Tech				
Semester	IV	ECE			
Course Type	Core				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	-	2	-	3	2
Chief Coordinator	Mr. K Sudhakar Reddy, Assistant Professor				
Course Faculty	Mrs. L Shruthi, Assistant Professor Mrs. K Swathi, Assistant Professor Mrs. Bindusree, Assistant Professor Mr. K Ravi, Assistant Professor Mr. N Nagaraju, Assistant Professor				

I. COURSE OVERVIEW:

This course gives knowledge about the design, analysis, simulation of circuits used as building blocks in Very Large Scale Integration (VLSI) devices. Students can apply the concepts learn in the lectures towards design of actual VLSI subsystem all the way from specification, modeling, synthesis and physical design. This lab provides hands-on experience on implementation of digital circuit designs using HDL language, which are required for development of various projects and research work.

II. COURSE PRE-REQUISITES:

Level	Course Code	Semester	Prerequisites	Credits
UG	AEC002	III	Digital System Design	4

III. MARKS DISTRIBUTION:

Subject	SEE Examination	CIA Examination	Total Marks
Digital System Design Laboratory	70 Marks	30 Marks	100

IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

✘	Chalk & Talk	✘	Quiz	✘	Assignments	✘	MOOCs
✔	LCD / PPT	✘	Seminars	✘	Mini Project	✔	Videos
✔	Open Ended Experiments						

V. EVALUATION METHODOLOGY:

Each laboratory will be evaluated for a total of 100 marks consisting of 30 marks for internal assessment and 70 marks for semester end lab examination. Out of 30 marks of internal assessment, continuous lab assessment will be done for 20 marks for the day to day performance and 10 marks for the final internal lab assessment.

Semester End Examination (SEE): The semester end lab examination for 70 marks shall be conducted by two examiners, one of them being Internal Examiner and the other being External Examiner, both nominated by the Principal from the panel of experts recommended by Chairman, BOS.

The emphasis on the experiments is broadly based on the following criteria:

20 %	To test the preparedness for the experiment.
20 %	To test the performance in the laboratory.
20 %	To test the calculations and graphs related to the concern experiment.
20 %	To test the results and the error analysis of the experiment.
20 %	To test the subject knowledge through viva – voce.

Continuous Internal Assessment (CIA):
CIA is conducted for a total of 30 marks (Table 1), with 20 marks for continuous lab assessment during day to day performance, 10 marks for final internal lab assessment.

Table 1: Assessment pattern for CIA

Component	**Laboratory**		**Total Marks**
Type of Assessment	Day to day performance	Final internal lab assessment	
CIA Marks	20	10	30

Continuous Internal Examination (CIE):
One CIE exam shall be conducted at the end of the 16th week of the semester. The CIE exam is conducted for 10 marks of 3 hours duration.

Preparation	**Performance**	**Calculations and Graph**	**Results and Error Analysis**	**Viva**	**Total**
2	2	2	2	2	10

VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (POs)		Strength	Proficiency assessed by
PO 1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	2	Coding and design observations
PO 2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	2	Simulation graphs
PO 4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	2	Term observations
PO 5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.	3	Design Exercises

3 = High; 2 = Medium; 1 = Low

VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSOs)		Strength	Proficiency assessed by
PSO 1	**Professional Skills:** The ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	2	Coding and design observations
PSO 2	**Problem-Solving Skills:** The ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	2	Program Coding
PSO 3	**Successful Career and Entrepreneurship:** The understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.	2	Presentation on real-world problems

3 = High; 2 = Medium; 1 = Low

VIII. COURSE OBJECTIVES (COs):

The course should enable the students to:	
I	Design of combinational circuits using Verilog Hardware Description Language.
II	Implementation of Sequential circuits using Verilog Hardware Description Language.
III	Demonstration of different case studies for Verilog HDL implementation.

IX. COURSE LEARNING OUTCOMES (CLOs):

CLO Code	CLO's	At the end of the course, the student will have the ability to	PO's Mapped	Strength of Mapping
AEC103.01	CLO 1	Knowledge and use of hardware description language (VHDL) for system modeling and simulation.	PO 1, PO 5	3
AEC103.02	CLO 2	Describe and explain the operation of fundamental digital gates.	PO 1, PO 2	2
AEC103.03	CLO 3	Minimize the Boolean expression using Boolean algebra and design it using logic gates.	PO 2	2
AEC103.04	CLO 4	Analyze the operation of medium complexity standard combinational circuits like the encoder, decoder.	PO 2, PO 4	3
AEC103.05	CLO 5	Analyze the operation of medium complexity standard combinational circuits like the multiplexer, demultiplexers.	PO 2, PO 4	3
AEC103.06	CLO 6	Analyze the operation of medium complexity standard combinational circuits like the code converters.	PO 2, PO 4	3
AEC103.07	CLO 7	Design complex digital systems at several level of abstractions; behavioral and structural, synthesis and rapid system prototyping.	PO 4	2
AEC103.08	CLO 8	Design complex digital system such as ALU.	PO 4	2
AEC103.09	CLO 9	Analyze the operation of a flip-flop and examine relevant timing diagrams.	PO 4, PO 5	2
AEC103.10	CLO 10	Analyze the operation of counters and shift registers.	PO 4	2
AEC103.11	CLO 11	Develop and simulate register-level models of hierarchical digital systems.	PO 2	2
AEC103.12	CLO 12	Design and model complex digital system.	PO 4, PO 5	2
AEC103.13	CLO 13	Consolidation of the design methodologies for combinational and sequential digital systems.	PO 4	2
AEC103.14	CLO 14	Implementation of digital systems on reconfigurable programmable logic devices (FPGA).	PO 5	3
AEC103.15	CLO 15	Analyze and synthesize digital modules and circuits for a wide application range.	PO 5	3

3 = High; 2 = Medium; 1 = Low

X. MAPPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

(CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 1	3				3										
CLO 2	2	1											3	1	
CLO 3	2	2											2		2
CLO 4		3		3											
CLO 5		3		3										2	

(CLOs)	Program Outcomes (POs)												Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CLO 6		3		3											2
CLO 7				2										3	
CLO 8				2									3		
CLO 9				2	3									2	
CLO 10				1									2		3
CLO 11		2											1		2
CLO 12				2	2								2		
CLO 13				2										2	1
CLO 14					3								2		
CLO 15					3								2		3

3 = High; 2 = Medium; 1 = Low

XI. ASSESSMENT METHODOLOGIES – DIRECT

CIE Exams	PO 1, PO 2, PO 4, PO 5	SEE Exams	PO 1, PO 2, PO 4, PO 5	Assignments	-	Seminars	-
Laboratory Practices	PO 1, PO 2, PO 4, PO 5	Student Viva	-	Mini Project	-	Certification	-

XII. ASSESSMENT METHODOLOGIES - INDIRECT

✔	Early Semester Feedback	✔	End Semester OBE Feedback
✘	Assessment of Mini Projects by Experts		

XIII. SYLLABUS

LIST OF EXPERIMENTS	
WEEK-l	**REALIZATION OF A BOOLEAN FUNCTION**
Design and simulate the HDL code to realize three and three variable Boolean functions	
WEEK-2	**DESIGN OF DECODER AND ENCODER**
Design and simulate the HDL code for the following combinational circuits a. 3 to 8 Decoder b. 8 to 3 Encoder (With priority and without priority)	
WEEK-3	**DESIGN OF MULTIPLEXER AND DEMULTIPLEXER**
Design and simulate the HDL code for the following combinational circuits a. Multiplexer	

b. De-multiplexer	
WEEK-4	**DESIGN OF CODE CONVERTERS**
Design and simulate the HDL code for the following combinational circuits a. 4 - Bit binary to gray code converter b. 4 - Bit gray to binary code converter c. Comparator	
WEEK-5	**FULL ADDER AND FULL SUBTRACTOR DESIGN MODELING**
Write a HDL code to describe the functions of a full Adder and full subtractor using three modeling styles	
WEEK-6	**DESIGN OF 8-BIT ALU**
Design a model to implement 8-bit ALU functionality	
WEEK-7	**HDL MODEL FOR FLIP FLOPS**
Write HDL codes for the flip-flops - SR, D, JK, T	
WEEK-8	**DESIGN OF COUNTERS**
Write a HDL code for the following counters a. Binary counter b. BCD counter (Synchronous reset and asynchronous reset)	
WEEK-9	**HDL CODE FOR UNIVERSAL SHIFT REGISTER**
Design and simulate the HDL code for universal shift register	
WEEK-l0	**HDL CODE FOR CARRY LOOK AHEAD ADDER**
Design and simulate the HDL code for carry look ahead adder	
WEEK-l1	**HDL CODE TO DETECT A SEQUENCE**
Write a HDL code to detect the sequence 1010101 and simulate the code	
WEEK-l2	**CHESS CLOCK CONTROLLER FSM USING HDL**
Design a chess clock controller FSM using HDL and simulate the code	

Text Books:

1. Stephen Brown, Zvonko Vranesic, Fundamentals of Digital Logic Design with VHDL, TMH, 2nd Edition, 2009.
2. Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Sun Microsystems Press, 2nd Edition, 2003.

Reference Books:

1. T.R. Padmanabhan, B. Bala Tripura Sundari, Design Through Verilog HDL, New Jersey, Wiley-IEEE Press, 2009.
2. Zainalabedin Navabi, Verilog Digital System Design, TMH, 2nd Edition, 2008.

XIV. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

Week No	Topics to be covered	Course Learning Outcomes (CLOs)	Reference
1	Design and simulate the HDL code to realize three and three variable Boolean functions.	CLO 1, CLO 2, CLO 3	T1:2.5 & 2.10
2	Design and simulate the HDL code for the following combinational circuits a. 3 to 8 Decoder b. 8 to 3 Encoder (With priority and without priority)	CLO 4	T1:6.2, 6.3, 6.6
3	Design and simulate the HDL code for the following combinational circuits a. Multiplexer b. De-multiplexer	CLO 5	T1:6.1
4	Design and simulate the HDL code for the following combinational circuits a. 4 - Bit binary to gray code converter b. 4 - Bit gray to binary code converter c. Comparator	CLO 6	T1:6.4
5	Write a HDL code to describe the functions of a full Adder and full subtractor using three modeling styles	CLO 7	T1:5.2
6	Design a model to implement 8-bit ALU functionality	CLO 8	T1:5.5
7	Write HDL codes for the flip-flops - SR, D, JK, T	CLO 9	T1:7.2-7.5
8	Write a HDL code for the following counters a. Binary counter b. BCD counter (Synchronous reset and asynchronous reset)	CLO 10	T1:7.9
9	Design and simulate the HDL code for universal shift register	CLO 10, CLO 11	T1:7.8
10	Design and simulate the HDL code for carry look ahead adder	CLO 13	T1:5.4
11	Write a HDL code to detect the sequence 1010101 and simulate the code	CLO 12, CLO 13	T1:8.1
12	Design a chess clock controller FSM using HDL and simulate the code	CLO 15	T1:8.4

XV. GAPS IN THE SYLLABUS - TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

S No	Description	Proposed actions	Relevance with POs	Relevance with PSOs
1	Design of different FSM circuits	Guest Lectures	PO 4	PSO 3
2	Design of advanced digital circuits.	Seminars / NPTEL	PO 5	PSO 3

Prepared by:
Mr. K Sudhakar Reddy, Assistant Professor

HOD, ECE