

# VLSI DESIGN LABORATORY

## VII Semester . ECE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
AEC112	Core	L	T	P	C	CIA	SEE	Total
		-	-	3	2	30	70	100
<b>Contact Classes : Nil</b>	<b>Total Tutorials : Nil</b>	<b>Total Practical Classes : 36</b>				<b>Total Classes : 36</b>		

## OBJECTIVES:

- I. Understand the basic concepts about MOS device and inverter characteristics
- II. Understand the fabrication steps of IC design and design flow of VLSI circuits
- III. Design the stick diagram and layout of a circuit
- IV. Design the different MOSFET amplifier circuits

**COURSE LEARNING OUTCOME:**

1. Understand fundamentals of MOS devices and its V-I characteristics.
2. Analyze the effect of parasitic elements on MOS device, effect of threshold voltage MOSFET.
3. Understand the importance and effect of scaling on MOS devices; analyze the latest trends in CMOS technology.
4. Understand the basic CMOS nano technology and the importance of it.
5. Understand the fabrications steps involved in the MOS transistor.
6. Study various inverter characteristics of NMOS, CMOS.
7. Understand the effect of delay, noise margin and power dissipation of MOS devices.
8. Understand implementation of logic designs using MOS transistors series & parallel circuits.
9. Study other logic families like pass transistor logic, Bi-CMOS logic and various pull-up networks.
10. Understand to implement layers using stick diagram along with the color representation.
11. Study the design rules of transistors, wires, contacts and layouts with respect to width, length and spacing based on type of technology.
12. Understand effects on VLSI Interconnects and electron migration.
13. Study the latch up problems and reliability issues of CMOS.
14. Understand various gate level designs for the logics and study about Fan-In and Fan-out.
15. Analyze the effect of various capacitances of MOS devices on propagation delay and study about the reduction of RC values based on the choice of layers in the MOS devices.
16. Understand the implementation strategies of VLSI design.
17. Understand the design of programmable logic devices and analyze the speed and area tradeoffs.
18. Understand data path subsystem designs, array subsystem designs
19. Understand the operation of various static and dynamic latches and registers.
20. Analyze the timing issues and the clock strategies of VLSI designs.
21. Understand the purpose and operation of Low power memory Circuits.
22. Study various Synchronous and asynchronous circuit design; understand the operation of static and dynamic latches and registers.

<b>LIST OF EXPERIMENTS</b>	
<b>Week-1</b>	<b>MOSFET</b>
To plot the (i) output characteristics (ii) Transfer characteristics of an n-channel and p-channel MOSFET.	
<b>Week-2</b>	<b>CMOS INVERTER</b>
To design and plot the static (VTC) and dynamic characteristics of a digital CMOS inverter.	
<b>Week-3</b>	<b>RING OSCILLATOR</b>
To design and plot the output characteristics of a 3-inverter ring oscillator.	
<b>Week-4</b>	<b>LOGIC GATES</b>
To design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS technology.	
<b>Week-5</b>	<b>4X1 MULTIPLEXER</b>
To design and plot the characteristics of a 4x1 digital multiplexer using pass transistor logic.	
<b>Week-6</b>	<b>LATCHES</b>
To design and plot the characteristics of a positive and negative latch based on multiplexers.	
<b>Week-7</b>	<b>REGISTERS</b>
To design and plot the characteristics of a master-slave positive and negative edge triggered registers based on multiplexers.	
<b>Week-8</b>	<b>DIFFERENTIAL AMPLIFIER</b>
Design and simulation of a simple 5 transistor differential amplifier. Measure gain, ICMR, and CMRR.	
<b>Week-9</b>	<b>NMOS INVERTER AND CMOS INVERTER</b>
To design layout of NMOS and CMOS inverter.	
<b>Week-10</b>	<b>LAYOUT OF 2-INPUT NAND, NOR GATES</b>
To design the layout of 2-input NAND, NOR gates.	
<b>Week-11</b>	<b>COMMON SOURCE AMPLIFIER</b>
Analysis of Frequency response of Common source amplifiers.	
<b>Week-12</b>	<b>COMMON DRAIN AMPLIFIER</b>
Analysis of Frequency response of Common drain amplifiers.	
<b>Week-13</b>	<b>SINGLE STAGE CASCODE AMPLIFIER</b>
Design and Simulation of Single Stage Cascode Amplifier.	

<b>Week-14</b>	<b>BASIC CURRENT MIRROR, CASCODE CURRENT MIRROR AMPLIFIER</b>
Design and Simulation of Basic Current Mirror, Cascode Current Mirror Amplifier.	
<b>Reference Books</b>	
1. Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw Hill Publications, 2002. 2. Allen Holberg, CMOS Analog Circuit Design, Oxford Publications, 2002. 3. Baker, Li, Boyce, CMOS Mixed Circuit Design, Wiley Publications, 2002.	
<p style="text-align: center;"><b>SOFTWARE AND HARDWARE REQUIREMENTS FOR 36 STUDENTS</b></p> <p><b>HARDWARE .</b> Desktop Computer Systems 36 nos</p> <p><b>SOFTWARE .</b> Cadence tools</p>	