INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

TUTORIAL QUESTION BANK

Course Title	**VERILOG HDL**				
Course Code	AEC807				
Programme	B.Tech				
Semester	VII	ECE			
Course Type	Skill				
Regulation	R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Practicals**	**Credits**
	-	-	-	-	-
Chief Coordinator	Dr. Vijay Vallabhuni, Professor, Department of ECE				
Course Faculty	Dr. Vijay Vallabhuni, Professor, Department of ECE				

COURSE OBJECTIVES:

The course should enable the students to:	
I	Describe Verilog hardware description languages (HDL)
II	Write Register Transfer Level (RTL) models of digital circuits
III	Synthesize RTL models to standard cell libraries and FPGAs
IV	Implement RTL models on FPGAs and testing & verification

QUESTION BANK

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
UNIT-I INTRODUCTION TO VERILOG HDL				
PART-A (SHORT ANSWER QUESTIONS)				
1	Define verilog HDL?	Remember	CO 1	
2	List levels of design description in verilog HDL?	Remember	CO 1	
3	Describe is concurrency?	Remember	CO 1	
4	What is simulation and synthesis?	Remember	CO 1	
5	What is functional verification?	Remember	CO 1	
6	What are system tasks?	Remember	CO 1	
7	Write short notes on programming language interface (PLI).	Remember	CO 1	
8	What is module?	Remember	CO 1	
9	What is a simulation and synthesis tool?	Understand	CO 1	
10	What is test bench?	Remember	CO 1	
11	Define keywords and identifiers?	Remember	CO 1	
12	What are white space characters?	Remember	CO 1	
13	Define comments and numbers?	Understand	CO 1	
14	Define strings and logic values?	Remember	CO 1	
15	What is a data types? And what are those?	Understand	CO 1	
16	Define scalars and vectors?	Remember	CO 1	
17	Define parameters and memory operators?	Remember	CO 1	
18	Define system tasks?	Understand	CO 1	
19	What is the acronym of Verilog?	Remember	CO 1	
20	Define synthesis?	Understand	CO 1	
PART-B (LONG ANSWER QUESTIONS)				
1	Write short note on “Verilog as HDL”	Understand	CO 1	
2	Discuss Level of design description.	Remember	CO 1	
3	Explain top-down design methodology with example.	Understand	CO 1	
4	Write short notes on, a. Concurrency b. Functional verification	Remember	CO 1	
5	Define the following terms relevant to Verilog HDL, (a). Simulation versus synthesis. (b). PLI (c). System tasks.	Understand	CO 1	
6	What are the system tasks available in Verilog for making and controlling simulation?	Remember	CO 1	
7	Explain about, (a). Display tasks (b). Strobe tasks (c). Monitor tasks with examples.	Understand	CO 1	
8	Define the following terms relevant to Verilog HDL. (a). Module (b). Test bench.	Understand	CO 1	
9	Write a syntax functions and tasks with one example.	Remember	CO 1	
10	Write about $readmemb with example.	Remember	CO 1	
11	Write value change dump file.	Remember	CO 1	
12	Explain the synthesis procedure in Verilog HDL.	Understand	CO 1	
13	Give the surfaces for Verilog module and explain gate instantiations with examples.	Understand	CO 1	

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14	Explain assertion verification.	Remember	CO 1	
15	Design a JK flip flop using NAND gates.	Remember	CO 1	
16	Write a Verilog code for JK flip flop using NAND gates.	Remember	CO 1	
17	Explain the design approach of a master slave flip-flop with gate primitives. (OR) Design a master slave JK flip-flop using NAND gates.	Understand	CO 1	
18	Write a Verilog code for master slave JK flip flop using NAND gates.	Understand	CO 1	
19	Design a T flip flop using NAND gates.	Remember	CO 1	
20	Write a Verilog code for T flip flop using NAND gates.	Remember	CO 1	
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)				
1	Using examples, explain about concurrent and procedural statement with syntaxes.	Apply	CO 1	
2	Explain port declaration with an example using Verilog code.	Apply	CO 1	
3	Explain the components of a Verilog module with block diagram.	Apply	CO 1	
4	Define the following terms relevant to Verilog HDL construct and convention. (a). Identifiers (b). Strings (c). Data types.	Apply	CO 1	
5	Define the following terms relevant to Verilog HDL constructs and conventions. (a). Keywords (b). Strengths (c). Parameters.	Apply	CO 1	
6	Explain about number system used in Verilog.	Apply	CO 1	
7	Define the following terms relevant to Verilog HDL construct and conventions. (a). Comments, (b). Scalars and vectors.	Apply	CO 1	
8	Write about and differences scalars vectors in Verilog module with examples.	Apply	CO 1	
9	Using examples, explain about concurrent and procedural statement with syntaxes.	Apply	CO 1	
10	Explain port declaration with an example using Verilog code.	Apply	CO 1	
UNIT-II GATE LEVEL MODELING				
PART-A(SHORT ANSWER QUESTIONS)				
1	What is gate level modeling?	Remember	CO 2	
2	What is AND gate primitive?	Remember	CO 2	
3	What is module structure? Give the example of module structure.	Remember	CO 2	
4	Define tri-state gate?	Remember	CO 2	
5	What is array of instances of primitives?	Understand	CO 2	
6	Define delay?	Remember	CO 2	
7	Define strengths and content resolution?	Understand	CO 2	
8	What is a net data type?	Apply	CO 2	
9	How many types of net data types?	Understand	CO 2	
10	How many tri-state gates are there in verilog?	Understand	CO 2	
11	What is continuous assignment structure?	Remember	CO 2	

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
12	What is assignment to vectors?	Understand	CO 2	
13	Define operators in verilog?	Apply	CO 2	
14	What is Place and route?	Understand	CO 2	
15	What is an entity in Verilog programming?	Understand	CO 2	
16	What is timing verification?	Remember	CO 2	
17	What is compillation?	Understand	CO 2	
18	What is the syntax of architecture?	Apply	CO 2	
19	What is the syntax of signal declaration?	Understand	CO 2	
20	How to delete component in Verilog programming?	Understand	CO 2	
PART-B (LONG ANSWER QUESTIONS)				
1	Explain in brief built-in primitive gates that are available in Verilog HDL.	Understand	CO 2	
2	Explain NAND gate primitive with Verilog module.	Understand	CO 2	
3	Explain NOR gate primitive with Verilog module.	Understand	CO 2	
4	Design a module for addition of 16 bit words.	Understand	CO 2	
5	Write Verilog module for addition 16 bit words.	Understand	CO 2	
6	What is a three-state gate and explain each type of three-state gate with truth tables?	Understand	CO 2	
7	Write a Verilog code for tri-state devices.	Understand	CO 2	
8	Write Verilog HDL source code for a gate level description of 4 to 1 multiplexer circuit. Draw the relevant logic diagram.	Understand	CO 2	
9	Implement Verilog HDL source code and draw the logic diagram of a 2-to-4 decoder circuit. Give the gate level description.	Understand	CO 2	
10	Design module and a test bench for a half-adder.	Understand	CO 2	
11	Design module and a test bench for a 4 to 1 multiples module.	Understand	CO 2	
12	Explain simple latch with Verilog module.	Understand	CO 2	
13	Design a RS-flip with NAND gates.	Understand	CO 2	
14	Write a Verilog code for RS flip-flop with NAND gates.	Understand	CO 2	
15	Explain clocked RS flip-flop Verilog module and test bench.	Understand	CO 2	
16	Design a D-Flip-flop with gate primitives and write its Verilog code.	Understand	CO 2	
17	Design a D flip flop using NAND gates.	Understand	CO 2	
18	Write a Verilog code for D flip flop using NAND gates.	Understand	CO 2	
19	Classify delays and explain.	Understand	CO 2	
20	Explain inertial and intra-assignment delays in Verilog.	Understand	CO 2	
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)				
1	Write a Verilog HDL code for n-bit right-to-left shift register using data flow level.	Apply	CO 2	
2	Give the list of operations in data flow level and give one example for each one. OR Write short notes for the following with examples. (a). Unary operators (b). Binary operators (c). Arithmetic operators (d). Logical operators.	Apply	CO 2	
3	Explain about operator priority with examples.	Apply	CO 2	
4	Explain bit widths of expressions.	Apply	CO 2	

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
5	Design a Verilog module for a 4 to 1 vector multiplexer or module at data flow level.	Apply	CO 2	
6	Give the block diagram of one digit BCD adder and write its Verilog HDL code. OR Design a Verilog module for a BCD adder module at the data flow level.	Apply	CO 2	
7	Write a data flow model for a 9-bit parity generator circuit. Use only two assignment statements. Specify rise and fall delays as well.	Apply	CO 2	
8	Explain NMOS enhancement with conditions.	Apply	CO 2	
9	Design a Verilog module of a 4-bit bus switcher at the data flow level.	Apply	CO 2	
10	Design Verilog module of an edge triggered flip-flop built with the latch at the data flow level.	Apply	CO 2	
UNIT-III BEHAVIORAL MODELING				
PART-A (SHORT ANSWER QUESTIONS)				
1	What is behavioral modeling?	Remember	CO 3	
2	What are operations and assignments?	Remember	CO 3	
3	Define functional Bifurcation.	Remember	CO 3	
4	Define initial construct.	Remember	CO 3	
5	Define always construct.	Understand	CO 3	
6	Explain assignments with delays	Understand	CO 3	
7	Define wait construct	Remember	CO 3	
8	Explain multiple always blocks	Remember	CO 3	
9	Define blocking and non-blocking assignments	Understand	CO 3	
10	Explain the case statement	Remember	CO 3	
11	Draw a simulation flow chart	Remember	CO 3	
12	Explain if and if-else construct	Remember	CO 3	
13	Explain assign and de-assign construct.	Remember	CO 3	
14	Define repeat construct	Understand	CO 3	
15	Write the syntax for a for loop	Understand	CO 3	
16	Write the syntax for a while loop and forever loop	Remember	CO 3	
17	Explain parallel blocks	Remember	CO 3	
18	Explain force – release construct	Understand	CO 3	
19	What is the difference between signal and wire?	Understand	CO 3	
20	What are the features of VERILOG?	Remember	CO 3	
PART-B (LONG ANSWER QUESTIONS)				
1	Write a short note on, (a). Functional bifurcation (b). Intra-assignment delays.	Understand	CO 3	
2	Write the differences between begin-end and fork-blocks with examples.	Analyze	CO 3	
3	Design up counter coding procedural assignment.	Apply	CO 3	
4	Write up counter test bench, simulation results.	Analyze	CO 3	
5	Write the syntax for the following constructs and give one example for each relevant to behavioral Verilog HDL modeling. (a). initial construct, (b). always construct (c). wait construct.	Understand	CO 3	

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
6	What is the difference between an intra- statement delay and an inter- statement delay? explain using an example.	Apply	CO 3	
7	Write short notes on the following with examples, (a). Intra-assignment delays (b). Delay assignments (c). Zero delay.	Analyze	CO 3	
8	What are the advantages of multiple always blocks? Explain with example.	Analyze	CO 3	
9	Write a Verilog module for a rudimentary serial transmitter module.	Analyze	CO 3	
10	Explain multiple always blocks.	Analyze	CO 3	
11	Write a model using the behavioral modeling style to describe the behavior of a JK flip- flop using an always statement.	Apply	CO 3	
12	Design Verilog module to identify the highest priority interrupts. Write test bench simulation results of above questions with explanation	Analyze	CO 3	
13	Design module to convert angels in radians to one in degrees. Write Verilog code above question with explanation.	Analyze	CO 3	
14	Explain blocking and non-blocking statement with examples.	Analyze	CO 3	
15	Write a Verilog HDL code for n-bit shift register with an enable input using blocking assignments.	Analyze	CO 3	
16	Draw the flowchart for the simulation flow. OR Explain flowchart for the simulation flow.	Apply	CO 3	
17	Write Verilog code using case statement for any one example.	Analyze	CO 3	
18	Write the syntax for the following constructs and give one example for each relevant to behavioral Verilog HDL modeling. (a). The case statement (b). If and if-else constructs.	Analyze	CO 3	
19	Write notes on gate delays with necessary instantiations.	Analyze	CO 3	
20	Explain delays with tristate gates.	Analyze	CO 3	
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)				
1	Write the syntax for the following constructs and give one example for each relevant to behavioral Verilog HDL modeling. (a). assign-deassign construct (b). repeat construct for loop.	Apply	CO 3	
2	Write the syntax for the following constructs and give one example for each relevant to behavioural Verilog HDL modeling. (a). The disable construct (b). While loop (c). force-release construct.	Apply	CO 3	
3	Explain about forever loop.	Apply	CO 3	
4	Define while loop, write syntax with flow chart.	Apply	CO 3	
5	What is the difference between a sequential block and a parallel block? Explain using an example.	Apply	CO 3	
6	Design Verilog code of OR gate using for and disable. Write simulation results of above question with explanation.	Apply	CO 3	
7	Write syntax for ‘for while ’loop and write a Verilog code for n bit Johnson counter.	Apply	CO 3	

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8	Explain event construct in a module.	Apply	CO 3	
9	Explain stratified event queue.	Apply	CO 3	
10	Design Verilog module event construct for a serial data receive and test bench for the same.	Apply	CO 3	
	UNIT-IV SWITCH LEVEL MODELING			
	PART-A(SHORT ANSWER QUESTIONS)			
1	Explain basic transistor switches.	Remember	CO 4	
2	Define basic switch primitive.	Remember	CO 4	
3	Explain the operation of nmos switch.	Understand	CO 4	
4	Explain the operation of pmos switch.	Understand	CO 4	
5	Define resistive switches.	Remember	CO 4	
6	Define cmos switch.	Remember	CO 4	
7	Explain Bi-Directional gates.	Understand	CO 4	
8	How to insatiate with strength and delays.	Understand	CO 4	
9	Define system task.	Remember	CO 4	
10	Define parameter.	Remember	CO 4	
11	Explain parameter declaration and assignments.	Remember	CO 4	
12	Define module paths.	Understand	CO 4	
13	Define specify block.	Understand	CO 4	
14	Define system function.	Remember	CO 4	
15	Explain $display Task.	Remember	CO 4	
16	Explain file based tasks and functions.	Understand	CO 4	
17	Explain compiler directives.	Understand	CO 4	
18	Define hierarchical access.	Remember	CO 4	
19	Draw and explain the design flow of verilog?	Remember	CO 4	
20	Explain the program structure of verilog?	Understand	CO 4	
	PART-B (LONG ANSWER QUESTIONS)			
1	Design half subtractor using CMOS switches.	Understand	CO 4	
2	Write the Verilog code for half subtractor using CMOS switches.	Remember	CO 4	
3	Design code, test bench, results for CMOS switch with a single control line.	Understand	CO 4	
4	Design CMOS flip-flop.	Remember	CO 4	
5	Design Verilog module for CMOS flip-flop.	Understand	CO 4	
6	Explain bi-directional gates with suitable logic diagrams and give their switch level modeling	Understand	CO 4	
7	Design half -adder using CMOS switches.	Remember	CO 4	
8	Write the Verilog code for half adder using CMOS switches.	Remember	CO 4	
9	Write about basic switch primitives.	Remember	CO 4	
10	Write notes on time delays with switch primitives relevant to switch level modeling.	Understand	CO 4	
11	How strength and delays are instantiated? Explain. OR Write notes on instantiations with strength and delays relevant to switch level modeling.	Understand	CO 4	
12	Define and explain the following terms relevant to Verilog HDL, (a). Module parameters (b). File-based tasks and functions (c). Compiler directives.	Remember	CO 4	

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
13	Explain parameter declaration and assignments.	Remember	CO 4	
14	Explain type declaration for parameters.	Remember	CO 4	
15	Explain automatic (recursive) function.	Understand	CO 4	
16	Explain about module paths.	Understand	CO 4	
17	Define and explain the following terms relevant to Verilog HDL, (a). Hierarchical access (b). Path delays.	Remember	CO 4	
18	Explain $ finish task with example.	Remember	CO 4	
19	Explain $ random function with example.	Remember	CO 4	
20	Explain asymmetric sequence generator with example.	Understand	CO 4	
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)				
1	Explain automatic (re-entrant) tasks with example.	Remember	CO 4	
2	Explain and design Verilog module of timing related parameter with example.	Remember	CO 4	
3	Explain edge sensitive path using an example.	Understand	CO 4	
4	Explain overriding parameters.	Understand	CO 4	
5	Design Verilog module for left/right shifter.	Remember	CO 4	
6	Design Verilog module using path delay.	Understand	CO 4	
7	(a) Design Verilog module use of specify block to specify out rise end full time separation for spin delays. (b)Write test bench and simulation for the above.	Remember	CO 4	
8	Design the use of group delay with an ALU module. Write test bench and simulation results for the above.	Remember	CO 4	
9	What do you mean by User Defined Primitives (UDP) and explain the types with examples	Remember	CO 4	
10	Give the syntax for function and write a program for 16-to-1 multiplexer using function.	Remember	CO 4	
UNIT-V SEQUENTIAL CIRCUIT DESCRIPTION				
PART-A(SHORT ANSWER QUESTIONS)				
1	What are the types of sequential models?	Understand	CO 5	
2	Explain Feedback model.	Understand	CO 5	
3	Explain capacitive model.	Understand	CO 5	
4	Explain implicit model.	Remember	CO 5	
5	What are the basic memory components?	Remember	CO 5	
6	Explain functional register.	Understand	CO 5	
7	Define state machine coding.	Remember	CO 5	
8	How do you explain sequential synthesis?	Understand	CO 5	
9	What is test bench?	Understand	CO 5	
10	How to test a combinational circuit.	Remember	CO 5	
11	What is sequential circuit testing?	Remember	CO 5	
12	Explain test bench techniques.	Understand	CO 5	
13	Define design verification.	Understand	CO 5	
14	Write about types and constants in VERILOG programming.	Remember	CO 5	
15	Write about structural style of VERILOG programming.	Remember	CO 5	
16	Write about behavioural style of VERILOG programming.	Understand	CO 5	
17	Write about dataflow style of VERILOG programming.	Understand	CO 5	
18	Write about mixed style of VERILOG programming.	Remember	CO 5	

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19	Write about primary differences between the various programming styles of VERILOG language.	Remember	CO 5	
20	Write about primary differences between the dataflow style and behavioural style of VERILOG language.	Understand	CO 5	
PART-B (LONG ANSWER QUESTIONS)				
1	Classify and explain strength and contention resolution.	Remember	CO 5	
2	Design module to illustrate use if the wand-type net and test bench with stimulation results.	Remember	CO 5	
3	Draw the half adder circuits in terms of EX-OR and AND gates. Prepare the half adder module and test bench in terms of and AND gate primitives.	Understand	CO 5	
4	Design a module and test bench for a full-adder.	Apply	CO 5	
5	Design a 4 X 4 multiplier circuit and write its Verilog HDL code.	Remember	CO 5	
6	Write a Verilog HDL code for ripple-carry adder using generic specification?	Understand	CO 5	
7	Design a 4 bit full adder using gate level primitives and write its HDL code.	Understand	CO 5	
8	Design a 1to 4 demultiplexer module by using 2 to 4 decoder, and white its Verilog code.	Remember	CO 5	
9	Explain continuous assignment structures with examples.	Understand	CO 5	
10	Explain about the concurrent statements in data flow level. Give one example to each one.	Remember	CO 5	
11	Explain net delay with assignment delay and effects of net delay with suitable example.	Understand	CO 5	
12	Explain combining assignment and net declarations with examples.	Remember	CO 5	
13	Develop a VERILOG code for the 4x1 multiplexer, using three state logic.	Understand	CO 5	
14	Write a VERILOG code for a 4 bit adder and briefly explain it. Use component declaration for the program.	Remember	CO 5	
15	Write a VERILOG program to model a 4 bit comparator and explain the same briefly.	Understand	CO 5	
16	Model 8:3 encoder using VERILOG and explain the same briefly.	Remember	CO 5	
17	Write a VERILOG code to implement a 2:4 decoder with an active low enable line using, i) conditional signal assignment. ii) Selected signal assignment statement. Use '&' operator as required.	Understand	CO 5	
18	Model a 3-8 decoder with enable input using verilog.	Remember	CO 5	
19	Using VERILOG process, model the JK flip flop having set and reset pins.	Understand	CO 5	
20	Write a VERILOG code for a 4 bit ripple counter, built using D flip-flops.	Remember	CO 5	
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)				
1.	Write a Verilog module for PLA.	Remember	CO 5	
2.	What is functional register? Write and explain the Verilog module for basic shift register?	Understand	CO 5	
3.	Design and explain the Verilog module for universal shift register.	Understand	CO 5	
4.	Explain about shift register that uses separates combinational and sequential blocks. Also write a Verilog code for the same.	Understand	CO 5	

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5.	Write a Verilog code for 4-binary up-down counter.	Understand	CO 5	
6.	Write a short notes on gray-code counter. Also design a Verilog module for the same.	Understand	CO 5	
7.	Explain about LFSR and design its Verilog module in structural model.	Understand	CO 5	
8.	Explain MISR with the help of a neat sketch and also write the Verilog code for the same.	Understand	CO 5	
9.	Explain about FIFO Queue with the help of block diagram.	Understand	CO 5	
10.	Write a Verilog module for PLA.	Remember	CO 5	

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