INSTITUTE OF AERONAUTICAL ENGINEERING
(Autonomous)
Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

TUTORIAL QUESTION BANK

Course Title	DIGITAL SYSTEM DESIGN				
Course Code	AECB07				
Programme	B.Tech				
Semester	III	ECE			
Course Type	Core				
Regulation	R18				
Course Structure	**Theory**			**Practical**	
	Lectures	Tutorials	Credits	Practicals	Credits
	3	1	4	-	-
Chief Coordinator	Dr. V Vijay, Associate Professor				
Course Faculty	Dr. P Munaswamy, Professor Dr. Lalit Kumar Kaul, Professor				

COURSE OBJECTIVES:

The course should enable the students to:	
I	Understand common forms of number representation in logic circuits.
II	Learn basic techniques for the design of digital circuits and fundamental concepts used in the design of digital systems.
III	Understand the concepts of combinational logic circuits and sequential circuits.
IV	Understand the Realization of Logic Gates Using Diodes & Transistors.

COURSE OUTCOMES (COs):

CO 1	Understand the logic simplification and combinational logic design.
CO 2	Explore the MSI devices like Comparators, Multiplexers, Encoder, Decoder, Driver & Multiplexed Display, Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder, Barrel shifter and ALU
CO 3	Understand the building blocks like FF, Ripple and Synchronous counters, Shift registers, Finite state machines, Design of synchronous FSM, Algorithmic State Machines charts

CO 4	Understand the Logic Families And Semiconductor Memories
CO 5	Explore the VHDL Design entry and Modeling, Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits

COURSE LEARNING OUTCOMES (CLOs):

CLO 1	Understand number systems, binary addition and subtraction, 2's complement Representation and operations with this representation and understand the different binary codes.
CLO 2	Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.
CLO 3	Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method.
CLO 4	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder
CLO 5	Understand Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder.
CLO 6	Analyze Barrel shifter and ALU
CLO 7	Understand bi-stable elements like latches, flip-flop and illustrate the excitation tables of different flip flops.
CLO 8	Analyze and apply the design procedures of small sequential circuits to build the gated latches.
CLO 9	Understand the concept of Shift Registers and implement the bidirectional and universal shift registers.
CLO 10	Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
CLO 11	Implement the Asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
CLO 12	Analyze TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out.
CLO 13	Implement Tristate TTL, ECL, CMOS families and their interfacing, Memory elements,
CLO 14	Understand Concept of Programmable logic devices like FPGA. Logic implementation using Programmable Devices.
CLO 15	Design entry: Schematic, FSM & HDL, different modeling styles in VHDL,
CLO 16	Understand Data types and objects, Dataflow, Behavioral and Structural Modeling,
CLO 17	Analyze Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits.

TUTORIAL QUESTION BANK

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
**UNIT-I** **LOGIC SIMPLIFICATION AND COMBINATIONAL LOGIC DESIGN**			
**PART-A (SHORT ANSWER QUESTIONS)**			
1	Write short notes on binary number systems.	Remember	CO 1	AECB07.01
2	Discuss 1's and 2's complement methods of subtraction.	Remember	CO 1	AECB07.01
3	Discuss octal number system.	Remember	CO 1	AECB07.01
4	Convert the octal numbers into binary numbers $(47.5)8$, $(32.3)8$.	Remember	CO 1	AECB07.01
5	Show an example to convert gray code to binary code.	Remember	CO 1	AECB07.01
6	Describe a short note on four bit BCD codes.	Remember	CO 1	AECB07.01
7	Illustrate about unit–distance code? State where they are used.	Remember	CO 1	AECB07.02
8	State error correcting codes.	Remember	CO 1	AECB07.01
9	Convert 10101101.0111 to octal equivalent and hexadecimal equivalent.	Understand	CO 1	AECB07.01
10	State about logic design and what do you mean by positive logic system.	Remember	CO 1	AECB07.01
11	Identify Y for a given problem is $(2.3)8 + (1.7)8 = (Y)8$.	Remember	CO 1	AECB07.01
12	Explain the specialty of unit –distance code.	Remember	CO 1	AECB07.02
13	Convert $(4065)8$ into base 5.	Understand	CO 1	AECB07.01
14	Convert $(4065)8$ into base 3.	Remember	CO 1	AECB07.01
15	Convert 11001_2 into decimal?	Understand	CO 1	AECB07.01
16	Convert $(3543)8$ into base 5.	Remember	CO 1	AECB07.01
17	Convert $(277)8$ into base 3.	Remember	CO 1	AECB07.02
18	Convert 10011001_2 into decimal?	Understand	CO 1	AECB07.01
19	Convert $(2431)8$ into base 5.	Remember	CO 1	AECB07.01
20	Convert $(6254)8$ into base 3.	Understand	CO 1	AECB07.01
**PART-B (LONG ANSWER QUESTIONS)**			
1	Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend.	Understand	CO 1	AECB07.01

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
	i. 100 – 110000 ii. 11010 - 1101.			
2	a) Rewrite the decimal number $(215)10$ as an octal number b) Find $(3250 - 72532)10$ using 9's complement c) Change $(1001011101)2$ to a hexadecimal number?	Remember	CO 1	AECB07.01
3	a) Find $(3250 - 72532)10$ using 10's complement? b) Convert $(B3D9)16$ to a binary number. c) Convert $(10110101)2$ to decimal equivalent?	Understand	CO 1	AECB07.02
4	a) Convert 4510 to binary number b) Convert 0.62510 to binary number?	Remember	CO 1	AECB07.02
5	(a) Add 01100100 by 00011001. (b) Given that $(292)10 = (1204)b$ determine `b'.	Understand	CO 1	AECB07.02
6	(a) What is the gray code equivalent of the Hex Number 3A7. (b) Find 9's complement of $(25.639)10$?	Remember	CO 1	AECB07.03
7	(a) Find (72532 - 03250) using 9's complement. (b) Express each number as an octal number. a. 101001001_2 b. 1234_{16}	Understand	CO 1	AECB07.03
8	Explain Self complemented codes.	Understand	CO 1	AECB07.02
9	Convert $(4085)10$ into base-4 and obtain its 9's complement.	Remember	CO 1	AECB07.01
10	Convert the following Hexadecimal number to their Decimal equivalent $(EAF2)16$.	Remember	CO 1	AECB07.02
11	Convert $(3874)10$ into base-4 and obtain its 9's complement.	Remember	CO 1	AECB07.03
12	Convert the following Hexadecimal number to their Decimal equivalent $(DEA5)16$.	Understand	CO 1	AECB07.03
13	Convert $(7821)10$ into base-4 and obtain its 9's complement.	Understand	CO 1	AECB07.02
14	Convert the following Hexadecimal number to their Decimal equivalent $(8DAB)16$.	Remember	CO 1	AECB07.01
15	Convert $(3278)10$ into base-4 and obtain its 9's complement.	Remember	CO 1	AECB07.02

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
16	Convert the following Hexadecimal number to their Decimal equivalent (CC63)16.	Remember	CO 1	AECB07.03
17	Convert (8745)10 into base-4 and obtain its 9's complement.	Understand	CO 1	AECB07.03
18	Convert the following Hexadecimal number to their Decimal equivalent (AAC5)16.	Understand	CO 1	AECB07.02
19	Convert (6548)10 into base-4 and obtain its 9's complement.	Remember	CO 1	AECB07.01
20	Convert the following Hexadecimal number to their Decimal equivalent (EAC8)16.	Remember	CO 1	AECB07.02
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)				
1	Given the 8bit data word 01011011, generate the 12-bit composite word for the hamming code that corrects and detects single errors.	Apply	CO 1	AECB07.01
2	Express each number as an octal number. (1001010000100010)2 c. (B78)16 d. (1234)16	Apply	CO 1	AECB07.01
3	A device transmits the binary data using even parity, the message is 1011001. Identify the receiver receives the correct data or not.	Apply	CO 1	AECB07.02
4	Subtract the following binary numbers using 1's complement. i) 1011-101 ii) 10110-1011	Apply	CO 1	AECB07.02
5	Differentiate between BCD code and 2421 code and XS-3.	Apply	CO 1	AECB07.01
6	Find 7-bit hamming code for given message 1010 by using odd parity.	Apply	CO 1	AECB07.01
7	The message below coded in the seven-bit hamming code is transmitted through a noisy channel. Decode the message assuming the at most a single error occurred in each code word. 1001011,0111001,1110110	Apply	CO 1	AECB07.01
8	Generate an 11-bit hamming code for a given data 1011010 using odd parity.	Apply	CO 1	AECB07.01

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
9	Express each number as a hexadecimal number. a. $(1010101010)_2$ b. $(2526)_8$	Apply	CO 1	AECB07.02
10	a. Convert 0.35_{10} to octal number. b. Convert $9F2_{(16)}$ to its binary equivalent	Apply	CO 1	AECB07.02

UNIT-II

MSI DEVICES

PART-A(SHORT ANSWER QUESTIONS)

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
1	Define K-map.	Remember	CO 2	AECB07.04
2	Define Implicant, Prime Implicant and Essential Prime Implicant.	Remember	CO 2	AECB07.06
3	Define Consensus Theorem.	Remember	CO 2	AECB07.05
4	Solve AB+BC+CA=AB+BC.	Remember	CO 2	AECB07.04
5	Simplify the Boolean function A′BC +A′BC′ + AB′C′ + AB′C using K- map.	Understand	CO 2	AECB07.06
6	Simplify the Boolean function x′yz + x′yz′ + xy′z′ + xy′z without using K-Map.	Remember	CO 2	AECB07.04
7	Sketch and implement following logic function using k-map for given Y(A, B,C,D)= ∑m(0,1,2,3,4,7,8,9,10,11,12,14).	Understand	CO 2	AECB07.04
8	Design a logic circuit to convert BCD and gray code.	Apply	CO 2	AECB07.06
9	Design Full adder using Logic Gates.	Understand	CO 2	AECB07.04
10	Design Half subtractor using NAND Gates.	Understand	CO 2	AECB07.05
11	Simplify the Boolean function A′BCD +A′BC′D′ + AB′C′D + AB′CD′ using K- map.	Remember	CO 2	AECB07.04
12	Simplify the Boolean function A′BC D′ +A′BC′ D′ + AB′C′ D + AB′C D using K- map.	Understand	CO 2	AECB07.04
13	Simplify the Boolean function x′y + x′z′ + xy′z′ + xy′ without using K-Map.	Apply	CO 2	AECB07.06
14	Sketch and implement following logic function using k-map for given Y(A, B,C,D)= ∑m(0,1,7,8,9,10,12,14).	Understand	CO 2	AECB07.04
15	Sketch and implement following logic function using k-map for given Y(A, B,C,D)= ∑m(0,1,2,3,4,7,8,9,10).	Understand	CO 2	AECB07.05

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
16	Simplify the Boolean function A′BCD′ +A′BC′ D + AB′C′ D + ABC D′ using K- map.	Remember	CO 2	AECB07.04
17	Simplify the Boolean function x′y′z + x′yz + x′yz + x′y′z without using K-Map.	Understand	CO 2	AECB07.04
18	Sketch and implement following logic function using k-map for given Y(A, B,C,D)= ∑m(0,1,7,8,11,12,14).	Apply	CO 2	AECB07.06
19	Sketch and implement following logic function using k-map for given Y(A, B,C,D)= ∑m(0,1,2,3,7,8,11,12,14).	Understand	CO 2	AECB07.04
20	Simplify the Boolean function A′BCD′ +A′BC′D + AB′C′D′ + ABCD using K- map.	Understand	CO 2	AECB07.05
PART-B (LONG ANSWER QUESTIONS)				
1	Minimize the following function using K-map. F (A, B, C, D) = ∑m (1, 3, 5, 7, 9, 10, 11, 12, 15).	Understand	CO 2	AECB07.06
2	Minimize the following function using K-map f = ∑m (1, 2, 3, 5, 12, 13).	Understand	CO 2	AECB07.06
3	Simplify the following Boolean expressions using K-map and implement them using logic gates. (a) F (A, B, C, D)= AB'C' + AC + A'CD'. (b) F (W, X, Y, Z) = W'X'Y'Z' + WXY'Z' + W'X'YZ + WXYZ.	Understand	CO 2	AECB07.05
4	Minimize the following function using K-map. F (A, B, C, D, E) = ∑m (1,3,5,7,9,10,11,12,15,19,21,22,27) + ∑d (0,4,8).	Understand	CO 2	AECB07.04
5	Minimize the Boolean function F (w, x, y, z) = Σm (1, 3, 7, 11, 15) + Σd(0, 2, 5), obtain its POS Expression.	Understand	CO 2	AECB07.04
6	Reduce the following expression using Karnaugh map (B 'A + A'B +AB').	Understand	CO 2	AECB07.05
7	Show that AB+AB'C+BC' = AC+BC'.	Understand	CO 2	AECB07.06
8	Convert (A+B) (A+B+C)(B+C) Expression into canonical POS.	Understand	CO 2	AECB07.06
9	Expand A (A'+B) (A'+B+C') to maxterms and minterms.	Understand	CO 2	AECB07.06

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
10	Identify all the prime implicants and essential prime implicants for a given function using k-map. F(A,B,C,D)=Σm(0,1,2,5,6,7,8,9,10,13,14,15).	Understand	CO 2	AECB07.06
11	Convert (A+B+C) (A+C)(A+C) Expression into canonical POS.	Understand	CO 2	AECB07.05
12	Expand B (A+B) (A+B+C') to maxterms and minterms.	Understand	CO 2	AECB07.06
13	Identify all the prime implicants and essential prime implicants for a given function using k-map. F(A,B,C,D)=Σm(0,1,6,7,8,10,13,14,15).	Understand	CO 2	AECB07.06
14	Convert (A+C) (B+C)(A'+C) Expression into canonical POS.	Understand	CO 2	AECB07.06
15	Expand C (A'+B') (A'+C') to maxterms and minterms.	Understand	CO 2	AECB07.06
16	Identify all the prime implicants and essential prime implicants for a given function using k-map. F(A,B,C,D)=Σm(0,1,2,6,7,8,9,10,15).	Understand	CO 2	AECB07.05
17	Convert B (A+B)(B+C) Expression into canonical POS.	Understand	CO 2	AECB07.06
18	Expand A (A'+C) (A'+C') to maxterms and minterms.	Understand	CO 2	AECB07.06
19	Identify all the prime implicants and essential prime implicants for a given function using k-map. F(A,B,C,D)=Σm(0,6,7,8,10,13,14,15).	Understand	CO 2	AECB07.06
20	Convert (A'+B) (A+B'+C)(B+C) Expression into canonical POS.	Understand	CO 2	AECB07.06
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)				
1	Implement the Boolean function F = AB + CD + E using NAND gates?	Apply	CO 2	AECB07.04
2	Simplify the Boolean function F (w, x, y, z) = Σm(1, 3, 7, 11, 15) + Σd(0, 2, 5).	Apply	CO 2	AECB07.06
3	Design all logic gates using NAND.	Apply	CO 2	AECB07.04
4	Design all logic gates using NOR.	Apply	CO 2	AECB07.04
5	A function having three data inputs to implement the logic for the function F = Σm (0, 1, 2, 3, 4, 7).	Apply	CO 2	AECB07.06
6	Construct and explain the working of decimal adder.	Apply	CO 2	AECB07.04
7	Realize the Boolean expression for half subtractor.	Apply	CO 2	AECB07.05

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
8	Simplify the Boolean function F = Σm(0, 1, 2, 3, 4, 7, 9, 10, 14, 15) using tabular method.	Apply	CO 2	AECB07.05
9	Convert A.B.C+A.D expression into standard SOP form.	Apply	CO 2	AECB07.05
10	Convert (A+B+C)(B+C')(A'+C) into standard POS form.	Apply	CO 2	AECB07.06

UNIT-III
SEQUENTIAL LOGIC DESIGN

PART-A (SHORT ANSWER QUESTIONS)

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
1	Define stable state?	Remember	CO 3	AECB07.07
2	Define Flip-Flop?	Remember	CO 3	AECB07.07
3	List the applications of Flip-Flops?	Remember	CO 3	AECB07.07
4	Express your view about synchronous latch?	Remember	CO 3	AECB07.07
5	How do you build a latch using universal gates?	Understand	CO 3	AECB07.08
6	Explain about flip-flop memory characteristic?	Understand	CO 3	AECB07.08
7	Distinguish between synchronous and asynchronous latch?	Remember	CO 3	AECB07.07
8	Define clocked flip-flop?	Remember	CO 3	AECB07.08
9	Why a gated D latch is called a transparent latch?	Understand	CO 3	AECB07.08
10	List the two types of flip-flops?	Remember	CO 3	AECB07.08
11	Explain about Different types of Latches in detail	Remember	CO 3	AECB07.08
12	Explain about S-R (NOR gates) Latch?	Remember	CO 3	AECB07.09
13	Explain about S-R (NAND gates) Latch?	Remember	CO 3	AECB07.09
14	Draw The truth table of gated D-Latch?	Understand	CO 3	AECB07.08
15	Distinguish between Latch and Flip Flop?	Understand	CO 3	AECB07.07
16	Draw The truth table of gated SR-Latch?	Remember	CO 3	AECB07.09
17	Explain about J-K (NOR gates) Latch?	Remember	CO 3	AECB07.09
18	Draw The truth table of gated T-Latch?	Understand	CO 3	AECB07.08
19	Explain about J-K (NAND gates) Latch?	Understand	CO 3	AECB07.07
20	Draw The truth table of gated JK-Latch?	Remember	CO 3	AECB07.09

PART-B (LONG ANSWER QUESTIONS)

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
1	List Shift registers?	Understand	CO 3	AECB07.07
2	List the types of Shift registers.	Analyze	CO 3	AECB07.07

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
3	Explain basic difference between a shift register and counter?	Apply	CO 3	AECB07.08
4	Classify the basic types of counters?	Analyze	CO 3	AECB07.07
5	Differentiate the advantages and disadvantages of ripple counters?	Understand	CO 3	AECB07.09
6	Sketch mod 10 asynchronous counter?	Apply	CO 3	AECB07.08
7	Sketch mod 6 asynchronous counter?	Analyze	CO 3	AECB07.07
8	How does a binary counter work?	Analyze	CO 3	AECB07.08
9	Sketch mod 5 asynchronous counter?	Analyze	CO 3	AECB07.09
10	State the use of clock pulse?	Analyze	CO 3	AECB07.09
11	Sketch mod 3 asynchronous counter?	Apply	CO 3	AECB07.08
12	Sketch mod 8 asynchronous counter?	Analyze	CO 3	AECB07.07
13	Sketch mod 5 synchronous counter?	Analyze	CO 3	AECB07.08
14	Sketch mod 10 synchronous counter?	Analyze	CO 3	AECB07.09
15	Sketch mod 2 synchronous counter?	Analyze	CO 3	AECB07.09
16	Sketch mod 7 asynchronous counter?	Apply	CO 3	AECB07.08
17	Sketch mod 4 asynchronous counter?	Analyze	CO 3	AECB07.07
18	Sketch mod 4 synchronous counter?	Analyze	CO 3	AECB07.08
19	Sketch mod 2 asynchronous counter?	Analyze	CO 3	AECB07.09
20	Sketch mod 11 asynchronous counter?	Analyze	CO 3	AECB07.09
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)				
1	Explain the working principle of JK Flip-Flop in detail.	Apply	CO 3	AECB07.10
2	Define Latch. Explain about Different types of Latches in detail.	Apply	CO 3	AECB07.10
3	Differentiate combinational and sequential circuits.	Apply	CO 3	AECB07.10
4	Describe about T – Flip-flop with the help of a logic diagram and characteristic table. Derive a T-flip-flop from JK and D flip-flops.	Apply	CO 3	AECB07.11
5	Explain with the help of a block diagram, the basic components of a Sequential Circuit?	Apply	CO 3	AECB07.11
6	Explain about RS and JK flip-flops?	Apply	CO 3	AECB07.11
7	Define T – Flip-flop with the help of a logic diagram and characteristic table?	Apply	CO 3	AECB07.11

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
8	Define Latch. Explain about Different types of Latches in detail?	Apply	CO 3	AECB07.11
9	Define JK – Flip-flop with the help of a logic diagram and characteristic table?	Apply	CO 3	AECB07.10
10	List the characteristic equations for all Flip-Flops?	Apply	CO 3	AECB07.10
UNIT-IV **LOGIC FAMILIES AND SEMICONDUCTOR MEMORIES**				
PART-A(SHORT ANSWER QUESTIONS)				
1	What is negative logic?	Remember	CO 4	AECB07.12
2	What is a logic family.	Remember	CO 4	AECB07.12
3	Draw the n-channel and p-channel transistors.	Understand	CO 4	AECB07.13
4	Draw the CMOS inverter circuit.	Understand	CO 4	AECB07.12
5	What are different logic levels?	Remember	CO 4	AECB07.14
6	What are power supply rails?	Remember	CO 4	AECB07.14
7	What is Fanout?	Understand	CO 4	AECB07.14
8	What is ESD?	Understand	CO 4	AECB07.13
9	What is transition time?	Remember	CO 4	AECB07.13
10	What is high-impedance state?	Remember	CO 4	AECB07.14
11	What are PLD's?	Remember	CO 4	AECB07.14
12	Draw the general structure of PLD's.	Understand	CO 4	AECB07.14
13	Draw the 2 to 4 decoder logic symbol.	Understand	CO 4	AECB07.13
14	What are the types of PLD's?	Remember	CO 4	AECB07.13
15	What is three state buffer?	Remember	CO 4	AECB07.14
16	What is magnitude comparator?	Understand	CO 4	AECB07.14
17	Draw the full adder circuit truth table.	Understand	CO 4	AECB07.13
18	Give the comparison between PROM and PLA.	Remember	CO 4	AECB07.13
19	What is carry look ahead adder?	Remember	CO 4	AECB07.14
20	Give the comparison between PAL and PLA.	Understand	CO 4	AECB07.14
PART-B (LONG ANSWER QUESTIONS)				
1	Explain about different logic families?	Understand	CO 4	AECB07.12
2	Draw and explain TTL inverter and NAND gate.	Remember	CO 4	AECB07.12
3	Draw and explain CMOS NAND and NOR.	Understand	CO 4	AECB07.13

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
4	What would happen if three-state outputs turned on faster than they turned off?	Remember	CO 4	AECB07.13
5	Explain about Complementary metal oxide semiconductor (CMOS) ?	Understand	CO 4	AECB07.13
6	Write about the main characteristics of Logic families	Understand	CO 4	AECB07.14
7	Write about CMOS circuit's dynamic electrical behavior.	Remember	CO 4	AECB07.14
8	Explain about various CMOS logic families.	Remember	CO 4	AECB07.13
9	Draw and explain general Structure of PLD	Remember	CO 4	AECB07.12
10	Explain about emitter coupled logic.	Understand	CO 4	AECB07.13
11	Explain about TTL logic family?	Understand	CO 4	AECB07.14
12	Explain about different programmable logic devices (PLD's)	Remember	CO 4	AECB07.14
13	Compare logic families of CMOS,TTL and ECL with their specifications.	Remember	CO 4	AECB07.13
14	Explain about programmable read only memory (PROM) logic device?	Remember	CO 4	AECB07.12
15	Realize the following Boolean function using PROM 1. $f1 (x2,x1,x0) = \sum m (0,1,2,5,7)$, 2. $f2(x2,x1,x0) = \sum m(1,2,4,6)$	Understand	CO 4	AECB07.13
16	Realizing the following Boolean function using PLA 1. $f1 (x3,x2,x1,x0) = \sum m (0,1,2,5,7 ,10\ 14)$, 2. $f2(x3,x2,x1,x0) = \sum m(1,2,4,6,7,9,11,13)$	Understand	CO 4	AECB07.14
17	Realize the following Boolean function using PAL 1. $f1 (x3,x2,x1,x0) = \sum m (0,1,2,5,7 ,10\ 14)$, 2. $f2(x3, x2,x1,x0) = \sum m(1,2,4,6,7,9,11,13)$.	Remember	CO 4	AECB07.14
18	Realize the following Boolean function using PLA 1. $f1 (x3,x2,x1,x0) = {}^{\pi}M (0,1,2,5,7 ,10\ 14)$, 2. $f2(x3, x2,x1,x0) = {}^{\pi}M (1,2,4,6,7,9,11,13)$	Remember	CO 4	AECB07.13
19	Realize the following Boolean function using PAL 1. $f1 (x3,x2,x1,x0) = {}^{\pi}M (0,1,2,5,7 ,10\ 14)$, 2. $f2(x3,x2,x1,x0) = {}^{\pi}M (1,2,4,6,7,9,11,13)$	Remember	CO 4	AECB07.12
20	Realize the following Boolean function using PLD's 1. $f1 (x3,x2,x1,x0) = \sum m (1,3,5,7,9,11,13,15)$, 2. $f2(x3, x2,x1,x0) = \sum m(0,2,4,6,8,10,12,14)$	Understand	CO 4	AECB07.13
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)				
1	Give the comparison between PROM and PLA.	Remember	CO 4	AECB07.12
2	Give the classification of PLDs.and list the major differences between PLA and PAL	Remember	CO 4	AECB07.12

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
3	Realize the following Boolean function using PLD's 1. $f1\ (x2,x1,x0) = \sum m\ (1,3,5,7)$, 2. $f2(\ x2,x1,x0) = \sum m(0,2,4,6,8)$	Understand	CO 4	AECB07.12
4	Realize the CMOS NAND gate in transistor level using NOR gate circuit.	Understand	CO 4	AECB07.13
5	Explain about four modeling styles of body architecture?	Remember	CO 4	AECB07.13
6	Draw and explain CMOS Or And Invert gates.	Understand	CO 4	AECB07.14
7	Draw and explain CMOS And Or Invert gates.	Remember	CO 4	AECB07.14
8	Write a VHDL code for Multiplexer and describe the operation of Mux?	Remember	CO 4	AECB07.14
9	Write a VHDL code for Decoder and describe the operation of Decoder?	Remember	CO 4	AECB07.13
10	Explain dataflow style and behavioral style of modeling in VHDL for the expression $Y = \overline{AB} + AC$. Develop suitable VHDL code.	Remember	CO 4	AECB07.12
**UNIT-V** **VLSI DESIGN FLOW**			
**PART-A(SHORT ANSWER QUESTIONS)**			
1	What is the acronym of VHDL?	Understand	CO 5	AECB07.15
2	Define synthesis?	Understand	CO 5	AECB07.15
3	What is Place and route?	Understand	CO 5	AECB07.15
4	What is an entity in VHDL programming?	Remember	CO 5	AECB07.15
5	What is timing verification?	Remember	CO 5	AECB07.15
6	What is compilation?	Understand	CO 5	AECB07.16
7	What is the syntax of architecture?	Remember	CO 5	AECB07.16
8	What is the syntax of signal declaration?	Understand	CO 5	AECB07.16
9	How to delete component in VHDL programming?	Understand	CO 5	AECB07.16
10	What is the difference between signal and wire?	Remember	CO 5	AECB07.16
11	What are the features of VHDL?	Remember	CO 5	AECB07.16
12	Draw and explain the design flow of VHDL?	Understand	CO 5	AECB07.16
13	Explain the program structure of VHDL?	Understand	CO 5	AECB07.16
14	Write about types and constants in VHDL programming.	Remember	CO 5	AECB07.16
15	Write about structural style of VHDL programming.	Remember	CO 5	AECB07.16

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
16	Write about behavioral style of VHDL programming.	Understand	CO 5	AECB07.16
17	Write about dataflow style of VHDL programming.	Understand	CO 5	AECB07.16
18	Write about mixed style of VHDL programming.	Remember	CO 5	AECB07.16
19	Write about primary differences between the various programming styles of VHDL language.	Remember	CO 5	AECB07.16
20	Write about primary differences between the dataflow style and behavioural style of VHDL language.	Understand	CO 5	AECB07.16
PART-B (LONG ANSWER QUESTIONS)				
1	Give the VHDL code that models 4-bit up-down synchronous counter.	Remember	CO 5	AECB07.15
2	Write the VHDL code of state machine to detect the sequence "1001" on a data input then produce a logic '1' output when the sequence has been detected. Overlaps must be considered.	Remember	CO 5	AECB07.15
3	Write a VHDL code for 3-bit ripple up counter employing JK flip-flops using structural style of modeling.	Understand	CO 5	AECB07.15
4	Write a VHDL code for positive edge triggered D flip flop with active high reset asynchronous input using guarded block statement.	Apply	CO 5	AECB07.15
5	Write about libraries and packages in VHDL programming.	Remember	CO 5	AECB07.15
6	Explain static RAM memory. Write simple memory model in VHDL.	Understand	CO 5	AECB07.15
7	Write a VHDL program to generate the contents of a 256x8 rom that converts from 8-bit gray to 8-bit binary code.	Understand	CO 5	AECB07.15
8	Using VHDL process, model the SR flip flop having set and reset pins.	Remember	CO 5	AECB07.15
9	Write a VHDL code for a 4 bit ripple counter, built using JK flip-flops.	Understand	CO 5	AECB07.15
10	Give the VHDL code that models 4-bit up-down asynchronous counter.	Remember	CO 5	AECB07.16
11	With the help of case construct, write VHDL code for SM chart for binary multiplier.	Understand	CO 5	AECB07.15
12	Write the VHDL code using structural description for the 4-bit adder.	Remember	CO 5	AECB07.15
13	Develop a VHDL code for the 4x1 multiplexer, using three state logic.	Understand	CO 5	AECB07.15
14	Write a VHDL code for a 4 bit adder and briefly explain it. Use component declaration for the program.	Remember	CO 5	AECB07.16
15	Write a VHDL program to model a 4 bit comparator and explain the same briefly.	Understand	CO 5	AECB07.15

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
16	Model 8:3 encoder using VHDL and explain the same briefly.	Remember	CO 5	AECB07.15
17	Write a VHDL code to implement a 2:4 decoder with an active low enable line using, i) conditional signal assignment. ii) Selected signal assignment statement. Use '&' operator as required.	Understand	CO 5	AECB07.15
18	Model a 3-8 decoder with enable input using VHDL.	Remember	CO 5	AECB07.16
19	Using VHDL process, model the JK flip flop having set and reset pins.	Understand	CO 5	AECB07.15
20	Write a VHDL code for a 4 bit ripple counter, built using D flip-flops.	Remember	CO 5	AECB07.15
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)				
1.	Describe the following with a suitable example. i. Symbol Vs Entity ii. Configuration iii. Event Scheduling and Gaurderd block statement.	Remember	CO 5	AECB07.15
2.	Explain transport and inertial delay model in VHDL using an inverter with a delay of 20 nsecs. Develop a VHDL code for above two models. Assume delay of wire = 10 nsecs.	Understand	CO 5	AECB07.15
3.	List the three styles of modeling a digital system in VHDL. Give the VHDL code for each of them, with reference to half adder.	Understand	CO 5	AECB07.15
4.	List the seven classes of VHDL operators according to their precedence and indicate the order of evaluation of the expression, A & not B or C nor D	Understand	CO 5	AECB07.15
5.	Explain the following giving requisite statements of VHDL: i) Transport delay ii) Inertial delay.	Understand	CO 5	AECB07.16
6.	What are VHDL functions? Where do they appear? Give the complete VHDL code to find 2's complement of a N-bit number.	Understand	CO 5	AECB07.16
7.	Write a VHDL code to model the Boolean expression, $F(A,B,C) = \sum m(0,3,5,6,7)$. Using process statement.	Understand	CO 5	AECB07.16
8.	Discuss various datatypes in VHDL with examples.	Understand	CO 5	AECB07.17
9.	What is meant by variables, signals and constants in VHDL? Compare signals with variables, give an example for each.	Understand	CO 5	AECB07.17

S. No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course learning Outcome
10.	Write a VHDL code for a full subtractor using logic equation.	Remember	CO 5	AECB07.17

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