INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)

Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

TUTORIAL QUESTION BANK

Course Title	COMPUTER ORGANIZATION				
Course Code	AEC010				
Programme	B.Tech				
Semester	V	ECE			
Course Type	Core				
Regulation	IARE - R16				
Course Structure	Theory			Practical	
	Lectures	Tutorials	Credits	Laboratory	Credits
	3	1	4	-	-
Chief Coordinator	Mr. N V Krishna Rao, Assistant Professor				
Course Faculty	Mr. P Anjaiah, Assistant Professor Ms. G Nishwitha, Assistant Professor Ms. B VijayaDurga, Assistant Professor				

COURSE OBJECTIVES:

The course should enable the students to:	
I	Understand the basic structure and operation of a digital computer.
II	Understand the operation of the arithmetic unit including the algorithms &implementation of fixed-point and floating-point addition, subtraction, multiplication & division.
III	Interpret the different types of control and the concept of pipelining.
IV	To study the different ways of communicating with I/O devices and standard I/O interfaces and RISC and CISC processors.
V	To study the hierarchical memory system including cache memories and virtual memory.

COURSE OUTCOMES:

CO 1	Ability to understand the concepts of associated with the computer system design and data representation.
CO 2	Explore the concepts associated with the fixed point arithmetic operations and algorithms.
CO 3	Understand the concepts of Control design of a computer.
CO 4	Ability to learn the concepts associated with the memory organization.
CO 5	Explore the concepts of System Organization including types of interrupts and processors.

COURSE LEARNING OUTCOMES:

AEC010.01	Describe the various components like input/output units, memory unit, control unit, arithmetic logic unit connected in the basic organization of a computer.
AEC010.02	Understand the concepts associated with the computer organization.
AEC010.03	Describe various data representations and explain how arithmetic and logical operations are performed by computers.
AEC010.04	Understand instruction types, addressing modes and their formats in the assembly language programs.
AEC010.05	Describe the implementation of fixed point and floating point addition, subtraction operations.
AEC010.06	Describe the various major algorithmic techniques (Robertson algorithm, booth's algorithm, non-restoring division algorithm).
AEC010.07	Describe the pipeline processing concept with multiple functional units.
AEC010.08	Understand the concept of the modified booth's algorithm.
AEC010.09	Understand the connections among the circuits and the functionalities in the hardwired control unit.
AEC010.10	Describe the design of control unit with address sequencing and microprogramming Concepts.
AEC010.11	Describe the concepts CPU control unit, Pipeline control, instruction pipeline.
AEC010.12	Understand the functionality of super scalar processing and Nano programming.
AEC010.13	Understand the concept of memory hierarchy and different typed of memory chips.
AEC010.14	Describe the concepts of magnetic surface recording, optical memories
AEC010.15	Understand the cache and virtual memory concept in memory organization.
AEC010.16	Describe the hardware organization of associate memory and understand the read and write operations.
AEC010.17	Understand the various bus control interfaces and system control interfaces.
AEC010.18	Describe the various interrupts (Vectored Interrupts, PCI interrupts, Pipeline interrupts).
AEC010.19	Understand the functionally of RISC and CISC processors.
AEC010.20	Describe the concepts of superscalar and vector processor.

TUTORIAL QUESTION BANK

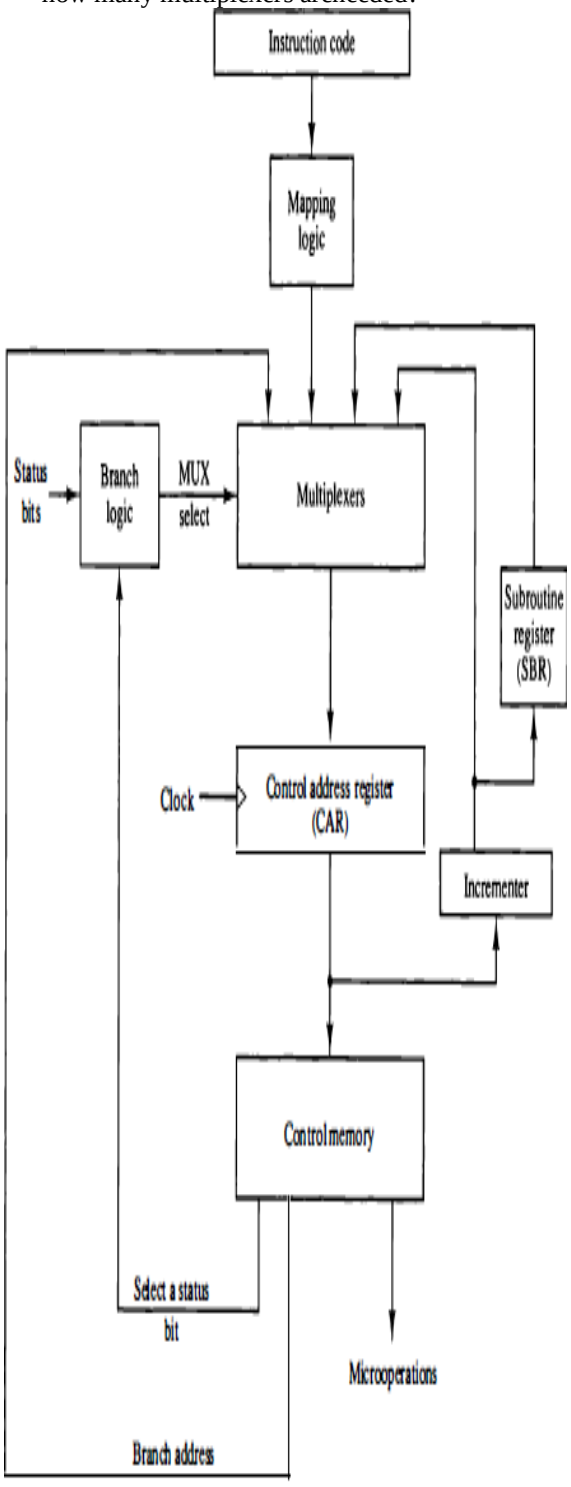
S. No.	Questions	Blooms Taxonomy Level	Course Outcomes	Course Learning Outcome
	UNIT – I			
	Group - A (Short Answer Questions)			
1	Define Computer Architecture?	Understand	CO 1	AEC010.01
2	Define Computer Organization?	Remember	CO 1	AEC010.02
3	Describe the basic functional units of a computer?	Remember	CO 1	AEC010.01
4	List out the limitations of computers?	Understand	CO 1	AEC010.02
5	Illustrate the generations of a computer?	Remember	CO 1	AEC010.02
6	Discuss about VLSI era?	Remember	CO 1	AEC010.01
7	Describe the system representation?	Remember	CO 1	AEC010.01
8	Demonstrate the register level components?	Understand	CO 1	AEC010.02
9	Demonstrate the Processor level components?	Understand	CO 1	AEC010.02
10	Show the pictorial representation of CPU organization?	Remember	CO 1	AEC010.02
11	Give some examples for fixed point representation?	Understand	CO 1	AEC010.03
12	Give some examples for floating point representation?	Understand	CO 1	AEC010.03
13	List out the instruction types?	Understand	CO 1	AEC010.03
14	Describe the instruction formats?	Understand	CO 1	AEC010.03
15	List out the types of addressing modes?	Understand	CO 1	AEC010.03
16	Write the need for different addressing modes?	Remember	CO 1	AEC010.04
17	Write short notes for Register Addressing Mode?	Understand	CO 1	AEC010.04
18	Write short notes for Direct Addressing Mode?	Understand	CO 1	AEC010.04
19	Write short notes for Indirect Addressing Mode?	Remember	CO 1	AEC010.04
20	What is software and hardware?	Understand	CO 1	AEC010.04
	Group - B (Long Answer Questions)			
1	Define about digital computer? Discuss briefly on various types of computer?	Understand	CO 1	AEC010.01
2	Explain the functional organization of a digital computer and explain the function of each element of a computer?	Remember	CO 1	AEC010.01
3	Illustrate the diagram for connection between the processor and the memory and explain basic operational concepts of computer?	Remember	CO 1	AEC010.01
4	Explain about various formats of instructions?	Understand	CO 1	AEC010.04
5	Explain the issues to be considered in accumulator based CPU with respect to programming considerations, instruction set?	Understand	CO 1	AEC010.04
6	Explain VLSI technology and describe how does it influence the design and application of both special purpose and genera purpose computers?	Remember	CO 1	AEC010.01
7	Discuss about system representation?	Understand	CO 1	AEC010.01
8	What are the different levels of system design and explain each level?	Understand	CO 1	AEC010.02
9	Explain the various Instruction types with examples.	Remember	CO 1	AEC010.03
10	Demonstrate the representation of fixed point numbers in computers?	Understand	CO 1	AEC010.03
11	Describe the register level components in system design?	Understand	CO 1	AEC010.01
12	Describe the Processor level components in system design?	Remember	CO 1	AEC010.01
13	Demonstrate the representation of floating point numbers in computers?	Understand	CO 1	AEC010.03
14	Explain different types of addressing modes with suitable examples	Understand	CO 1	AEC010.04
15	Show how can the following operation be performed using: a) three address instruction b) two address instruction c) one address instruction d) zero address instruction X = (A +B)* (C + D)	Remember	CO 1	AEC010.04

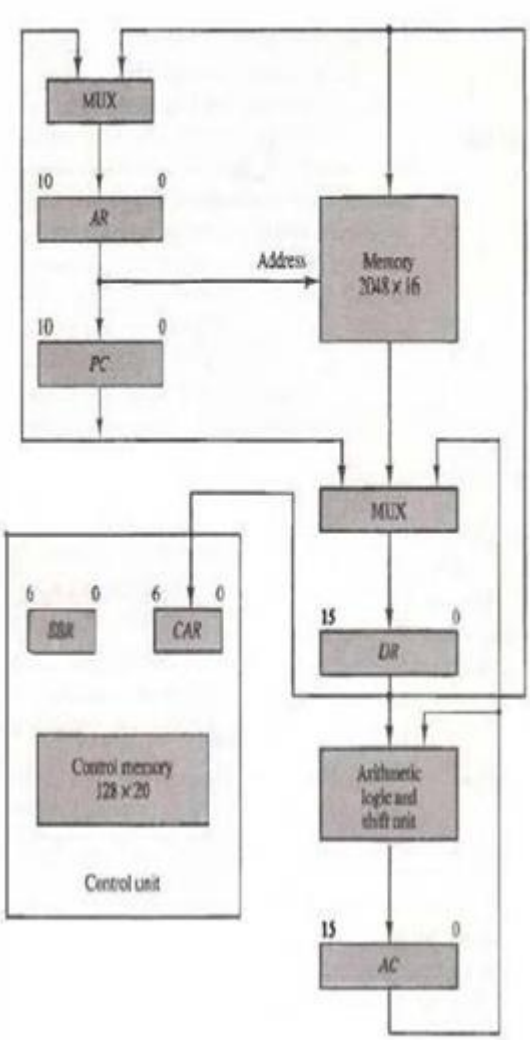
16	Compare RISC and CISC?	Understand	CO 1	AEC010.04
17	Explain i) ROM ii) PROM iii) EPROM iv) EEPROM.	Understand	CO 1	AEC010.02
18	Explain the speed up features of modern computers?	Understand	CO 1	AEC010.01
19	Explain about VLSI era?	Remember	CO 1	AEC010.01
20	Describe error correction and error detection?	Understand	CO 1	AEC010.02
Group - C (Analytical Questions)				
1	An instruction A is stored at location 300 with its adder field at 301. The adder field has value 400. A process register R1contains the number 200. Evaluate the effective address if addressing mode of instruction is 1. Direct 2. Immediate Relative	Remember	CO 1	AEC010.04
2	Calculate The amount of ROM needed to implement a 4 bit multiplier?	Remember	CO 1	AEC010.02
3	Explain the issues to be considered in accumulator based CPU with Respect to programming considerations, instruction set.	Understand	CO 1	AEC010.04
4	Explain VLSI technology and describe how does it influence the design and application of both special purpose and general purpose computers?	Understand	CO 1	AEC010.01
5	An instruction A is stored at location 300 with its adder field at 301. The adder field has value 400. A process register R1contains the number 200. Evaluate the effective address if addressing mode of instruction is 1.RegisterIndirect 2.Index with R1 as Index Reg.	Remember	CO 1	AEC010.04
6	Show how can the following operation be performed using: a) three address instruction b) two address instruction c) one address instruction zero address instruction Z = (P *Q)/ (K - M)	Understand	CO 1	AEC010.04
7	Explain about different types of memories in the primary and secondary memories with advantages and disadvantages	Remember	CO 1	AEC010.04
8	Explain the evolution of computers with diagrams in detail and write their limitations of one another.	Remember	CO 1	AEC010.04
9	Explain the block diagram of basic computer and different units in the computer system.	Remember	CO 1	AEC010.04
10	What is memory address register (MAR) and memory data register (MDR) and Describe the IEEE standard for floating point numbers for single precision number	Remember	CO 1	AEC010.04
UNIT - II				
Group - A (Short Answer Questions)				
1	State the various processing of pipeline	Remember	CO 2	AEC010.07
2	Discuss regarding parallel processing	Remember	CO 2	AEC010.07
3	Differentiate between restoring and non-restoring division algorithm	Understand	CO 2	AEC010.06
4	Write short notes on the following: CPU-IOP communication Micro program sequencer floating point arithmetic (addition and multiplication)	Understand	CO 2	AEC010.07
5	Discuss in brief about floating point arithmetic operations	Remember	CO 2	AEC010.05
6	What is pipelining?	Understand	CO 2	AEC010.07
7	What is branch penalty?	Understand	CO 2	AEC010.06
8	Define branch delay slot?	Remember	CO 2	AEC010.06
9	Define speculative execution?	Understand	CO 2	AEC010.07
10	What is a branch instruction?	Understand	CO 2	AEC010.07
11	Define underflow and overflow?	Understand	CO 2	AEC010.07
12	What is a floating point representation system?	Remember	CO 2	AEC010.05

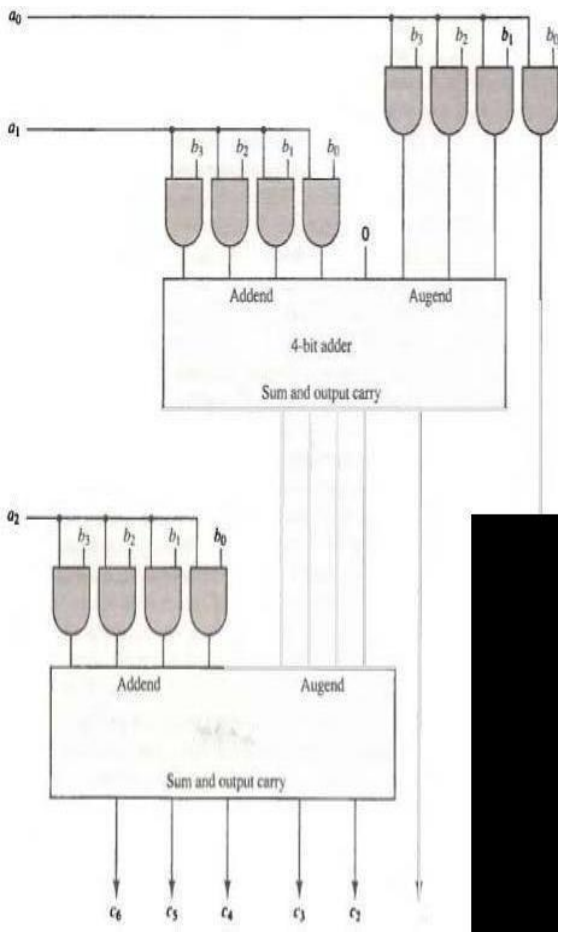
13	What is meant by multiplexer and demulplexer?	Remember	CO 2	AEC010.05
14	What is encoder and decoder ?	Remember	CO 2	AEC010.05
15	Explain the functionality of half adder with an example?	Remember	CO 2	AEC010.05
16	Define Full Adder with an example	Remember	CO 2	AEC010.05
17	What is combinational circuit and sequential circuit	Remember	CO 2	AEC010.05
18	Define Asynchronous Sequential Circuits?	Remember	CO 2	AEC010.05
19	What is Carry Look-ahead Adder?	Remember	CO 2	AEC010.05
20	What is Sequential ALU's?	Remember	CO 2	AEC010.05
Group - B (Long Answer Questions)				
1	Draw the black diagram of hardware for addition and subtraction?	Remember	CO 2	AEC010.05
2	Draw the floating point addition subtraction unit neatly and explain the operation?	Remember	CO 2	AEC010.05
3	Compare sequential ALU in terms of architecture, overhead application and latency?	Understand	CO 2	AEC010.05
4	Explain the Booths multiplication algorithm with an example	Understand	CO 2	AEC010.06
5	Derive an algorithm in flow chart form for non restoring algorithm method of fixed point binary division	Remember	CO 2	AEC010.06
6	Explain pipeline conflicts and discuss the remedies for those conflicts.	Understand	CO 2	AEC010.07
7	Illustrate the signed magnitude, signed 1's complement, and signed 2's complement for the decimal number 14.	Remember	CO 2	AEC010.05
8	Convert the following decimal numbers with the indicated bases to decimal. i. $(12121)_3$ ii. $(4310)_5$ iii. $(50)_7$	Understand	CO 2	AEC010.05
9	Calculate the subtraction with the following unsigned decimal numbers by taking the 10's complement of the subtrahend. 123900;090657:100000;000000	Understand	CO 2	AEC010.05
10	Calculate the arithmetic operations (+42) + (-13) and (-42) – (-13) in binary using signed 2's complement representation for negative numbers.	Understand	CO 2	AEC010.05
11	Calculate the arithmetic operations (+70) + (+80) and (-70) + (-80) with binary numbers in signed 2's complement representation. Use eight bits to accommodate each number together with its sign. Show that overflow Occurs in both cases.	Remember	CO 2	AEC010.05
12	Show the number (+46.5)10 as a floating-point binary number with 24 bits.	Understand	CO 2	AEC010.05
13	Explain in detail regarding the Instruction pipelining with various stages along with the pictorial representation?	Remember	CO 2	AEC010.07
14	Evacuate regarding the following Two stage pipelining Four segment CPU pipeline Six stage pipelining	Understand	CO 2	AEC010.07
15	Explain the 2's complement multiplication using Robertson's algorithm with an example	Understand	CO 2	AEC010.06
16	Illustrate Modified Booth's algorithm with an example	Remember	CO 2	AEC010.08
17	Describe the various Floating Point Formats with examples.	Understand	CO 2	AEC010.05
18	Explain algorithm for floating point addition and subtraction?	Remember	CO 2	AEC010.05
19	Use booth's algorithm to multiply -5 and 5.	Understand	CO 2	AEC010.06
20	What is Control Unit Function?	Understand	CO 2	AEC010.06
Group - C (Analytical Questions)				
1	Explain Booth's multiplication algorithm for signed 2's complement numbers in details, with a suitable example and give the hard ware requirement.	Understand	CO 2	AEC010.06

2	Discuss step by step Addition operation performance on t he following data 3.25 x 10 ** 3 + 2.63 x 10 ** -1 ----------	Understand	CO 2	AEC010.05
3	Discuss step by step Multiplication operation performance on t he following data 3.0 x 10 ** 1 + 0.5 x 10 ** 2 ----------	Understand	CO 2	AEC010.05
4	Explain how subtraction and division operation is performed in floating point arithmetic operations	Remember	CO 2	AEC010.05
5	With a help of flow chart explain the booth algorithm and show the step by step multiplication process for 15×12.	Remember	CO 2	AEC010.06
6	Show the difference between combinational and sequential circuits with an example	Remember	CO 2	AEC010.06
7	What is Multiplexer? And Define Demultiplexer?	Remember	CO 2	AEC010.06
8	With a help of flow chart explain the modified booth algorithm and show the step by step multiplication process for 16×10	Remember	CO 2	AEC010.06
9	Explain how subtraction and division operation is performed in floating point arithmetic operations with an example?	Remember	CO 2	AEC010.06
10	Design the decoder and encoder circuits with an example	Remember	CO 2	AEC010.06
UNIT - III				
Group - A (Short Answer Questions)				
1	Draw control unit organization?	Remember	CO 3	AEC010.11
2	What is a hardware control unit?	Understand	CO 3	AEC010.09
3	What is control store?	Understand	CO 3	AEC010.11
4	What is the purpose of WMFC signal?	Understand	CO 3	AEC010.09
5	What is static branch prediction?	Remember	CO 3	AEC010.09
6	What is dynamic branch prediction?	Remember	CO 3	AEC010.09
7	Draw a block diagram of control signal for register MDR?	Understand	CO 3	AEC010.09
8	What are the actions needed to execute the instruction Move R1 R2?	Remember	CO 3	AEC010.09
9	What is a hardware control unit?	Remember	CO 3	AEC010.08
10	What is micro routine?	Understand	CO 3	AEC010.10
11	What is control store?	Remember	CO 3	AEC010.10
12	Write control signals for storing a word in memory.	Understand	CO 3	AEC010.09
13	What is the necessity of grouping signals?	Understand	CO 3	AEC010.09
14	What is nano programming?	Remember	CO 3	AEC010.12
15	What is the superscalar processor?	Remember	CO 3	AEC010.12
16	What is the function of dispatch unit?	Understand	CO 3	AEC010.12
17	What is dynamic prediction?	Understand	CO 3	AEC010.12
18	Define data hazard?	Remember	CO 3	AEC010.12
19	Define structural hazard?	Understand	CO 3	AEC010.12
20	Define control hazard?	Remember	CO 3	AEC010.11
21	What is fetch instruction	Understand	CO 3	AEC010.12
22	Discuss about fetch operand?	Remember	CO 3	AEC010.11
23	Discuss about write result?	Understand	CO 3	AEC010.10
24	What do you mean by out-of order execution? Is it Desirable?	Remember	CO 3	AEC010.11
25	Define Pipeline Hazards?	Remember	CO 3	AEC010.11
26	What is a pipe stage and instruction pipeline?	Remember	CO 3	AEC010.12
	Group - B (Long Answer Questions)			
1	Explain the operation of address sequencer in a micro programmed control unit.	Remember	CO 3	AEC010.12
2	Explain micro programming with neat sketch?	Remember	CO 3	AEC010.12

3	Draw the block diagram of a complete processor?	Understand	CO 3	AEC010.10
4	Explain in detail the decoding and encoding function of hardwired control unit?	Understand	CO 3	AEC010.09
5	Compare hardwired control unit and micro programmed control unit	Remember	CO 3	AEC010.10
6	Discuss about the design of hardwired control unit for two's complement multiplier	Understand	CO 3	AEC010.09
7	What are the advantages of hardwired control unit? What are the disadvantages?	Remember	CO 3	AEC010.10
8	Describe Nano programming in detail with example?	Remember	CO 3	AEC010.12
9	Explain in detail regarding the implementation requirements of the pipeline	Understand	CO 3	AEC010.12
10	Give a detailed sketch on instruction pipeline and its operations along with a flow chart and timing diagram	Understand	CO 3	AEC010.12
11	Explain instruction pipeline conflicts and their remedies	Understand	CO 3	AEC010.12
12	Write a note about: Instruction pipeline and pipeline performance?	Remember	CO 3	AEC010.12
13	Discuss the various hazards that might arise in a pipeline. What are the remedies commonly adopted to overcome/minimize the sehazards.	Remember	CO 3	AEC010.12
14	Explain the various approaches used to deal with conditional pipelining?	Remember	CO 3	AEC010.12
15	Explain various factors that reduce the performance of the pipeline and how they can be overcome.	Remember	CO 3	AEC010.12
16	What is the relationship between instructions (assembly code) and micro operations?	Understand	CO 3	AEC010.12
17	Write a note about: superscalar processing and nano programming?	Remember	CO 3	AEC010.12
18	The stage delays in a 4-stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds. Find percentage of the throughput increase of the pipeline?	Understand	CO 3	AEC010.11
19	Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume that there are no stalls in the pipeline. Find the speed up achieved in this pipelined processor ?	Understand	CO 3	AEC010.11
20	The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write back (WB). The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards.Find the number of clock cycles required for completion of execution of the sequence of instructions ?	Understand	CO 3	AEC010.11
Group - C (Analytical Questions)				
1	The control memory in Fig. 7-2 has 4096 words of 24 bits each. 1. How many bits are there in the control addressregister? 2. How many bits are there in each of the four inputs shown going into themultiplexers?	Remember	CO 3	AEC010.10

	3. What are the number of inputs in each multiplexer and how many multiplexers areneeded?  Figure 7-2 Selection of address for control memory.			
2	Why do we need the two multiplexers in the computer hardware configuration shown in Fig. 7-4? Is there another way that information from multiple sources can be transferred to a common destination?	Remember	CO 3	AEC010.09

	 Figure 7-4 Computer hardware configuration.			
3	It Is necessary to design a pipeline for a fixed-point multiplier that multiplies two 8-blt binary integers. Each segment consists of a number of AND gates and a binary adder similar to an array multiplier as shown in following Fig. i. How many AND gates are there in the segment, and what size of adder is needed? ii. How many segments are there in the pipeline? iii. If the propagation delay in each segment is 30ns, what is the average time that takes to multiply two	Remember	CO 3	AEC010.12

	fixed-point numbers in the pipeline?  			
4	Consider the multiplication of two 40x 40 matrices using a vector processor. i. How many product terms are there in each inner product and how many inner products must be evaluated? ii. How many multiply-add operations are needed to calculate the product matrix?	Remember	CO 3	AEC010.13
5	Consider a computer with four floating-point pipeline processors. Suppose that each processor uses a cycle time of 40 ns. How long will it take to perform 400 floating - point operations? Is there a difference lf the same400operatlons is carried out using a single pipeline processor with a cycle time of 10ns?	Remember	CO 3	AEC010.13
6	Instruction execution in a processor is divided into 5 stages, Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX), and Write Back (WB). These stages take 5, 4, 20, 10 and 3 nanoseconds (ns) respectively. A pipelined implementation of the processor requires buffering between each pair of consecutive stages with a delay of 2 ns. Two pipelined implementations of the processor are contemplated: (i) a naive pipeline implementation (NP) with 5 stages and (ii) an efficient pipeline (EP) where the OF stage is divided into stages OF1 and OF2 with execution times of 12 ns and 8 ns respectively. Find the speedup (correct to two decimal places) achieved by EP over NP in executing 20 independent instructions with no hazards ?	Understand	CO 3	AEC010.11

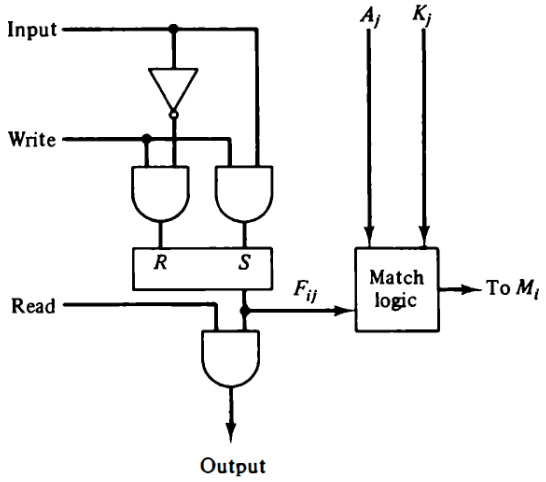
7	Consider a 3 GHz (gigahertz) processor with a three-stage pipeline and stage latencies τ_1, τ_2, τ_3 and such that $\tau_1 = 3\tau_2/4 = 2\tau_3$. If the longest pipeline stage is split into two pipeline stages of equal latency, Find the new frequency in GHz, ignoring delays in the pipeline registers.	Understand	CO 3	AEC010.11
8	An instruction pipeline has five stages, namely, instruction fetch (IF), instruction decode and register fetch (ID/RF), instruction execution (EX), memory access (MEM), and register writeback (WB) with stage latencies 1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns, respectively (ns stands for nanoseconds). To gain in terms of frequency, the designers have decided to split the ID/RF stage into three stages (ID, RF1, RF2) each of latency 2.2/3 ns. Also, the EX stage is split into two stages (EX1, EX2) each of latency 1 ns. The new design has a total of eight pipeline stages. A program has 20% branch instructions which execute in the EX stage and produce the next instruction pointer at the end of the EX stage in the old design and at the end of the EX2 stage in the new design. The IF stage stalls after fetching a branch instruction until the next instruction pointer is computed. All instructions other than the branch instruction have an average CPI of one in both the designs. The execution times of this program on the old and the new design are P and Q nanoseconds, respectively. Find the value of P/Q ?	Understand	CO 3	AEC010.11
9	Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions I_1, I_2, I_3, ..., I_{12} is executed in this pipelined processor. Instruction I_4 is the only branch instruction and its branch target is I_9. If the branch is taken during the execution of this program, Find the time (in ns) needed to complete the program ?	Understand	CO 3	AEC010.11
10	Consider a CPU where all the instructions require 7 clock cycles to complete execution. There are 140 instructions in the instruction set. It is found that 125 control signals are needed to be generated by the control unit. While designing the horizontal microprogrammed control unit, single address field format is used for branch control logic. What is the minimum size of the control word and control address register?	Understand	CO 3	AEC010.11
UNIT - IV				
Group - A (Short Answer Questions)				
1	What is magnetic surface recording?	Understand	CO 4	AEC010.13
2	How CAM is different from read / writes memory?	Understand	CO 4	AEC010.14
3	Define address space and memory space.	Understand	CO 4	AEC010.14
4	Differentiate between memory mapped I/O and isolated mapped I/O	Remember	CO 4	AEC010.14
5	Mention the types of memory?	Remember	CO 4	AEC010.14
6	What is a memory unit called as RAM?	Understand	CO 4	AEC010.14
7	What are the characteristic of semiconductor RAM memories?	Understand	CO 4	AEC010.14

8	Compare SRAMs DRAMs?	Understand	CO 4	AEC010.14
9	Give memory hierarchy?	Remember	CO 4	AEC010.14
10	What is multilevel hierarchy?	Understand	CO 4	AEC010.14
11	Define memory cycle time?	Remember	CO 4	AEC010.14
12	Define rotational latency?	Understand	CO 4	AEC010.15
13	Give the bit representation by phase encoding?	Understand	CO 4	AEC010.15
14	Define system space?	Remember	CO 4	AEC010.15
15	Define user space?	Understand	CO 4	AEC010.15
16	Write formula for calculating the average access time experienced by the processor in a system with two levels of caches?	Understand	CO 4	AEC010.15
17	Define address space and memory space.	Remember	CO 4	AEC010.15
18	Explain various types of interrupts in brief.	Understand	CO 4	AEC010.15
19	Define Read access time ?	Remember	CO4	AEC010.15
20	Define Destructive readout(DRO) ?	Remember	CO4	AEC010.15
Group - B (Long Answer Questions)				
1	What is Cache and Virtual memory in detail?	Remember	CO 4	AEC010.14
2	Draw the block diagram of an association memory and explain its operation in terms of match logic, read and write operations.	Understand	CO 4	AEC010.14
3	Explain DMA transfer in detail with all relevant block diagrams.	Understand	CO 4	AEC010.14
4	Explain the internal organization of memory chip?	Understand	CO 4	AEC010.14
5	Write short notes on : 1. Optical Memory 2. Associative Memory	Remember	CO 4	AEC010.14
6	Draw the organization of the serial access memory unit and explain its accessing mechanism?	Remember	CO 4	AEC010.14
7	Explain memory hierarchy and memory types?	Understand	CO 4	AEC010.15
8	Write notes on: 1. Virtual Memory 2. Memory Interleaving 3. Associative Memory 4. Optical Memory	Understand	CO 4	AEC010.15
9	Explain the organization of RAM in detail?	Remember	CO 4	AEC010.15
10	Explain the operation of associative cache memories?	Understand	CO 4	AEC010.15
11	Discuss the various memory types and mention its advantages?	Remember	CO 4	AEC010.15
12	Analyze the memory hierarchy in terms of speed, size and Cost ?	Remember	CO4	AEC010.15
13	Explain the Address Translation in Virtual Memory ?	Understand	CO4	AEC010.15
14	Design 64k X 16 memory chip using 16k X 8 memory chips ?	Understand	CO4	AEC010.15
15	Define Auxiliary memory? Discuss with neat diagrams?	Remember	CO4	AEC010.15
16	Compare the parameters size, speed and cost per bit in the hierarchy ?	Remember	CO4	AEC010.15
17	Compare and contrast between Asynchronous DRAM and Synchronous DRAM ?	Understand	CO4	AEC010.15
18	Draw the internal organization of a SRAM cell and explain the read and write operation.	Remember	CO4	AEC010.15
19	Explain in detail about associative mapping technique ?	Remember	CO4	AEC010.15
20	Write formula for calculating the average access time experienced by the processor in a system with two level of caches?	Understand	CO4	AEC010.15

Group - C (Analytical Questions)				
1	Criticize the following statement :"Using the faster processing chip results in a corresponding increase in the performance of computer even if the main memory speed remains the same"	Understand	CO 4	AEC010.13
2	An 8-bit computer has a 16-bit address bus. The first 15 lines of the address are used to select a bank of 32K bytes of memory. The high- order bit of the address is used to select a register which receives the contents of the data bus. Explain how this configuration can be used to extend the memory capacity of the system to eight banks of 32K bytes each, for a total of 256K bytes of memory.	Understand	CO 4	AEC010.15
3	The access time of a cache memory is 100 ns and that of main memory 1000 ns. It is estimated that 80 percent of the memory requests are for read and the remaining 20 percent for write. The hit ratio for read accesses only is 0.9. A Write-through procedure is used i) What is the average access time of the system considering only memory read cycle? ii) What is the average access time of the system for both read and write requests? iii) What is the hit ratio taking into consideration the write cycles?	Understand	CO4	AEC010.13
4	A two way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from the main memory. The main memory size is 128 K*32 i) Formulate all pertinent information required to construct the cache memory ii) What is the size of the cache memory	Remember	CO4	AEC010.13
5	Consider a main memory built with SDRAM chips. Data are transferred in burst lengths of 8. Assume that 32 bits of data are transferred in parallel. If a 400-MHz clock is used, how much time does it take to transfer: (a) 32 bytes of data (b) 64 bytes of data What is the latency in each case?	Remember	CO4	AEC010.13
6	Consider a processor running a program. 30% of the instructions of which require a memory read or write operation if the cache bit ratio is 0.95 for instructions and 0.9 for data. When a cache bit occurs for instruction or for data, only one clock is needed while the cache miss penalty is 17 clocks to read/write on the main memory. Work out the time saved by using the cache, given the total number of instructions executed is 1 million	Understand	CO4	AEC010.13
7	A computer uses RAM chips of 1024 × 1 capacity. a) How many chips are needed, and how should their address lines be connected to provide a memory capacity of 1024 bytes? b) How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus	Understand	CO4	AEC010.13
8	Using the 64Mb DRAM as basic component, design a 256Mx32bit DRAM.	Understand	CO4	AEC010.13
9	a) Draw the logic diagram of all the cells of one word in an associative memory. Include the read and write logic of Fig.	Understand	CO 4	AEC010.16

12-8 and the match logic of Fig. 12-9.

Figure 12-8 One cell of associative memory.



b) Draw the logic diagram of all cells along one vertical column (column j) in an associative memory. Include a common output line for all bits in the same column.

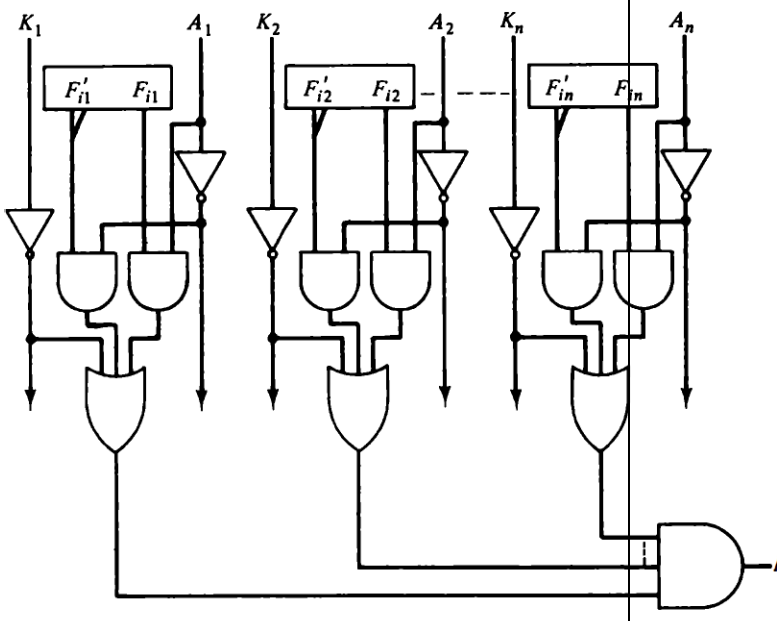


Figure 12-9 Match logic for one word of associative memory.

	c) If a page consists of 21< words, how many pages and blocks are there in the system?			
10	A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory- mapped 1/0 configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers. a) How many RAM and ROM chips are needed? b) Draw a memory-address map for the system. c) Give the address range in hexadecimal for RAM, ROM, and interface	Understand	CO 4	AEC010.13
UNIT - V				
Group - A (Short Answer Questions)				
1	Write features of RISC.	Remember	CO 5	AEC010.19
2	Write briefly about multi processor.	Understand	CO 5	AEC010.19
3	What is memory mapped I/O?	Understand	CO 5	AEC010.18
4	What is program controlled I/O?	Understand	CO 5	AEC010.18
5	What are the various mechanism for implementing i/o operation?	Remember	CO 5	AEC010.18
6	When the privilege exception arises?	Remember	CO 5	AEC010.18
7	What are the 2 independent mechanisms for controlling interrupt request?	Understand	CO 5	AEC010.18
8	Differentiate intra and inter system communication?	Remember	CO 5	AEC010.17
9	What you mean by bus arbitration?	Remember	CO 5	AEC010.17
10	What is DMA controller?	Understand	CO 5	AEC010.17
11	What are the three types of buses?	Remember	CO 5	AEC010.17
12	What is synchronous and asynchronous?	Understand	CO 5	AEC010.17
13	What is PCI interrupts?	Understand	CO 5	AEC010.18
14	What are the three different mechanism commonly used in bus arbitration?	Remember	CO 5	AEC010.18
15	What is meant by multiprocessor?	Understand	CO 5	AEC010.18
16	What is operating system?	Understand	CO 5	AEC010.20
17	Define deadlock?	Remember	CO 5	AEC010.20
18	Define advantages and disadvantages of bus organization?	Remember	CO 5	AEC010.17
19	Define availability in fault tolerance?	Understand	CO 5	AEC010.18
20	Distinguish the reliability and availability?	Understand	CO 5	AEC010.18
Group - B (Long Answer Questions)				
1	Discuss SIMD processor organization	Remember	CO 5	AEC010.19
2	Write a short notes on the following: 1. RISC/CISC –Differentiate 2. Stored program organization	Remember	CO 5	AEC010.19
3	Discuss the DMA operation with neat diagram in detail?	Understand	CO 5	AEC010.17
4	Write notes on: DMA and I/O interfaces.	Understand	CO 5	AEC010.17
5	What is fault tolerance? Give all the details regarding its function?	Remember	CO 5	AEC010.20
6	Write notes on: 1. Multiprogramming 2. Multiprocessing	Remember	CO 5	AEC010.20
7	Write a note sketch explain hoe data transfer can be carried out using DMA?	Understand	CO 5	AEC010.17
8	Write notes on polling.	Remember	CO 5	AEC010.17
9	What is meant by cache coherence problem, explain in detail.	Remember	CO 5	AEC010.18

10	Write notes on: 1.SynchronousI/O 2.AsynchronousI/O	Remember	CO 5	AEC010.17
11	Write a short notes on differences between RISC/CISC	Remember	CO 5	AEC010.19
12	Write a short notes on Stored program organization	Remember	CO 5	AEC010.17
13	Write notes on Vectored Interrupts.	Remember	CO 5	AEC010.18
14	Explain in detail the various aspects involved in fault tolerance.	Understand	CO 5	AEC010.18
15	Describe system bus structure for multiprocessors	Remember	CO 5	AEC010.19
16	Describe cache coherence and why is it important in shared memory multiprocessor systems? How can the problem be solved with a snoopy cache controller?	Remember	CO 5	AEC010.19
17	Determine the number of clock cycles that it takes to process 200 task in a six segment pipeline.	Understand	CO 5	AEC010.18
18	Explain in detail about DMA driven data transfer technique.	Remember	CO 5	AEC010.16
19	Describe the characteristics of super scalar and vector processing.	Remember	CO 5	AEC010.20
20	Describe about pipeline? Explain arithmetic pipeline.	Remember	CO 5	AEC010.18
Group - C (Analytical Questions)				
1	Consider a computer without priority interrupt hardware. Any one of many sources can interrupt the computer, and any interrupt request results in storing the return address and branching to a common interrupt routine. Explain how a priority can be established in the interrupt service program.	Remember	CO 5	AEC010.18
2	What programming steps are required to check when a source interrupts the computer while it is still being serviced by a previous interrupt request from the same source?	Understand	CO 5	AEC010.18
3	Write the RISC I instructions in assembly language that will cause a jump to address 3200 if the Z (zero) status bit is equal to 1. a. Using immediate mode b. Using a relative address mode (assume that PC =3400)	Remember	CO 5	AEC010.19
4	Write a program to evaluate the arithmetic statement: X = (A - B + C* (D * E - f)) / (G + H*K) a. Using a general register computer with three address instructions. b. Using a general register computer with two address instructions.	Understand	CO 5	AEC010.18
5	Write a program to evaluate the arithmetic statement: X = (A - B + C* (D * E - f)) / (G + H*K) 1. Using an accumulator type computer withone address instructions. 2. Using a stack organized computer with zero-address operation instructions.	Understand	CO 5	AEC010.18
6	What are the three different mechanism commonly used in bus arbitration and What are the various mechanism for implementing i/o operation?	Remember	CO 5	AEC010.16
7	What is the advantage of two-wired hand shaking method and detailed about data transfer between source and destination.	Remember	CO 5	AEC010.16
8	Write short notes on: 1. Kernel 2. Mutual exclusion	Remember	CO 5	AEC010.19

9	What programming steps are required to check when a source interrupts the computer while it is still being serviced by a previous interrupt request from the same source?	Remember	CO 5	AEC010.18
10	Write about the following concepts : a. RISC pipeline b. Vector processing c. Array processors	Remember	CO 5	AEC010.18

Prepared by:
Mr. N V Krishna Rao, Assistant Professor **HOD, ECE**