LECTURE NOTES

ON

PULSE AND DIGITAL CIRCUITS

B.Tech IV Semester (Autonomous)

(2018-19)

Ms. J Swetha
Assistant Professor

Ms. N Anusha
Assistant Professor

Mr. S Laxmana Chary
Assistant Professor

Mr. B Naresh
Assistant Professor

ELECTRONICS AND COMMUNICATION ENGINEERING

INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
DUNDIGAL, HYDERABAD - 500043

PULSE AND DIGITAL CIRCUITS

IV Semester: ECE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
AEC006	Foundation	3	1	-	4	30	70	100
Contact Classes: 45	Tutorial Classes: 15	Practical Classes: Nil				Total Classes: 60		

OBJECTIVES:

The course should enable the students to:

I. Proficient in the use of linear and nonlinear wave shaping circuits for sinusoidal, pulse and ramp inputs
II. Construct various multivibrators using transistors, and design sweep circuits and sampling gates.
III. Evaluate the methods to achieve frequency synchronization and division using the uni-junction transistors, multivibrators and symmetric circuits.
IV. Realize logic gates using diodes and transistors and distinguish between various logic families.

UNIT-I	WAVE SHAPING CIRCUITS	Classes: 10

Linear wave shaping circuits: High pass RC and low pass RC circuits, response to impulse and pulse inputs with different time constants, high pass RC circuit as a differentiator, low pass RC circuit as an integrator, switching characteristics of diode; Non-linear wave shaping circuits: Clipping circuits, diode clippers, shunt clippers, series clippers, clipping at two independent levels; Clamping circuits: Clamping theorem.

UNIT-II	MULTIVIBRATORS	Classes: 10

Multivibrators: Introduction, classification; Bistable multivibrator: Fixed bias, self bias, unsymmetrical triggering, symmetrical triggering; Schmitt trigger: Upper trigger point, lower trigger point, hysteresis, Applications of schmitt trigger; Monostable multivibrator: Collector coupled, triggering of monostable multivibrator; Astable multivibrator: Collector coupled, voltage to frequency converter.

UNIT-III	SAMPLING GATES AND TIME BASE GENERATORS	Classes: 08

Sampling gates: basic operating principle of sampling gate, uni and bi directional sampling gates.

Time base generators: General features of a time base signal; Methods of generating a time base waveform: Exponential sweep circuits, sweep circuit using uni junction transistor, Miller sweep circuit and Bootstrap sweep circuit.

UNIT-IV	SYNCHRONIZATION AND FREQUENCY DIVISION	Classes: 09

Synchronization and frequency division: Pulse synchronization of relaxation devices, frequency division with sweep circuits, other astable relaxation circuits, synchronization of astable multivibrator, monostable relaxation circuits as dividers, stability of relaxation dividers; Synchronization of a sweep circuit with symmetrical signals: Sinusoidal synchronization signals and sine wave frequency division with a sweep circuit.

UNIT-V	DIGITAL LOGIC FAMILIES	Classes: 08

Bipolar logic families: RTL, DTL, DCTL, HTL, TTL, ECL, MOS, and CMOS logic families, tristate logic; Interfacing of CMOS and TTL families.

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UNIT – I

WAVESHAPING CIRCUITS

A linear network is a network made up of linear elements only. A linear network can be described by linear differential equations. The principle of superposition and the principle of homogeneity hold good for linear networks. In pulse circuitry, there are a number of waveforms, which appear very frequently. The most important of these are sinusoidal, step, pulse, square wave, ramp, and exponential waveforms. The response of *RC, RL,* and *RLC* circuits to these signals is described in this chapter. Out of these signals, the sinusoidal signal has a unique characteristic that it preserves its shape when it is transmitted through a linear network, i.e. under steady state, the output will be a precise reproduction of the input sinusoidal signal. There will only be a change in the amplitude of the signal and there may be a phase shift between the input and the output waveforms. The influence of the circuit on the signal may then be completely specified by the ratio of the output to the input amplitude and by the phase angle between the output and the input. No other periodic waveform preserves its shape precisely when transmitted through a linear network, and in many cases the output signal may bear very little resemblance to the input signal. The process whereby the form of a non-sinusoidal signal is altered by transmission through a linear network is called linear wave shaping.

LOW-PASS RC CIRCUIT

Figure 1.1 shows a low-pass RC circuit. A low-pass circuit is a circuit, which transmits only low-frequency signals and attenuates or stops high-frequency signals.

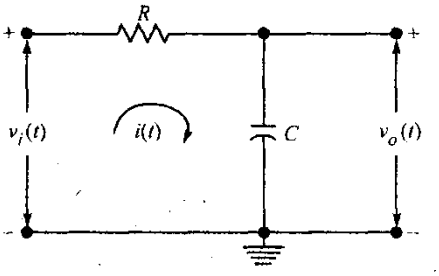


Figure 1.1 The low-pass *RC* circuit.

At zero frequency, the reactance of the capacitor is infinity (i.e. the capacitor acts as an open circuit) so the entire input appears at the output, i.e. the input is transmitted to the output with zero attenuation. So the output is the same as the input, i.e. the gain is unity. As the frequency increases the capacitive reactance decreases and so the output decreases. At very high frequencies the capacitor virtually acts as a short-circuit and the output falls to zero.

Sinusoidal Input

The Laplace transformed low-pass RC circuit is shown in Figure 1.2(a). The gain versus frequency curve of a low-pass circuit excited by a sinusoidal input is shown in Figure 1.2(b). This curve is obtained by keeping the amplitude of the input sinusoidal signal constant and varying its frequency and noting the output at each frequency. At low frequencies the output is equal to the input and hence the gain is unity. As the frequency increases, the output decreases and hence the gain decreases. The frequency at which the gain is $1/\sqrt{2}$ (= 0.707) of its maximum value is called the cut-off frequency. For a low-pass circuit, there is no lower cut-off frequency.

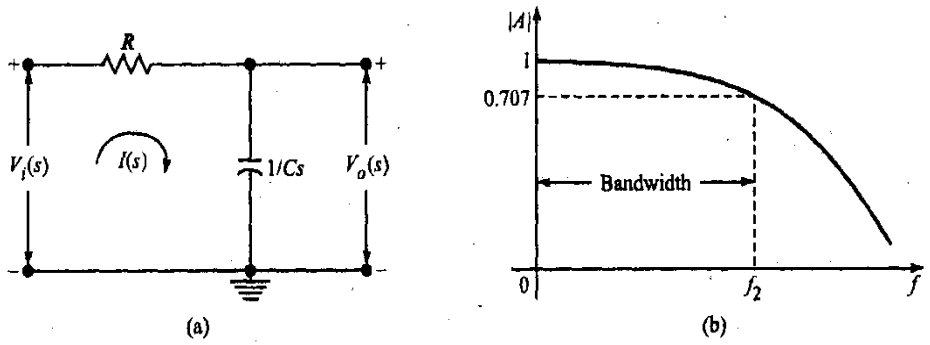


Figure 1.2 (a) Laplace transformed low-pass *RC* circuit and (b) its frequency response.

Step-Voltage Input

A step signal is one which maintains the value zero for all times $t < 0$, and maintains the value V for all times $t > 0$. The transition between the two voltage levels takes place at $t = 0$ and is accomplished in an arbitrarily small time interval. Thus, in Figure 1.3(a), $v_i = 0$ immediately before $t = 0$ (to be referred to as time $t = 0^-$) and $v_i = V$, immediately after t= 0 (to be referred to as time $t = 0^+$). In the low-pass *RC* circuit shown in Figure 1.1, if the capacitor is initially uncharged, when a step input is applied, since the voltage across the capacitor cannot change instantaneously, the output will be zero at $t = 0$, and then, as the capacitor charges, the output voltage rises exponentially towards the steady-state value V with a time constant *RC* as shown in Figure 1.3(b).

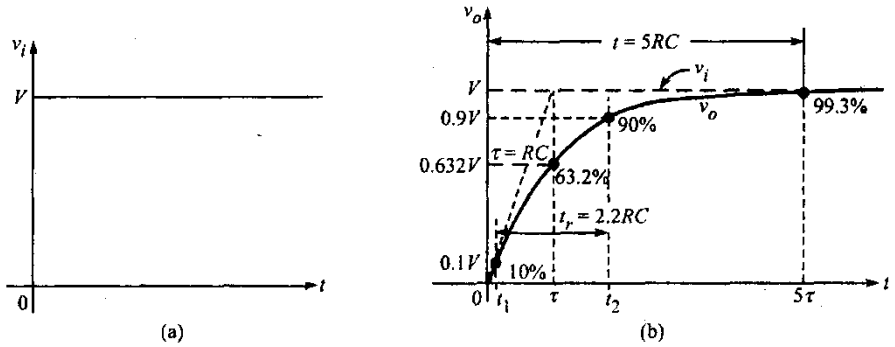


Figure 1.3 (a) Step input and (b) step response of the low-pass *RC* circuit.

$$Vo\ (t) = V(1\text{-}e^{-t/RC})$$

Expression for rise time

When a step signal is applied, the rise time t_r is defined as the time taken by the output voltage waveform to rise from 10% to 90% of its final value: It gives an indication of how fast the circuit can respond to a discontinuity in voltage.

$$t_r = 2.2RC$$

Pulse Input

The pulse shown in Figure 1.4(a) is equivalent to a positive step followed by a delayed negative step as shown in Figure 1 .4(b). So, the response of the low-pass *RC* circuit to a pulse for times less than the pulse width t_p is the same as that for a step input and is given by $v_0(t) = V(1 - e^{-t/RC})$. The responses of the low-pass *RC* circuit for time constant $RC \gg t_p$, *RC* smaller than t_p and *RC* very small compared to t_p are shown in Figures 1.5(a), 1.5(b), and 1.5(c) respectively. If the time constant *RC* of the circuit is very large, at the end of the pulse, the output voltage will be $V_p(t) = V(1 - e^{-t_p/RC})$, and the output will decrease to zero from this value with a time constant *RC* as shown in Figure 1.5(a). Observe that the pulse waveform is distorted when it is passed through a linear network. The output will always extend beyond the pulse width t_p, because whatever charge has accumulated across the capacitor *C* during the pulse cannot leak off instantaneously.

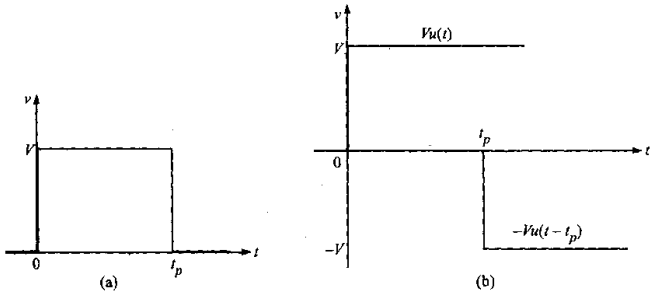


Figure 1.4 (a) A pulse and (b) a pulse in terms of steps.

If the time constant *RC* of the circuit is very small, the capacitor charges and discharges very quickly and the rise time t_r will be small and so the distortion in the wave shape is small. For minimum distortion (i.e. for reservation of wave shape), the rise time must be small compared to the pulse width t_p. If the upper 3-dB frequency /$_2$ is chosen equal to the reciprocal of the pulse width t_p, i.e. if $f_2 = 1/t_p$ then $t_r = 0.35t_p$ and the output is as shown in Figure 1.5(b), which for many applications is a reasonable reproduction of the input. As a rule of thumb, we can say

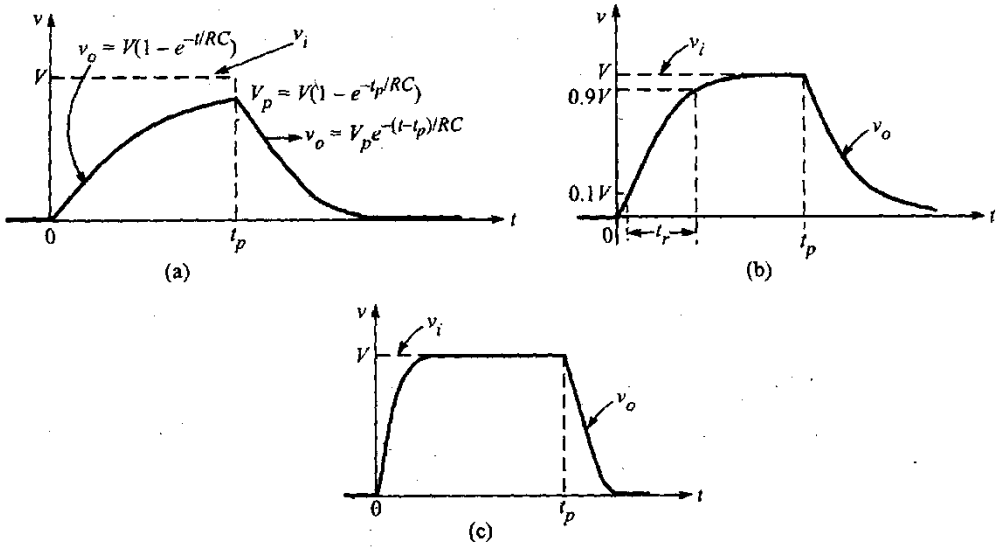


Figure 1.5 Pulse response for (a) $RC >> t_p$, (b) $RC < t_p$, and (c) $RC << t_p$.

Square-Wave Input

A square wave is a periodic waveform which maintains itself at one constant level *V'* with respect to ground for a time T_1 and then changes abruptly to another level *V"*, and remains constant at that level for a time T_2, and repeats itself at regular intervals of $T = T_1 + T_2$. A square wave may be treated as a series of positive and negative steps. The shape of the output waveform for a square wave input depends on the time constant of the circuit. If the time constant is very small, the rise time will also be small and a reasonable reproduction of the input may be obtained. For the square wave shown in Figure 1.6(a), the output waveform will be as shown in Figure 1.6(b) if the time constant *RC* of the circuit is small compared to the period of the input waveform. In this case, the wave shape is preserved. If the time constant is comparable with the period of the input square wave, the output will be as shown id Figure 1.6(c). The output rises and falls exponentially. If the time constant is very large compared to the period of the input waveform, the output consists of exponential sections, which are essentially linear as indicated in Figure 1.6(d). Since the average voltage across *R* is zero, the dc voltage at the output is the same as that of the input. This average value is indicated as *V&*.

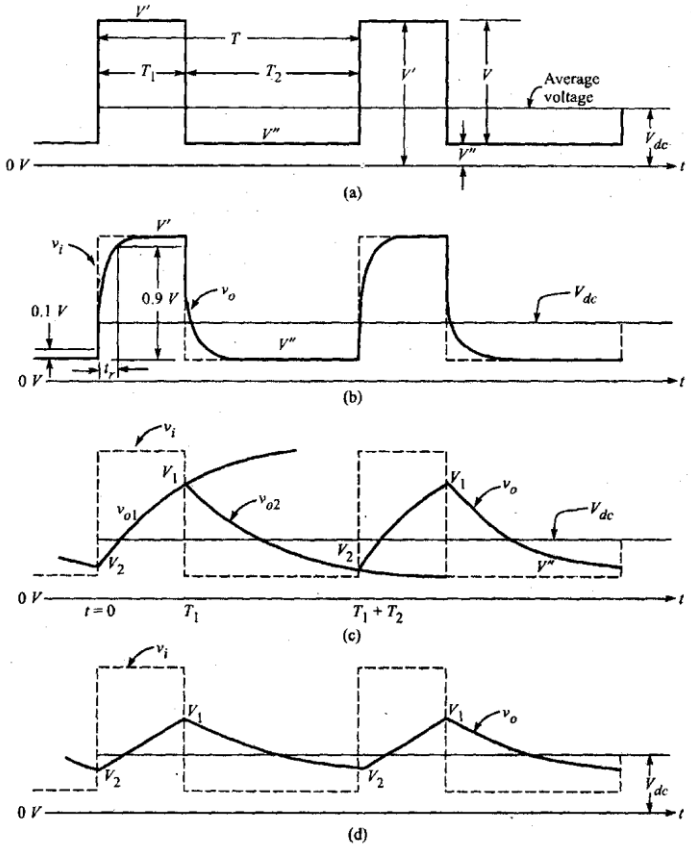


Fig. 1.6 Responses of Low pass RC Circuit With square wave Input

LOW-PASS *RC* CIRCUIT AS AN INTEGRATOR

If the time constant of an RC low-pass circuit is very large, the capacitor charges very slowly and so almost all the input voltage appears across the resistor for small values of time. As time increases, the voltage drop across C does not remain negligible compared with that across R and the output will not remain the integral of the input. The output will change from a quadratic to a linear function of time. If the time constant of an RC low-pass circuit is very large in comparison with the. Time required for the input signal to make an appreciable change, the circuit acts as an integrator. A criterion for good integration in terms of steady-state analysis is as follows: The low-pass circuit acts as an integrator provided the time constant of the circuit RC > 15T, where T is the period of the input sine wave. When RC > 15T, the input sinusoid will be shifted at least by 89.4° (instead of the ideal 90° shift required for integration) when it is transmitted through the network.

HIGH-PASS *RC* CIRCUIT

At zero frequency the reactance of the capacitor is infinity and so it blocks the input and hence the output is zero. Hence, this capacitor is called the blocking capacitor and this circuit, also called the *capacitive coupling circuit*, is used to provide dc isolation between the input and the output. As the frequency increases, the reactance of the capacitor decreases and hence the output and gain increase. At very high frequencies, the capacitive reactance is very small so a very small voltage appears, across *C* and, so the output is almost equal to the input and the gain is equal to 1. Since this circuit attenuates low-frequency signals and allows transmission of high-frequency signals with little or no attenuation, it is called a high-pass circuit.

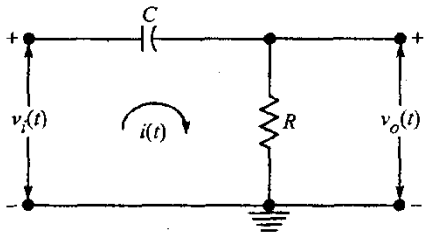


Figure 1.30 The high-pass *RC* circuit.

Sinusoidal Input

Figure 1.31 (a) shows the Laplace transformed high-pass *RC* circuit. The gain versus frequency curve of a high-pass circuit excited by a sinusoidal input is shown in Figure 1.31(b). For a sinusoidal input v, the output signal v_0 increases in amplitude with increasing frequency. The frequency at which the gain is 1/V2 of its maximum value is called the lower cut-off or lower 3-dB frequency. For a high-pass circuit, there is no upper cut-off frequency because all high frequency signals are transmitted with zero attenuation. Therefore, $f_2 - f_1$. Hence bandwidth B.W= f_2 - fi =∞

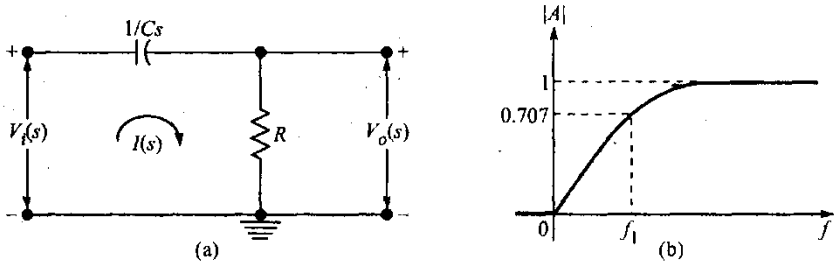


Figure 1.31 (a) Laplace transformed high-pass circuit and (b) gain versus frequency plot.

Step Input

When a step signal of amplitude *V* volts shown in Figure 1.32(a) is applied to the high- pass *RC* circuit of Figure 1.30, since the voltage across the capacitor cannot change instantaneously the output will be just equal to the input at $t = 0$ (for f < 0, v,- = 0 and $v_a = 0$). Later when the capacitor charges exponentially, the output reduces exponentially with the same time constant *RC.* The expression for the output voltage for $t > 0$ is given by Figure 1.32(b) shows the response of the circuit for large, small, and very small time constants. For $t > 5r$, the output will reach more than 99% of its final value. Hence although the steady state is approached asymptotically, for most applications we may assume that the final value has been reached after 5f. If the initial slope of the exponential is maintained, the output falls to zero in a time $t = T$.

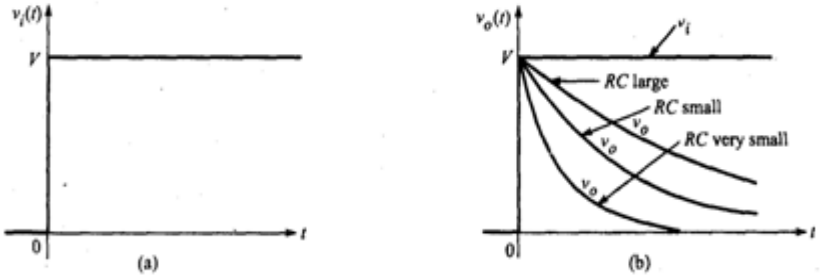


Figure 1.32 (a) Step input and (b) step response for different time constants.

Pulse Input

A pulse of amplitude *V* and duration t_p shown in Figure 1.4(a) is nothing but the sum of a positive step of amplitude *V* starting at $t = 0$ and a negative step of amplitude *V* starting at t_p as shown in Figure 1.4(b). So, the response of the circuit for $0 < t < t_p$, for the pulse input is the same as that for a step input and is given by $v_0(t) = Ve^{-t/RC}$. At $t = t_p$, $v_o(t) = V = Ve^{-t/RC}$. At $t = t_p$, since the input falls by *V* volts suddenly and since the voltage across the capacitor cannot change instantaneously, the output also falls suddenly by *V* volts to $V_p - V$. Hence at $t = t_p^+$, $v_a(t) = Ve^{-t_p/RC} - V$. Since $V_p < V$, $V_p - V$ is negative. The output waveforms for $RC \gg t_p$, *RC* comparable to t_p and $RC \ll t_p$ are shown in Figures 1.33(a), (b), and (c) respectively. There is distortion in the outputs and the distortion is the least when the time constant is very large. Observe that there is positive area

and negative area in the output waveforms. The negative area will always be equal to the positive area. So if the time constant is very large the tilt (the almost linear decrease in the output voltage) will be small and hence the undershoot will be very small, and for $t > t_p$, the output rises towards the zero level very very slowly. If the time constant is very small compared to the pulse width (i.e. $RC/t_p \ll T$), the output consists of a positive spike or pip of amplitude V volts at the beginning of the pulse and a negative spike of the same amplitude at the end of the pulse. Hence a high-pass circuit with a very small time constant is called a *peaking circuit* and this process of converting pulses into pips by means of a circuit of short time constant is called peaking.

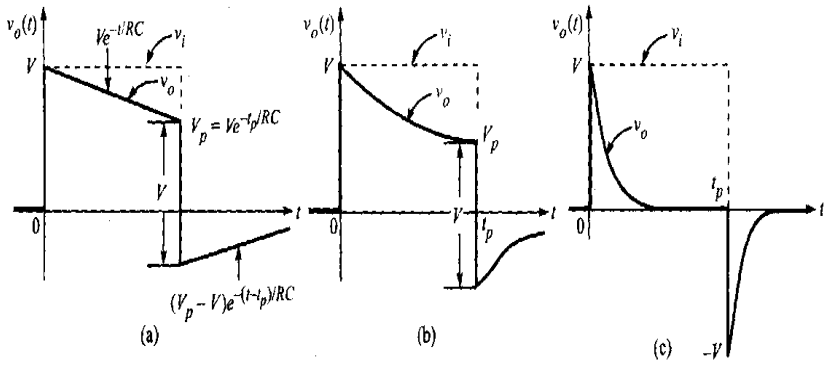


Figure 1.33 Pulse response for (a) $RC >> t_p$, (b) RC comparable to t_p and (c) $RC << t_p$.

Square-Wave Input

A square wave shown in Figure 1.34(a) is a periodic waveform, which maintains itself at one constant level V with respect to ground for a time T_ℓ and then changes abruptly to another level V'' and remains constant at that level for a time T_2, and then repeats itself at regular intervals of $T = T\backslash + T_2$. A square wave may be treated as a series of positive and negative steps. The shape of the output depends on the time constant of the circuit. Figures 1.34(b), 1.34(c), 1.34(d), and 1.34(e) show the output waveforms of the high-pass RC circuit under .steady-state conditions for the cases (a) $RC » T$, (b) $RC > T$, (c) RC - T, and (d) $RC « T$ respectively. When the time constant is arbitrarily large the output is same as the input but with zero dc level. When $RC > T$, the output is in the form of a tilt. When RC is comparable to T, the output rises and falls exponentially. When $RC « T$ (i.e. $RCIT\backslash$ and RC/T_2 *are very* small in comparison to unity), the output consists of alternate positive and negative spikes. In this case the peak-to-peak amplitude of the output is twice the peak-to-peak value of the input. In fact, for any periodic input waveform under steady-state conditions.

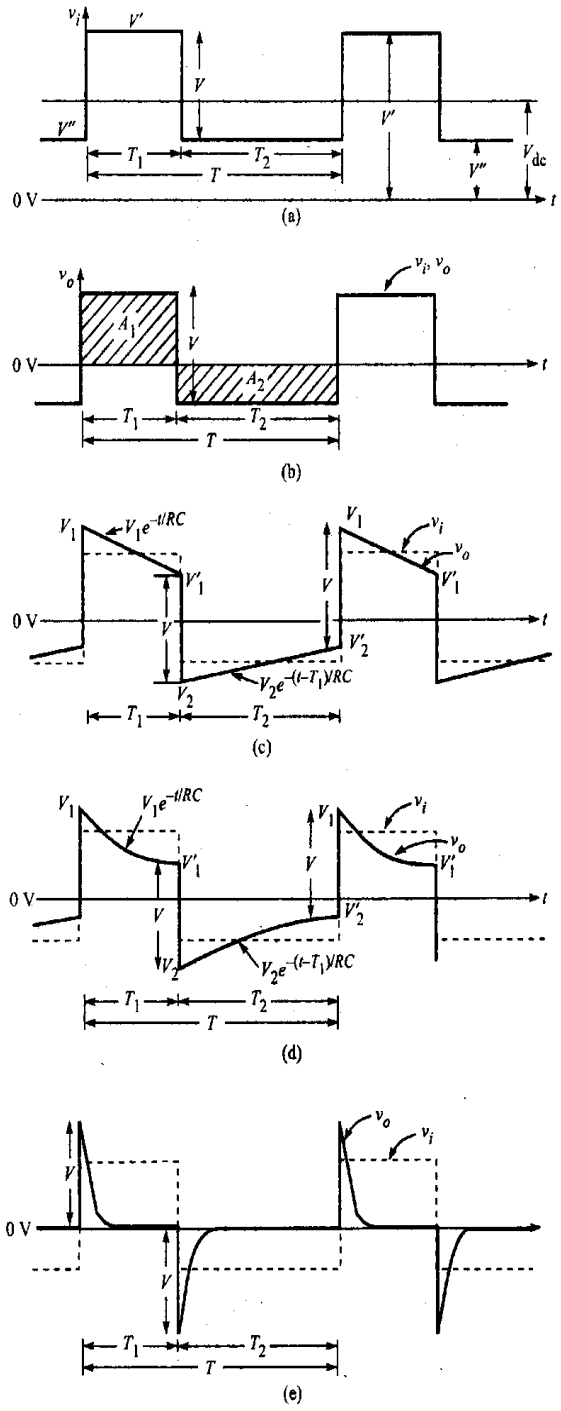


Figure 1.34 (a) A square wave input, (b) output when RC is arbitrarily large, (c) output when $RC > T$, (d) output when RC is comparable to T, and (e) output when $RC \ll T$.

High-Pass *RC* Circuit as Differentiator

When the time constant of the high-pass RC circuit is very small, the capacitor charges very quickly, so almost all the input v,(0 appears across the capacitor and the voltage across the resistor will be negligible compared to the voltage across the capacitor. Hence the current is determined entirely by the capacitance.

$$V_0(t) = RC \frac{dv_i(t)}{dt}$$

Thus we see that the output is proportional to the derivative of the input. The high-pass RC circuit acts as a differentiator provided the RC time constant of the circuit is very small in comparison with the time required for the input signal to make an appreciable change. The derivative of a step signal is an impulse of infinite amplitude at the occurrence of the discontinuity of step. The derivative of an ideal pulse is a positive impulse followed by a delayed negative impulse, each of infinite amplitude and occurring at the points of discontinuity. The derivative of a square wave is a waveform which is uniformly zero except, at the points of discontinuity. At these points, precise differentiation would yield impulses of infinite amplitude, zero width and alternating polarity. For a square wave input, an RC high-pass circuit with very small time constant will produce an output, which is zero except at the points of discontinuity. At these points of discontinuity, there will be peaks of finite amplitude V. This is because the voltage across R is not negligible compared with that across C.

Switching Characteristics of Diode:

Diode forward recovery time:

When a diode is driven from the: reverse-biased condition to the forward-biased condition or in the opposite direction, the diode response is accompanied by a transient, and an interval of time elapses before the diode recovers to its steady state. The nature of the forward recovery transient depends on the magnitude of the current being driven through the diode and the rise time of the driving signal. Consider the voltage which develops across the diode when the input is a current source supplying a step current I_v as shown in Figure1.7 (a). If the current amplitude is comparable to or larger than the diode rated current, and if the rise time of the current step is small enough, then the waveform of the voltage which appears across the diode is shown in Figure 1.7(b).

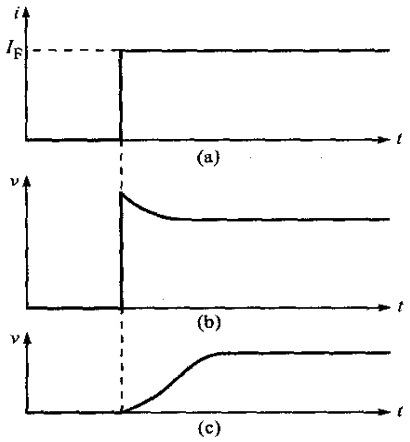


Figure 1.7 (a) Input step current to a diode, (b) diode voltage when the current is large, arid (c) diode voltage when the current is small.

Diode reverse recovery time

When an external voltage is impressed across a junction in the direction that reverse biases it, very little current called the reverse saturation current flows. This current is because of the minority carriers.

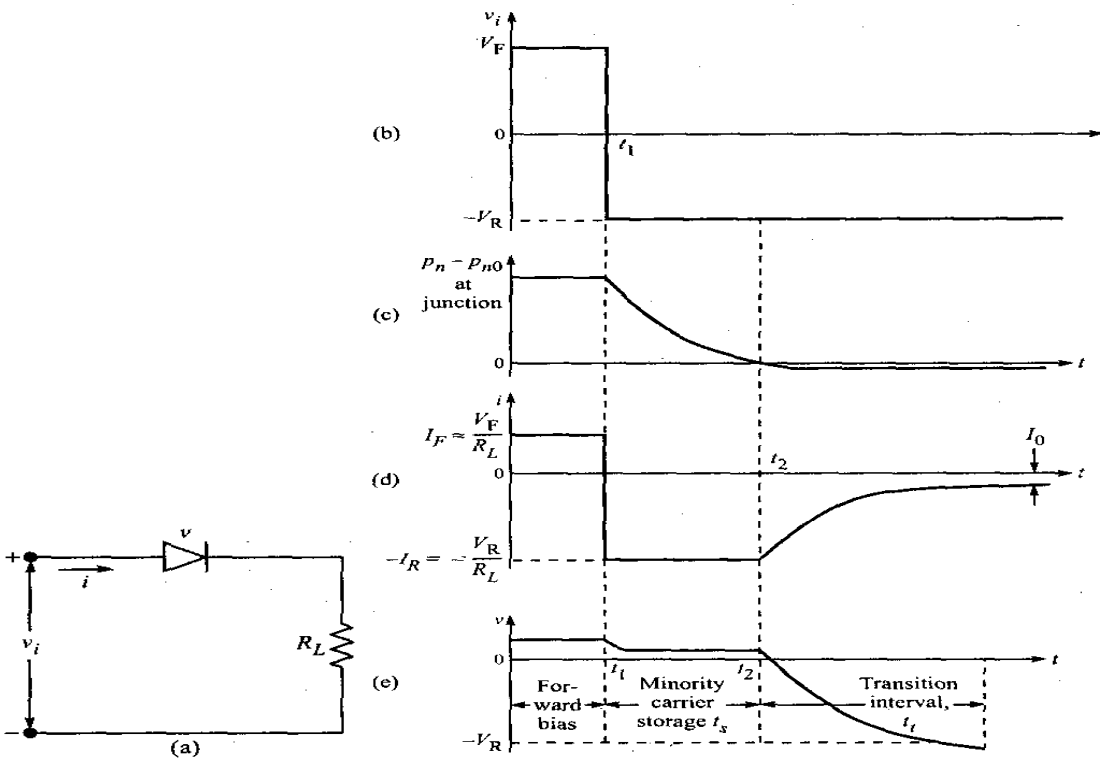


Figure 1.8 The waveform in (b) is applied to the diode circuit in (a), (c) the excess carrier density at the junction, (d) the diode current, and (e) the diode voltage.

NON LINEAR WAVESHAPING

Shunt Clippers

Clipping above reference level

Using the ideal diode characteristic of Figure 1.9(a), the clipping circuit shown in Figure 1.9(b), has the transmission characteristic shown in Figure 1.9(c). The transmission characteristic which is a plot of the output voltage v_0 as a function of the input voltage v, also exhibits piece-wise linear discontinuity. The break point occurs at the reference voltage VR. To the left of the break point i.e. for $v_t < V_R$ the diode is reverse biased (OFF) and the equivalent circuit shown in Figure 1.9(d) results. In this region the signal v, may be transmitted directly to the output, since there is no load across the output to cause a drop across the series resistor /?. To the right of the break point i.e. for $v_(> V_R$ the diode is forward biased (ON) and the equivalent circuit shown in Figure 1.9(e) results and increments in the inputs are totally attenuated and the output is fixed at V_R. Figure 1.9(c) shows a sinusoidal input signal of amplitude large enough so that the signal makes excursions past the break point. The corresponding output exhibits a suppression of the positive peak of the signal. The output will appear as if the positive peak had been clipped off or sliced off.

Clipping below reference level

If this clipping circuit of Figure 1.9(b), is modified by reversing the diode as shown in Figure 1.10(a), the corresponding piece-wise linear transfer characteristic and the output for a sinusoidal input will be as shown in Figure 1.10(b). In this circuit, the portion of the waveform more positive than V_R is transmitted without any attenuation but the portion of the waveform less positive than V_R is totally suppressed. For Vj < V_R, the diode conducts and acts as a short circuit and the equivalent circuit shown in Figure 1.10(c) results and the output is fixed at V_R. For v, > V_R, the diode is reverse biased and acts as an open circuit and the equivalent circuit shown in Figure 1.10(d) results and the output is the same as the input.

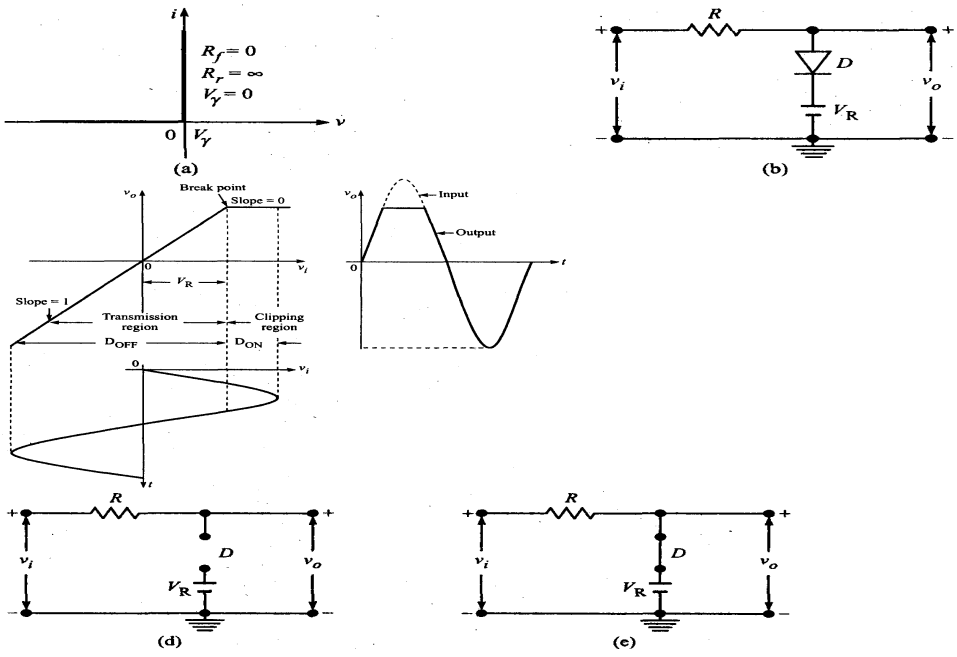


Figure 1.9 (a) *v-i* characteristic of an ideal diode, (b) diode clipping circuit, which removes that part of the waveform that is more positive than V_R, (c) the piece-wise linear transmission characteristic of the circuit, a sinusoidal input and the clipped output, (d) equivalent circuit for $v_(< V_R$, and (e) equivalent circuit for v, > V_R.

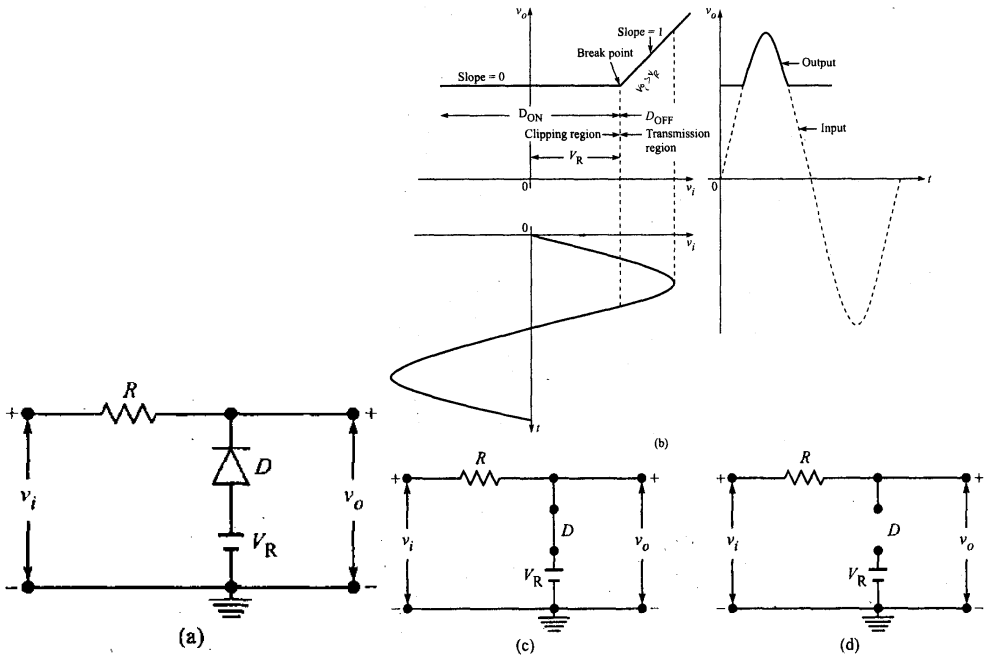


Figure 1.10(a) A diode clipping circuit, which transmits that part of the sine wave that is more positive than VR, (b) the piece-wise linear transmission characteristic, a sinusoidal input and the clipped output, (c) equivalent circuit for $v_{(} < V_R$, and (d) equivalent circuit for v,- > VR.

Series and Shunt Noise Clippers

Practically actual signals will be mostly associated with unwanted noise signals. The presence of noise signals may adversely affect sensitive circuits. So the noise signals must be eliminated to make the actual signal free from distortions and fluctuations. Noise signals can be eliminated by employing noise clippers. These clippers use two or more diodes depending upon whether the noise is quite small or considerably large. Noise clippers are of two types: series noise clippers and shunt noise clippers.

Transistor Clippers

A nonlinear device is required for clipping purposes. A diode exhibits a nonlinearity, which occurs when it goes from OFF to ON. On the other hand, the transistor has two pronounced nonlinearities, which may be used for clipping purposes. One occurs when the transistor crosses from the cut-in region into the active region and the second occurs when the transistor crosses from the active region into the saturation region. Therefore, if the peak-to-peak value of the input waveform is such that it can carry the transistor across the boundary between the cut-in and active regions, or across the boundary between the active and saturation regions, a portion of the input waveform will be clipped. Normally, it is required that the portion of the input waveform, which keeps the transistor in the active region shall appear at the output without distortion. In that case, it is required that the input current rather than the input voltage be the waveform of the

signal of interest. The reason for this requirement is that over a large signal excursion in the active region, the transistor output current responds nominally linearly to the input current but is related in a quite nonlinear manner to the input voltage. So, in transistor clippers a current drive needs to be used.

A transistor clipper is shown in Figure 1.11. The resistor *R* which represents either the signal source impedance or a resistor deliberately introduced must be large compared with the input resistance of the transistor in the active region. Under these circumstances, the input base current will very nearly have the waveform of the input voltage, because the base current is given by $i_B = (v_i - V_\gamma)/R$ where V_r is the base-to-emitter cut-in voltage. V_y » 0.1 V for Ge and V_y ~ 0.5 V for Si.

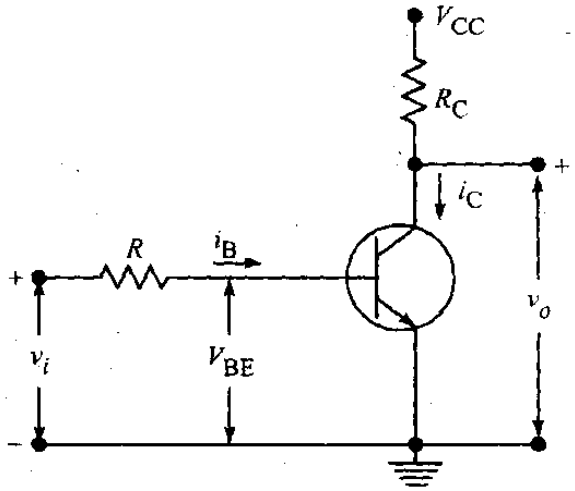


Figure 1.11 transistor clipper

CLAMPING CIRCUITS

Clamping circuits are circuits, which are used to clamp or fix the extremity of a periodic waveform to some constant reference level $V._R$. Under steady-state conditions, these circuits restrain the extremity of the waveform from going beyond V_R. Clamping circuits may be one- way clamps or two-way clamps. When only one diode is used and a voltage change in only one direction is restrained, the circuits are called one-way clamps. When two diodes are used and the voltage change in both the directions is restrained, the circuits are called two-way clamps.

The Clamping Operation

When a signal is transmitted through a capacitive coupling network (RC high-pass circuit), it loses its dc component, and a clamping circuit may be used to introduce a dc component by fixing the positive or negative extremity of that waveform to some reference level. For this reason, the clamping circuit is often referred to as dc restorer or dc reinserter. In fact, it should be called a dc inserter, because the dc component introduced may be different from the dc component lost during transmission. The clamping circuit only changes the dc level of the input signal. It does not affect its shape.

Negative Clamper

Figure 1.12 (a) shows the circuit diagram of a basic negative clamper. It is also termed a positive peak clamper since the circuit clamps the positive peak of a signal to zero level. Assume that the signal source has negligible output impedance and that the diode" is ideal, *Rf*= 0 n and V_y = 0 V in that, it exhibits an arbitrarily sharp break at 0 V, and that its input signal shown in Figure 1.12(b) is a sinusoid which begins at t = 0. Let the capacitor C be unchanged at t = 0.

During the first quarter cycle, the input signal rises from zero to the maximum value. The diode conducts during this time and since we have assumed an ideal diode, the voltage across it is zero. The capacitor *C* is charged through the series combination of the signal source and the diode and the voltage across C rises sinusoidally. At -the end of the first quarter cycle, the voltage across the capacitor, $v_c = V_m$. When, after the first quarter cycle, the peak has been passed and the input signal begins to fall, the voltage v_c across the capacitor is no longer able to follow the input, because there is no path for the capacitor to discharge. Hence, the voltage across the capacitor remains constant at $v_c = V_m$, and the charged capacitor acts as a voltage source of V.

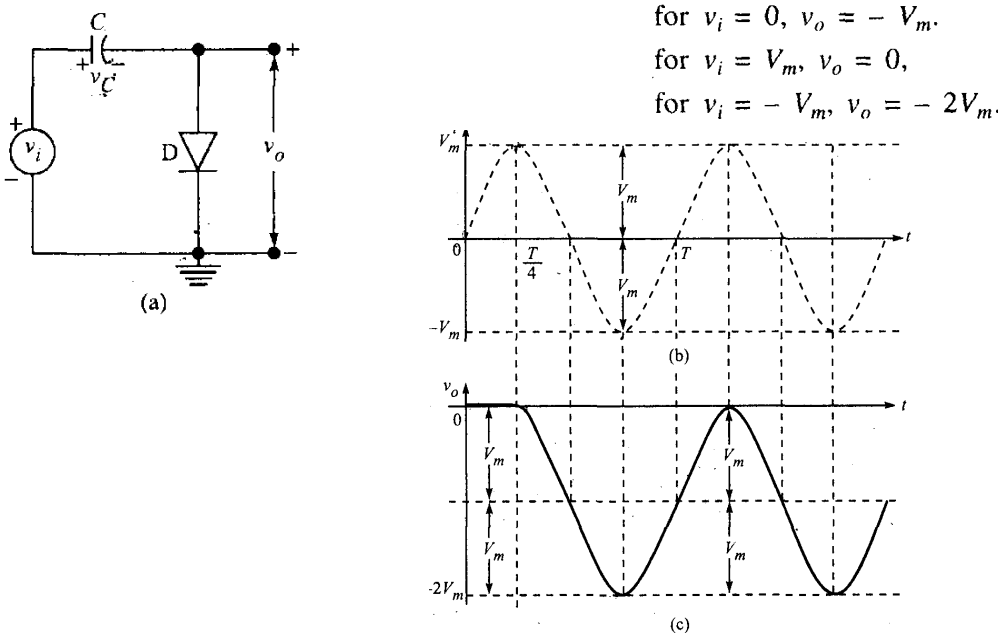


Figure1.12 (a) A negative clamping circuit, (b) a sinusoidal input, and (c) a steady-state clamped output.

Positive Clamper

Figure 1.13(a) shows a positive clamper. This is also termed as negative peak clamper since this circuit clamps the negative peaks of a signal to zero level. The negative peak clamper, i.e. the positive clamper introduces a positive dc.

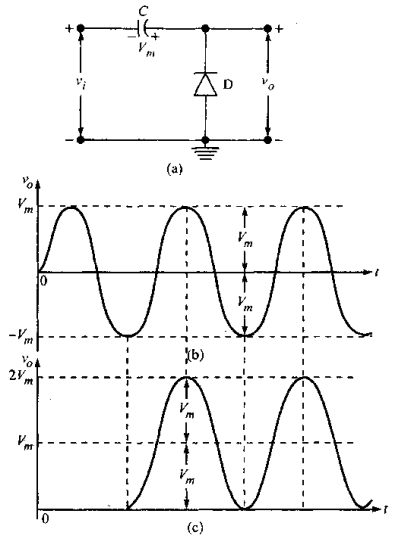


Figure 1.13: positive clamper

Let the input voltage be $v_i = V_m$ sinwt. When v, goes negative, the diode gets forward biased and conducts and in a few cycles the capacitor gets charged to V_m with the polarity shown in Figure 2.73(a). Under steady-state conditions, the capacitor acts as a

Constant voltage source and the output is $v_o = v_i - (-V_m) = v_i + V_m$.

Based on the above relation between v_0 and v,, the output voltage waveform is plotted. As seen in Figure 2.73(c) the negative peaks of the input signal are clamped to zero level. Peak-to- peak value of output voltage = peak-to-peak value of input voltage = $2V_m$. There is no distortion of waveform.

Clamping Circuit Theorem

Under steady-state conditions, for any input waveform, the shape of the output waveform of a clamping circuit is fixed and also the area in the forward direction (when the diode conducts) and the area in the reverse direction (when the diode does not conduct) are related.

The clamping circuit theorem states that, for any input waveform under steady-state conditions, the ratio of the area Af under the output voltage curve in the forward direction to that in the reverse direction A_r is equal to the ratio R_f/Rr.

UNIT – II

MULTIVIBRATORS

Multi means many, vibrator means oscillator. A circuit which can oscillate at a number of frequencies is called a multivibrator. Basically there are three types of multivibrators

1. Bistable multivibrator
2. Monostable multivibrator
3. Astable multivibrator

Each of these multivibrators has two states. As the names indicate, a bistable multivibrator has got two stable states, a monostable multivibrator has got only one stable state (the other state being quasi stable) and the astable multivibrator has got no stable state (both the states being quasi stable). The stable state of a multivibrator is the state in which the device can stay permanently. Only when a proper external triggering signal is applied, it will change its state. Quasi stable state means temporarily stable state. The device cannot stay permanently in this state. After a predetermined time, the device will automatically come out of the quasi stable state.

They have two cross-coupled inverters, i.e. the output of the first stage is coupled to the input of the second stage and the output of the second stage is coupled to the input of the first stage. In bistable circuits both the coupling elements are resistors (i.e. both are dc couplings). In monostable circuits, one coupling element is a capacitor (ac coupling) and the other coupling element is a resistor (dc coupling) In astable multivibrators both the coupling elements are capacitors (i.e. both are ac couplings).

A bistable multivibrator requires a triggering signal to change from one stable state to another. It requires another triggering signal for the reverse transition. A monostable multivibrator requires a triggering signal to change from the stable state to the quasi stable state but no triggering signal is required for the reverse transition, i.e. to bring it from the quasi stable state to the stable state. The astable multivibrator does not require any triggering signal at all. It keeps changing from one quasi stable state to another quasi stable state on its own the moment it is connected to the supply.

A bistable multivibrator is the basic memory element. It is used to perform many digital operations such as counting and storing of binary data. It also finds extensive applications in the generation and processing of pulse type waveforms. The monostable multivibrator finds extensive applications in pulse circuits. Mostly it is used as a gating circuit or a delay circuit. The astable circuit is used as a master oscillator to generate square waves. It is often a basic source of fast waveforms. It is a free running oscillator. It is called a square wave generator. It is also termed a relaxation oscillator.

BISTABLE MULTIVIBRATOR

A bistable multivibrator is a multivibrator which can exist indefinitely in either of its two stable states and which can be induced to make an abrupt transition from one state to the other by means of external excitation. In a bistable multivibrator both the coupling elements are resistors (dc coupling). The bistable multivibrator is also called a multi, Eccles-Jordan circuit (after its inventors), trigger circuit, scale-of-two toggle circuit, flip-flop, and binary. There are two types of bistable multivibrators

1. Collector coupled bistable multivibrator
2. Emitter coupled bistable multivibrator

There are two types of collector-coupled bistable multivibrators:

1. Fixed-bias bistable multivibrator
2. Self-bias bistable multivibrator

A FIXED-BIAS BISTABLE MULTIVIBRATOR

Figure 2.1 shows the circuit diagram of a fixed-bias bistable multivibrator using transistors (inverters). Note, that the output of each amplifier is direct coupled to the input of the other amplifier. In one of the stable states, transistor Q is ON (i.e. in saturation) and Q_2 is OFF (i.e. in cut-off), and in the other stable state Q1 is OFF and Q_2 is ON. Even though the circuit is symmetrical, it is not possible for the circuit to remain in a stable state with both the transistors conducting (i.e. both operating in the active region) simultaneously and carrying equal currents. The reason is that if we assume that both the transistors are biased equally and are carrying equal currents. Let us say it increases by a small amount then the voltage at the collector of Q1 decreases. This will result in a decrease in voltage at the base of Q_2. So Q_2 conducts less and $/_2$ decreases and hence the potential at the collector of Q_2 increases. This results in an increase in the base potential of *Qi*. So, Qi conducts still further increased and the potential at the collector of Q_1 is further reduced, and so on. So, the current *I*\ keeps on increasing and the current keeps on decreasing till Q $_{(}$goes into saturation and Q_2 goes into cut-off. This action takes place because of the regenerative feedback incorporated into the circuit and will occur only if the loop gain is greater than one. A stable state of a binary is one in which the voltages and currents satisfy the Kirchhoff's laws and are consistent with the device characteristics and in which, in addition, the condition of the loop gain being less than unity is satisfied.

The condition with respect to loop gain will certainly be satisfied, if either of the two devices is below cut-off or if either device is in saturation. But normally the circuit is designed such that in a stable state one transistor is in saturation and the other one is ir cut-off, because if one transistor is biased to be in cut-off and the other one to be in active region, as the temperature changes or the devices age and the device parameters vary, the

quiescent point changes and the quiescent output voltage may also change appreciably Sometimes the drift may be so much that the device operating in the active region may go into cut-off, and with both the devices in cut-off the circuit will be useless.

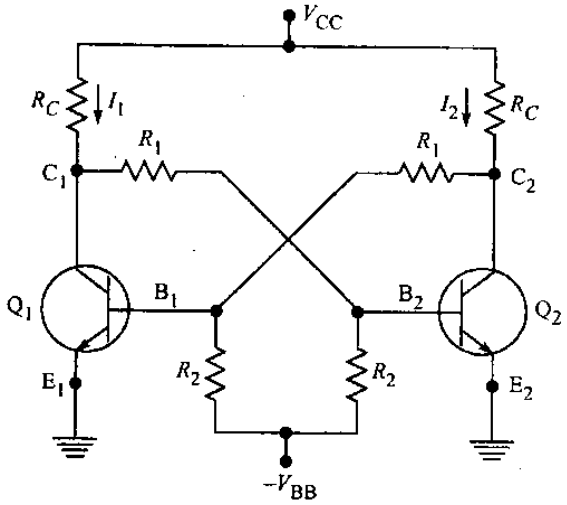


Figure 2.1: Bistable Multivibrator

Transistor as an ON-OFF switch

In digital circuits transistors operate either in the cut-off region or in the saturation region. Specially designed transistors called switching transistors with negligible active region are used. In the cut-off region the transistor does not conduct and acts as a open switch. In the saturation region the transistor conducts heavily and acts as a closed switch-In a binary which uses two cross-coupled transistors, each of the transistors is alternately cut-off and driven into saturation.

COMMUTATING CAPACITORS

We know that the bistable multivibrator has got two stable states and that it can remain in either of its two stable states indefinitely. It can change state only when a triggering signal such as a pulse from some external source is applied. When a triggering signal is applied, conduction has to transfer from one device to another. The transition time is defined as the interval during which conduction transfers from one transistor to another. The reason for this transition time is even though the input signal at the base of a transistor may be transferred to the collector with zero rise time, the signal at the collector of the transistor cannot be transferred to the base of the other transistor instantaneously. This is because the input capacitance C, present at the base of the transistor makes the *R\-R2* attenuator act as an uncompensated attenuator and so it will have a finite rise time, $t_r = (R_1 \backslash\backslash R_2)C_i$.

A transistor having been induced to change the state by a triggering signal, a certain minimum time must elapse before a succeeding signal is able to reliably induce the reverse transition. The smallest allowable interval between triggers is called the *resolving time* of the flip-flop, and its reciprocal is the maximum

frequency at which the binary will respond.

The complete transfer of conduction from one device to another involves two phases. The first of these is the transition time during which conduction transfers from one device to another. For this transfer of conduction to take place, the voltages across the input and output capacitances of the transistor have to change. The voltages across the commutating capacitors need not change during this transfer of conduction. After this transfer of conduction, the capacitors are allowed to interchange their voltages. This additional time required for the purpose of completing the recharging of capacitors after the transfer of conduction is called the settling time. Of course, no clear-cut distinction can be made between the transition time and the settling time. The sum of the transition time and the settling time is called the resolution time.

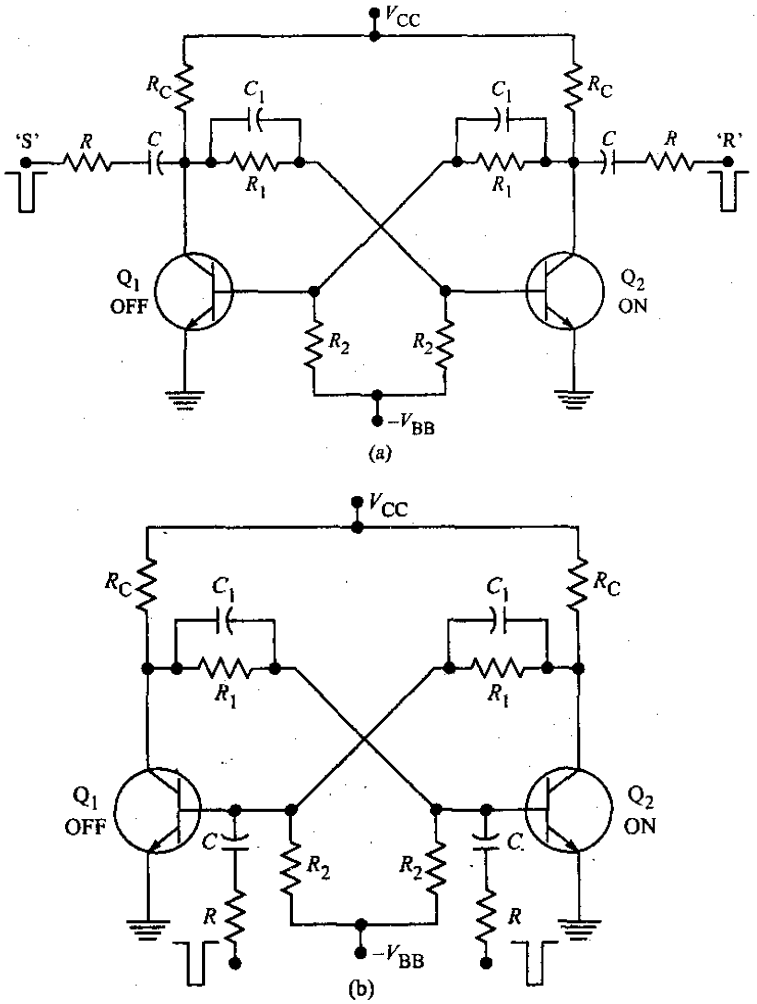


Figure 2.2 Unsymmetrical triggering through a resistor and a capacitor (a) at the collectors and (b) at the bases.

An excellent method for triggering a binary unsymmetrically on the leading edge of a pulse is to apply the pulse from a high impedance source to the output of the non-conducting device For p-n-p transistors, a positive pulse needs to be applied.

The triggering signal may be applied through a resistor and a capacitor or through a unilateral device such as a diode. Figure 2.2 shows a method of triggering unsymmetncally through a resistor and a capacitor.

Applications of Schmitt trigger circuit

Schmitt trigger is also a bistable multivibrator. Hence it can be used in applications where a normal binary is used. However for applications where the circuit is to be triggered back-and-forth between stable states, the normal binary is preferred because of its symmetry. Since the base of Q is not involved in regenerative switching, the Schmitt trigger is preferred for applications in which the advantage of this free terminal can be taken. The resistance of output circuit of Q_2 is not required for the operation of the binary. Hence this resistance may be selected over a wide range to obtain different output signal amplitudes.

A most important application of the Schmitt trigger is its use as an amplitude comparator to mark the instant at which an arbitrary waveform attains a particular reference level. As input v rises to Vi or falls to V_2, the circuit makes a fast regenerative transfer to its other state. Another important application of the Schmitt trigger is as a squaring circuit. It can convert a sine wave into a square wave. In fact, any slowly varying input waveform can be converted into a square wave with faster leading and trailing edges as shown in Figure 2.3, if the input has large enough excursions to carry the input beyond the limits of the hysteresis range, $V_H = V\backslash - V_2$.

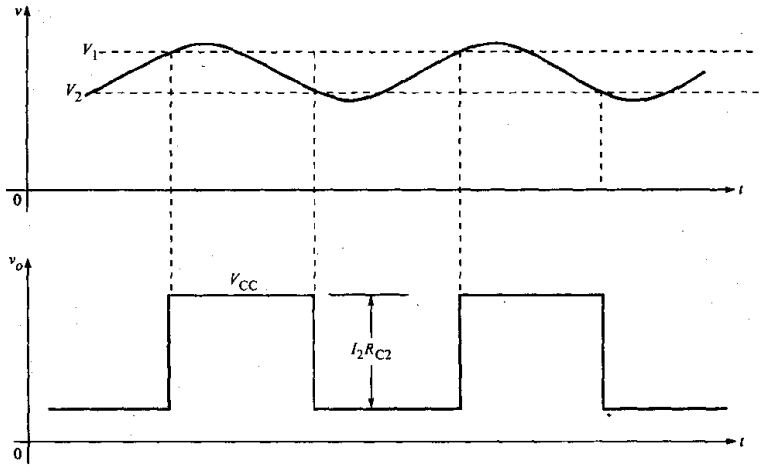


Figure 2.3 Response of the emitter-coupled binary to an arbitrary input waveform.

MONOSTABLE MULTIVIBRATOR

As the name indicates, a monostable multivibrator has got only one permanent stable state, the other state being quasi stable. Under quiescent conditions, the monostable multivibrator will be in its stable state only. A triggering signal is required to induce a transition from the stable state to the quasi stable state.

Once triggered properly the circuit may remain in its quasi stable state for a time which is very long compared with the time of transition between the states, and after that it will return to its original state. No external triggering signal is required to induce this reverse transition. In a monostable multivibrator one coupling element is a resistor and another coupling element is a capacitor.

When triggered, since the circuit returns to its original state by itself after a time T, it is known as a one- shot, a single-step, or a univibrator. Since it generates a rectangular waveform which can be used to gate other circuits, it is also called a gating circuit. Furthermore, since it generates a fast transition at a predetermin6d time T after the input trigger, it is also referred to as a delay circuit. The monostable multivibrator may be a collector-coupled one, or an emitter-coupled one.

Collector Coupled Monostable Multivibrator

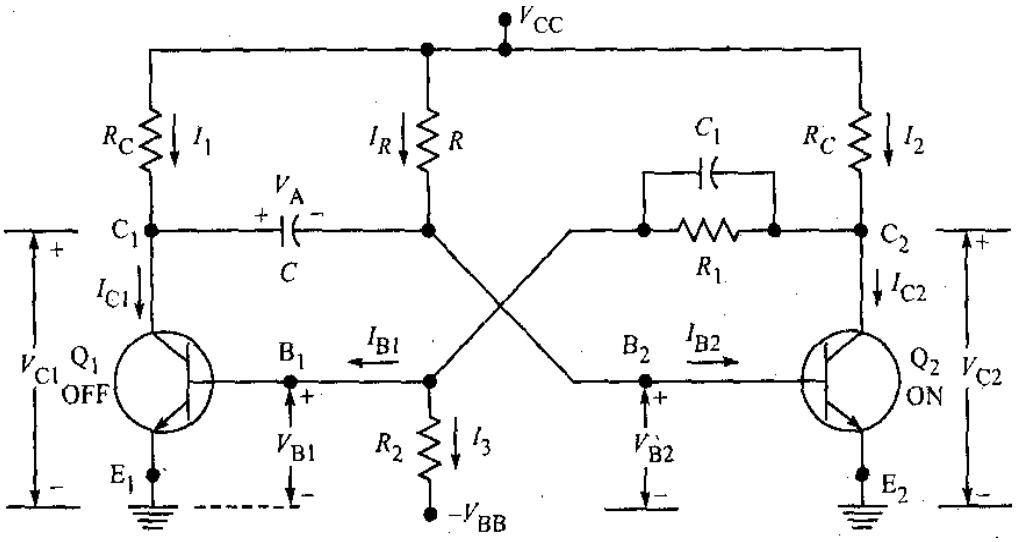


Figure 2.4 Circuit diagram of a collector-coupled monostable multivibrator.

Figure 2.4 shows the circuit diagram of a collector-to-base coupled (simply called collector- coupled) monostable multivibrator using n-p-n transistors. The collector of Q2 is coupled to the base of Qi by a resistor R} (dc coupling) and the collector of Qt is coupled to the base of Q2 by a capacitor C (ac coupling). Ci is the commutating capacitor introduced to increase the speed of operation. The base of Qi is connected to -VBB through a resistor R2, to ensure that Q1 is cut off under quiescent conditions. The base of Q2 is connected to Vcc through R to ensure that Q2 is ON under quiescent conditions. In fact, R may be returned to even a small

positive voltage but connecting it to Vcc is advantageous. The circuit parameters are selected such that under quiescent conditions, the monostable multivibrator finds itself in its permanent stable state with Q2ON (i.e. in saturation) and Q1 OFF (i.e. in cut-off). Multivibrator may be induced to make a transition out of its stable state by the application of a negative trigger at the base of Q2 or at the collector of Q1.

Monostable multivibrator as a voltage-to-time converter

Fig.2.5 shows the circuit diagram of a Monostable multivibrator as a voltage- to-time converter. By varying the auxiliary supply voltage V, the pulse width can be changed. It can be seen that the resistor R is connected to the auxiliary voltage source V.

The waveform of the voltage vB2 at the base of Q2 is shown in Fig.2.6.

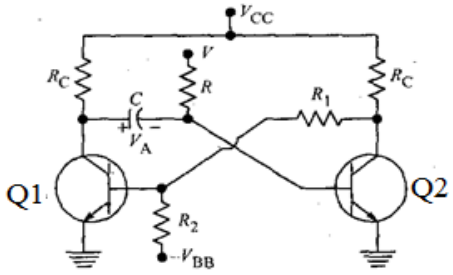


Fig.2.5: Monostable multivibrator as a voltage-to-time converter

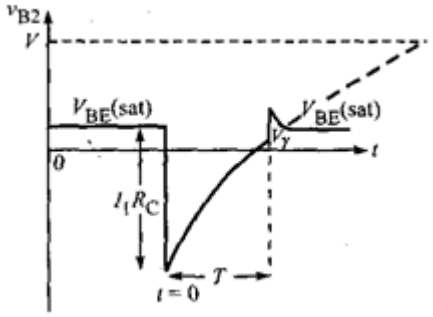


Fig.2.6: waveform of the voltage vB2 at the base of Q2

To identify the voltage across base of Q2

In the interval 0 < t < T, VB2 is given by

$$V_{B2} = V_f - (V_f - V_{in})e^{-t/\tau}$$

$$V_{B2} = V - (V - (-V_{CC})e^{-t/\tau}$$

$$V_{B2} = V - (V + V_{CC})e^{-t/\tau}$$

At t = T, VB2 = Vγ=0

$$0 = V - (V + V_{CC})e^{-t/\tau}$$

$$V = (V + V_{CC})e^{-t/\tau}$$

$$e^{-t/\tau} = \frac{V}{(V + V_{CC})}$$

$$t/\tau = \log(1 + \frac{V_{CC}}{V})$$

$$T = \tau \log(1 + \frac{V_{CC}}{V})$$

Where τ=RC, then

$$T = R C \log(1 + \frac{V_{CC}}{V})$$

VCC, R & C being fixed, it is seen from the above relationship that as V changes, T also Changes. Thus, the pulse width is a function of the auxiliary voltage v. For this reason, the monostable multi is called as voltage to time converter.

Triggering of Monostable Multivibrator

A monostable multivibrator needs to be triggered by a suitable signal in order to switch it from the stable state to the quasi stable state. However after remaining in the quasi stable state for a time $T = 0.693\ RC$, it automatically switches back to the original stable state, without any triggering signal applied. Thus unlike a bistable multivibrator, a monostable multivibrator requires only one triggering signal. Hence only unsymmetrical triggering techniques are adopted for monostable multivibrators. Generally speaking, all the triggering methods which are applicable to the binary are also applicable to the monostable multivibrator. The collector-coupled monostable multivibrator is normally triggered by applying a negative pulse at the collector of the OFF transistor (n-p-n) Q1 through an *RC* differentiator circuit which converts it into positive and negative spikes as shown in Figure 4.50. The positive spike is blocked by the diode and the negative spike is transmitted through it and the capacitor C to the base of the ON transistor Q_2. So Q_2 goes to the OFF state and Q1 to the ON state. This method has two advantages: one is as we know; the multivibrator is more sensitive to a pulse of such a polarity which brings the ON device to the OFF state. The second is, at the instant of the transition, the collector of Q1 drops, the diode no longer conducts, and the multivibrator does not respond to the triggering signal till the quasi-stable state is completed. The emitter-coupled monostable multivibrator may be triggered by applying a positive pulse of sufficient amplitude at the base of Q2 to bring the OFF transistor Q! to the ON state as shown in Figure 2.5.

Astable Multivibrator

As the name indicates an astable multivibrator is a multivibrator with no permanent stable state. Both of its states are quasi stable only. It cannot remain in any one of its states indefinitely and keeps on oscillating between its two quasi stable states the moment it is connected to the supply. It remains in each of its two quasi stable states for only a short designed interval of time and then goes to the other quasi stable state. No triggering signal is required. Both the coupling elements are capacitors (ac coupling) and hence both the states are quasi stable. It is a free running multivibrator. It generates square waves. It is used as a master oscillator.

COLLECTOR-COUPLED ASTABLE MULTIVIBRATOR

Fig.2.7 shows the circuit diagram of a collector-coupled astable multivibrator using n-p-n transistors. The collectors of both the transistors Q1 and Q2 are connected to the bases of the other transistors through the coupling capacitors Cs and C2. Since both are ac couplings, neither transistor can remain permanently at cut-off. Instead, the circuit has two quasi-stable states, and it makes periodic transitions between these states. Hence it is used as a master oscillator. No triggering signal is required for this multivibrator.

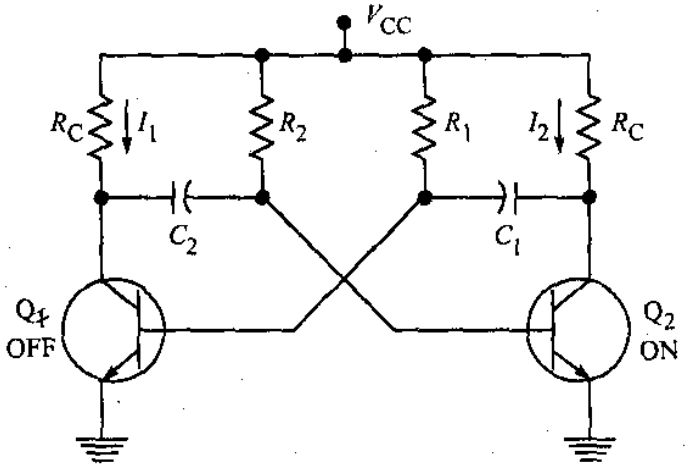


Fig.2.7: Collector Coupled Astable multivibrator

The waveforms at the bases and collectors for the astable multivibrator are shown in Fig.2. Let us say at t = 0, Q2 goes to ON state and Q1 goes to OFF state. So, for t < 0, Q2 was OFF and Q1 was ON. Hence for t < 0, V_{B2} is negative, V_{C2} = Vcc, $V_{B1} = V_{BE(sat)}$ and $V_{c1} = V_{CE(sat)}$. The capacitor C2 charges from V_{CC} through R2 and V_{B2} rises exponentially towards $V_{CC.}$

The cycle of events repeats and the circuit keeps on oscillating between its two quasi-stable states. Hence the output is a square wave. It is called a square wave generator or square wave oscillator or relaxation oscillator.

It is a free running oscillator.

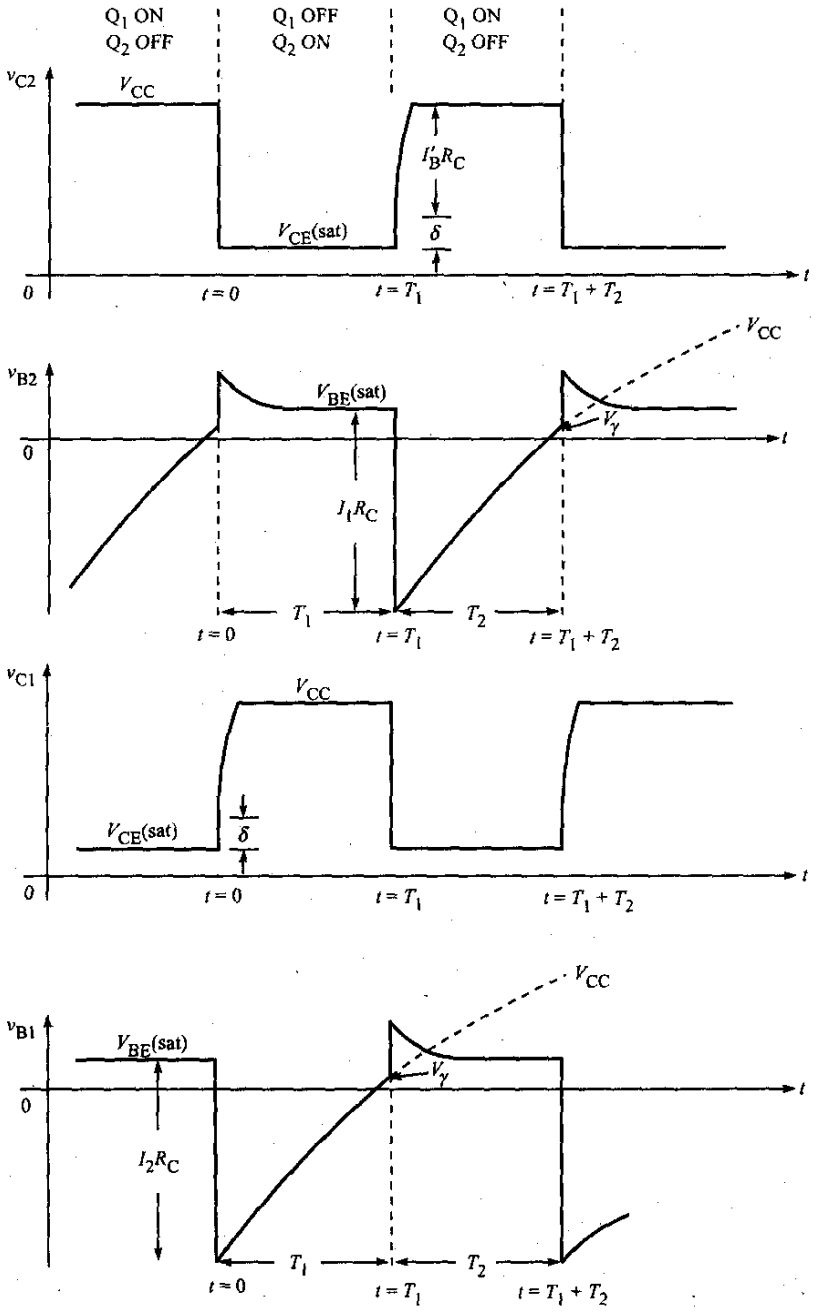


Fig.2.8: waveforms at the bases and collectors of astable Multi

Expression for T:

$$V_B = V_f - (V_f - V_{in})e^{-t/\tau}$$

Let $V_{in} = -V_{CC}$, $V_f = V_{CC}$

Substitute and calculate T1 & T2

From the above analysis

$T1= 0.69R_1C_1$

$T2= 0.69R_2C_2$

Hence the total time period is represented by

$T=T1+T2$

$T=0.69R_1C_1+0.69R_2C_2$

$T= 0.69(R_1C_1+ R_2C_2)$

The total oscillations of astable multi is

$f= 1.38RC$ (if $R_1C_1=R_2C_2$)

Voltage-to-Frequency Converter:

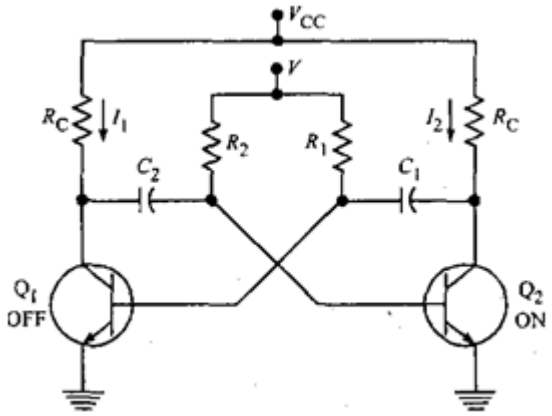


Fig.2.9: Voltage-to-Frequency Converter

Fig.2.9 shows the circuit diagram of an astable multivibrator used as a voltage-to-frequency converter. The frequency can be varied by varying the magnitude of the auxiliary voltage source V.

For $0 < t < T1$, Q1 is OFF and Q2 is ON.

Initial value of $V_B = V_{IN} = -V_{CC}$

Final Value of $V_B = V_f = V$

The exponentially rising voltage V_B is expressed as

$$V_B = V_f - (V_f - V_{in})e^{-t/R_2C_2}$$

$$= V - (V + V_{CC})e^{-t/R_2C_2}$$

At t= T2, we have $V_B=V\gamma=0$.

$$0 = V - (V + V_{CC})e^{-T2/R_2C_2}$$

$$T2 = R_2 C_2 \log\left(1 + \frac{V_{CC}}{V}\right)$$

Similarly

$$T1 = R_1 C_1 \log\left(1 + \frac{V_{CC}}{V}\right)$$

Total time period T= T1+T2

$$T = (R_1 C_1 + R_2 C_2) \log\left(1 + \frac{V_{CC}}{V}\right)$$

Hence the oscillations are expressed as

$$f = \frac{1}{2RC \log\left(1 + \frac{V_{CC}}{V}\right)}$$

UNIT-III
SAMPLING GATES &TIME BASE GENERATORS

INTRODUCTION:

A sampling gate is a transmission circuit that faithfully transmits an input signal to the output for a finite time duration which is decided by an external signal, called a gating signal (normally rectangular in shape), as shown in Fig.1.

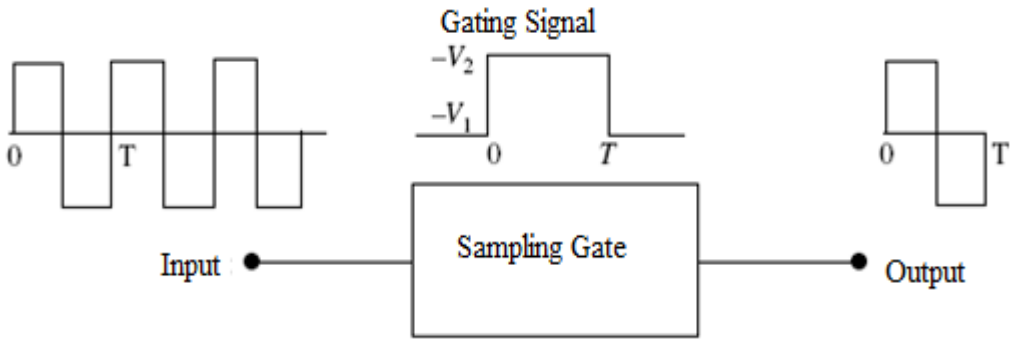


Fig. 3.1: Sampling gate

The input appears without a distortion at the output, but is available for a time duration T and after wards the signal is zero. They can transmit more number of signals. The main applications of the sampling gates are Multiplexers, choppers, D/A converter, sample and hold circuits, etc.

Earlier, we had seen logic gates in which the output, depending on the input conditions, is either a 1 level or a 0 level. That is, the inputs and outputs are discrete in nature. In a sampling gate, however, the output is a faithful replica of the input. Hence, sampling gates are also called linear gates, transmission gates or time selection circuits.

Basic Principle of Sampling Gate:

Linear gates can use either a series switch, as shown in Fig. 3.2 or a shunt switch, as shown in Fig. 3.3. In Fig. 3.2, only when the switch closes, the input signal is transmitted to the output. In Fig. 3.3, only when the switch is open the input is transmitted to the output.

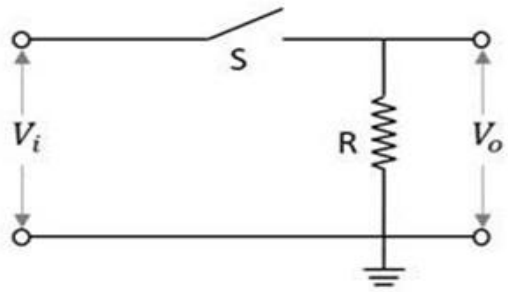


Fig.3.2 Series switch

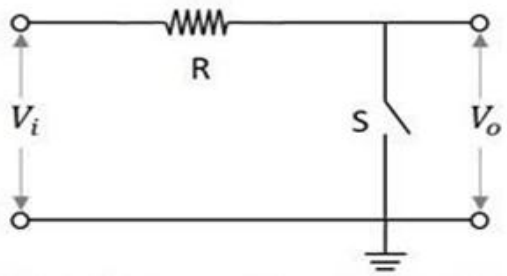


Fig.3.3 Shunt Switch

Sampling Gate using a Series Switch

In this type of switch, if the switch S is closed, the output will be exactly equal or proportional to the input. That time period will be the **Transmission Period**.

If the switch S is open, the output will be zero or ground signal. That time period will be the **Non-transmission Period**.

Sampling Gate using a Shunt Switch

In this type of switch, if the switch S is closed, the output will be zero or ground signal. That time period will be the **Non-transmission Period**.

If the switch S is open, the output will be exactly equal or proportional to the input. That time period will be the **Transmission Period**.

The sampling gates are entirely different from logic gates of digital circuits. They are also represented by pulses or voltage levels. But they are digital gates and their output is not the exact replica of the input. Whereas the sampling gate circuits are the analog gates whose output is exact replica of the input.

Classification of sampling gates:

Sampling gates can be of two types:

1. Unidirectional gates: These gates transmit the signals of only one polarity.
2. Bidirectional gates: These gates transmit bidirectional signals (i.e., positive and negative signals).

Unidirectional Diode Sampling Gate:

A unidirectional gate can transmit either positive or negative pulses (or signals) to the output. It means that this gate transmits pulses of only one polarity to the output. The signal to be transmitted to the output is the input signal. This input signal is transmitted to the output only when the control signal enables the gate circuit. Therefore, we discuss two types of unidirectional diode gates, namely, unidirectional diode gates that transmit positive pulses and unidirectional diode gates that transmit negative pulses.

A unidirectional sampling gate circuit consists of a capacitor C, a diode D and two resistors R1 and RL. The signal input is given to the capacitor and the control input is given to the resistor R1. The output is taken across the load resistor RL. The circuit is as shown below fig.3.4.

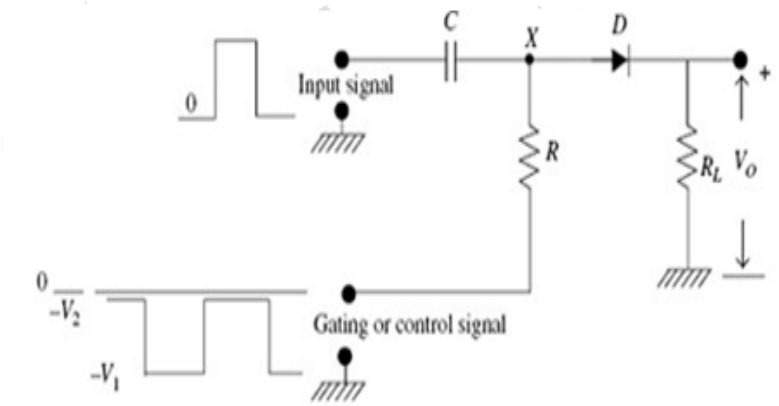


Fig. 3.4 Unidirectional Sampling Gate

According to the functioning of a diode, it conducts only when the anode of the diode is more positive than the cathode of the diode. If the diode has positive signal at its input, it conducts. The time period in which the gate signal is ON, is the transmission period. Hence it is during that period in which the input signal is transmitted. Otherwise the transmission is not possible.

Consider the instant at which the gating signals is –V1, which is a reasonably large negative voltage. As a result, D is OFF. Even if a positive input pulse is present when the gating signal with value – V1 is present, the diode D remains OFF since the input may not be sufficiently large to forward- bias it. Hence, the output is zero.

Now consider the duration when the gate signal has a value –V2 (smaller negative value) and when the input is also present (coincidence occurs). Assume that the control signal has peak-to- peak swing of 25 V and the signal has peak-to-peak swing of 15 V.

1) Let, for example, −V1 = −40 V, − V2 = −15 V and the signal amplitude be 15 V, as shown in Fig. 3.5. The net voltage at the anode of the diode, when the input is present for the duration of the gating signal, is 0. The diode is OFF and the output in this case is zero.

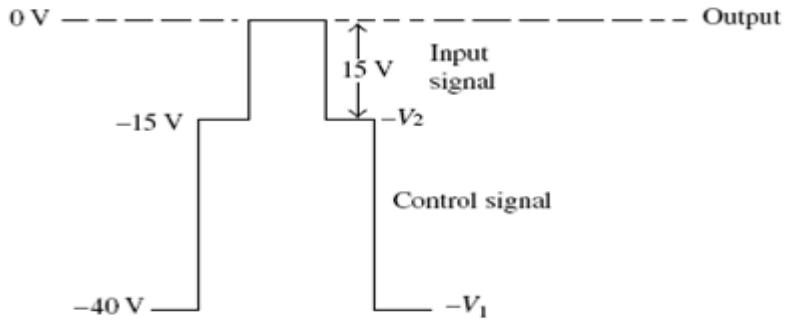


Fig.3.5: The control signal with $-V1 = -40$ V, $-V2 = -15$ V and the input amplitude 15 V

2. Now, change the levels to −V1 = −35 V, − V2 = −10 V and the signal amplitude remains constant at 15 V, as shown in Fig. 3.6. Only when the input forward-biases the diode, there is an output. The output in this case is a pulse of amplitude 5 V (assuming an ideal diode). The duration of the output is the same as the duration of the input signal.

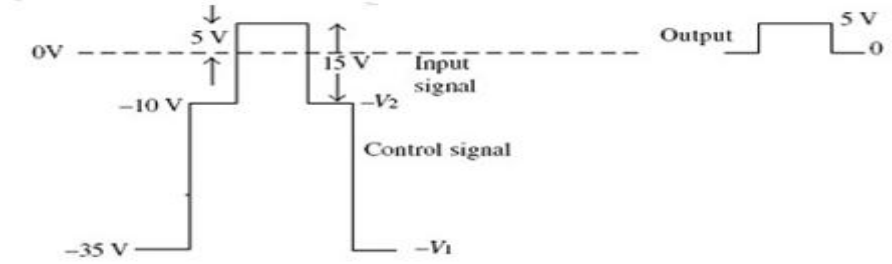


Fig.3.6: The control signal with $V1 = -35$ V, $-V2 = -10$ V and the input amplitude 15 V

3. Now let −V1 = −30 V, − V2 = −5 V and the signal amplitude be 15 V, as shown in Fig.3.7. As the signal above the zero level is 10 V, the output is a pulse of amplitude 10 V and has the same duration as the input.

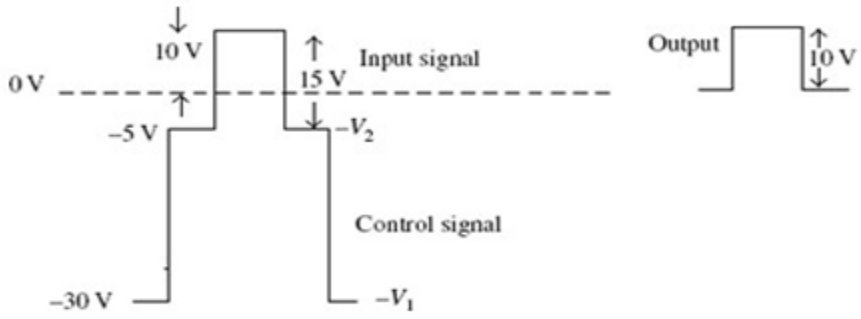


Fig.3.7: The control signal with $V1 = -30$ V, $-V2 = -5$ V and the input amplitude 15 V

4. Let −V1 = −25 V, − V2 = 0 V and the signal amplitude be 15 V, as shown in Fig.3.8. The output in this case is 15 V and has the same duration as the input.

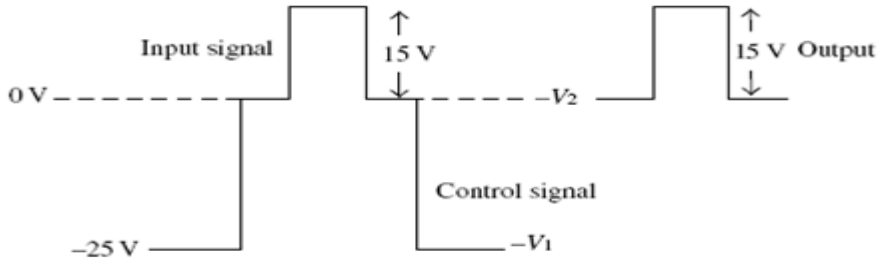


Fig.3.8: The control signal with $V1 = -25$ V, $-V2 = 0$ V and the input amplitude 15 V

5. Let −V2 = +5 V and − V1 = −20 V, as shown in Fig.3.9. In this case, the output not only contains the input but also a portion of the control signal. The desired signal at the output is seen to be riding over a pedestal. We see that the output of the gate changes by adjusting –V2 and in the last case it is seen that the output is superimposed on a pedestal of 5 V. Thus, the output is influenced by the control signal.

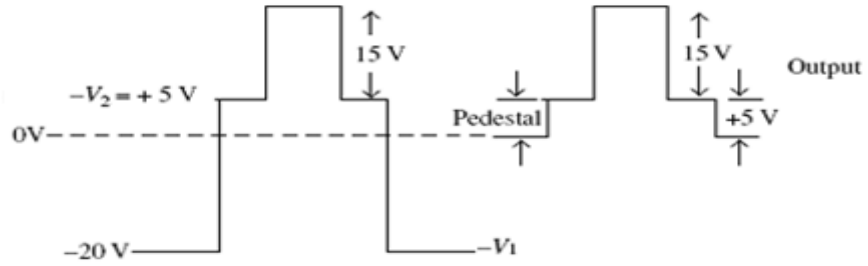


Fig.3.9: The control signal with $V1 = -20$ V, $-V2 = 5$ V and the input amplitude 15 V

For a gating signal, the RC network behaves as an integrator. Hence, the gate signal is not necessarily a rectangular pulse but rises and falls with a time constant RC. As a result, there is a distortion in the gate signal. However, if the duration of the input signal (a pulse) is much smaller than the duration of the gate, this distortion associated with the gating signal is not necessarily transmitted to the output, and the output is a sharp pulse as desired, provided the pedestal is eliminated, as shown in Fig. 3.10. On the contrary, if there is a pedestal, there is a corresponding distortion in the output, as shown in Fig.3.11.

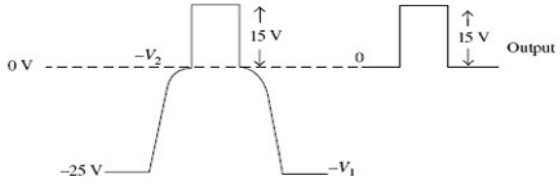


Fig.3.10: There is no distortion in the output through the control signal is distorted

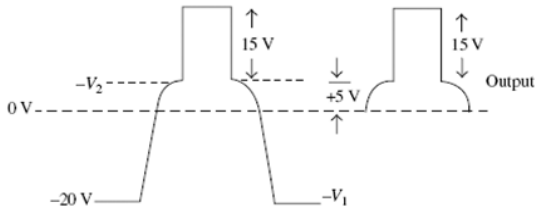


Fig.3.11: The distorted gate signal giving rise to a distorted pedestal.

Two input unidirectional sampling gate:

Two input unidirectional sampling gate is shown in below fig 3.12.

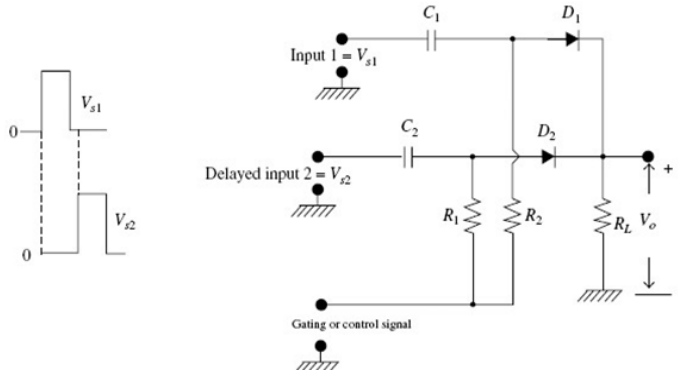


Fig.3.12: Two input unidirectional sampling gate

Let $V_{S}1$ and $V_{S}2$ be the pulses of amplitude 5 V. When both these signals appear at the input simultaneously, having the same duration, the output is shown in Fig. 3.13, when $-V1 = -25$ V and $-V2 = 0$.

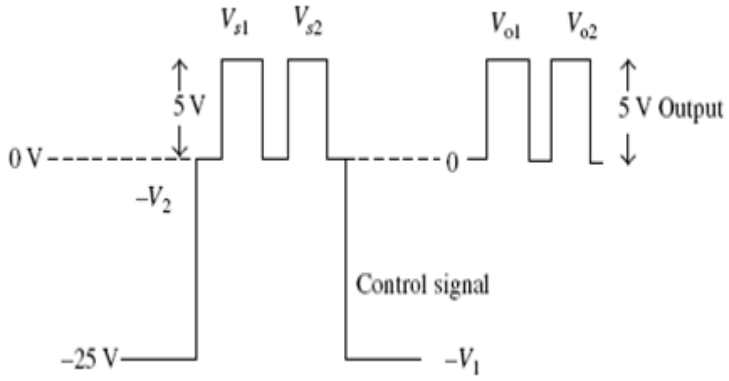


Fig.3.13: The waveforms of a two-input unidirectional gate.

When the control signal is at $-V2$ (= 0 V), and if both the inputs are 0 the output is zero. When the inputs are above 0, the output is 5 V. However, when the control input is at $-V1$ (−25 V), no output is available. This negative control signal inhibits the gate. Hence, this circuit is a two-input OR gate with $-V1$ (−25 V) and inhibiting the gate operation.

Bidirectional Sampling Gates:

A basic bidirectional sampling gate consists of a transistor and three resistors. The input signal voltage VS and the control input voltage VC are applied through the summing resistors to the base of the transistor. The circuit diagram given below shows the bidirectional sampling gate using transistor.

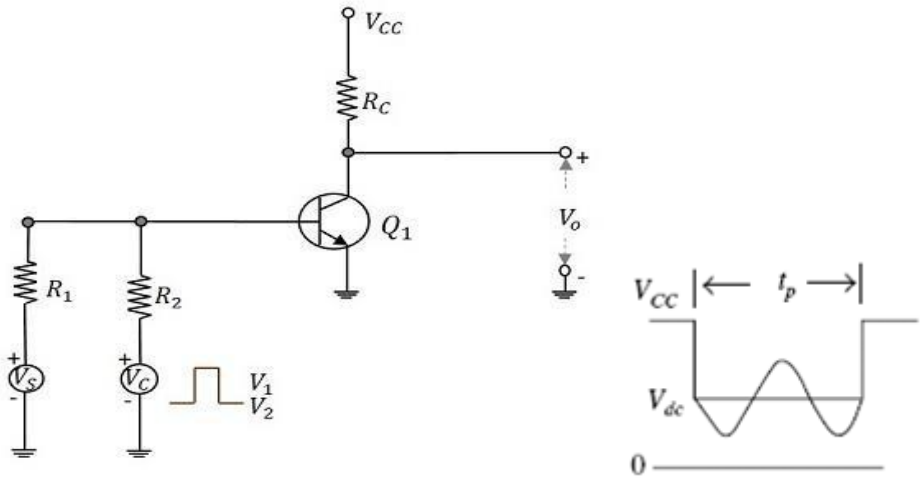


Fig.3.14: Bidirectional sampling gate using transistors

The control input VC applied here is a pulse waveform with two levels V1 and V2 and pulse width tp. This pulse width decides the desired transmission interval. The gating signal allows the input to get transmitted. When the gating signal is at its lower level V2, the transistor goes into active region. So, until the gating input is maintained at its upper level, signals of either polarity, which appear at the base of the transistor will be sampled and appear amplified at the output.

Two-transistor Bidirectional Sampling Gates:

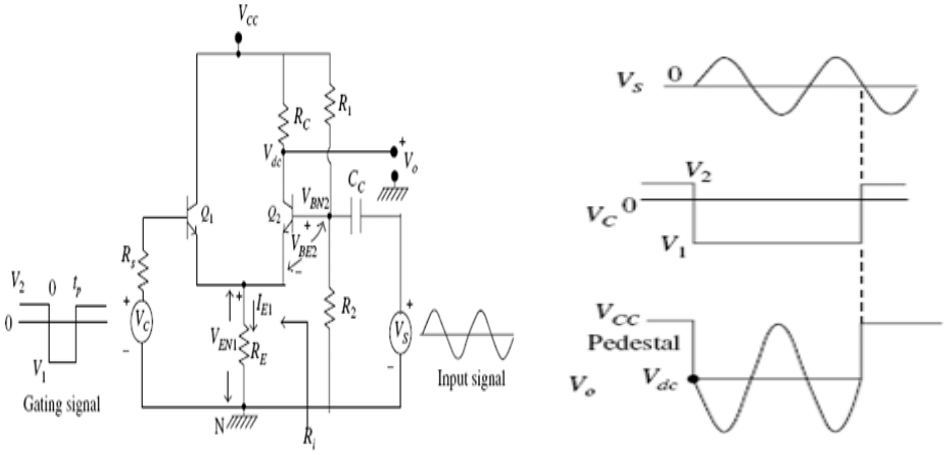


Fig.3.15: Two-transistor Bidirectional Sampling Gates with waveforms

The Fig. 3.15 Shows another bidirectional transistor gate where two devices Q1 and Q2 are used and the

control signal and the input signal are connected to the two separate bases.

There is no external dc voltage connected to the base of Q1, only the gating signal VC is connected. Let the control voltage be at its upper level, V2. Then, Q1 is ON and there is sufficient emitter current IE1 which results in VEN1 across RE. Q2 is biased to operate in the active region using R1 and R2. The voltage at the base of Q2 with respect to its emitter (VBE2) is (VBN2 − VEN1). If this voltage is sufficient enough to reverse-bias the base emitter diode of Q2, then Q2 is OFF. There is no output signal, but only a dc voltage VCC is available. However, when the gating signal is at its lower level V1, Q1 is OFF and Q2 operates in the active region and can also operate as an amplifier. If an input signal is present, there is an amplified output Vo. The presence of RE increases the input resistance Ri and thus, the signal source is not loaded.

From the waveforms shown in Fig. 3.15. It is seen that the output is VCC when Q2 is OFF. When the gating signal drives Q1 OFF and Q2 ON, the dc voltage at the collector of Q2 falls to V_{dc} (a voltage much smaller than VCC). During the period of the gating signal, the input signal is amplified and phase inverted by Q2 and is available at the output. Again at the end of the gating signal Q2 goes OFF and V_O jumps to VCC. Hence, the signal is superimposed on a pedestal.

Two Diode Bidirectional Sampling Gate:

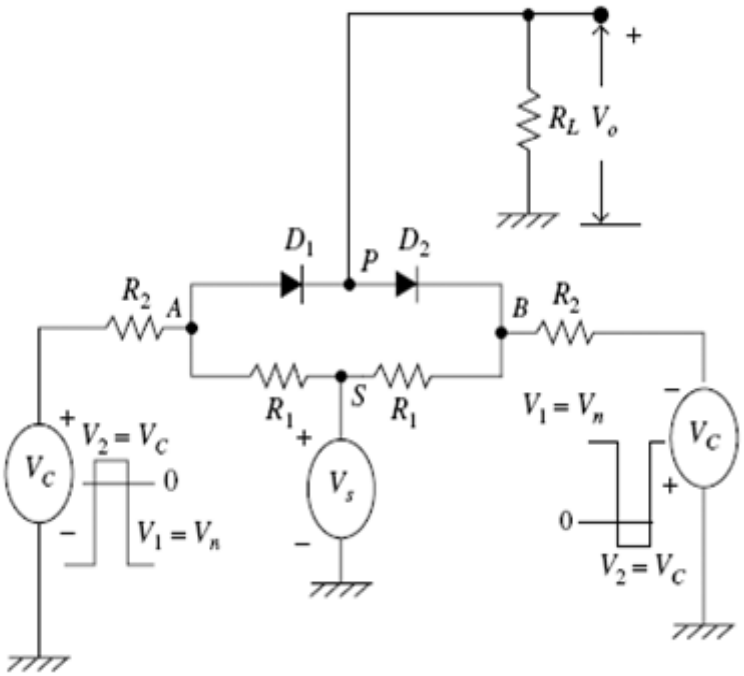


Fig.3.16: Two Diode bidirectional sampling gate

The above circuit consists of two symmetrical gate signals +Vc and –Vc. When the gate voltage levels are such that the voltage at point A is –ve (-Vc) and at point B is +ve (+Vc), then the both diodes are reverse biased and hence there is no transmission of signals. when the gate voltages are such that ythe voltage at point A is +ve (+Vc) and the voltage at point B is –ve(-Vc) the both diodes D1 and d2 are ON, As a result there is a transmission of input signal for the duration of gate pulses.

The equivalent circuit to calculate voltage at node A due to Vs source

$$v_{th\,A1} = \frac{R2}{R1 + R2} Vs = \alpha Vs$$

The equivalent circuit to calculate voltage at node A due VC source

$$v_{th\,2} = \frac{R1}{R1 + R2} Vc = \left(1 - \frac{R2}{R1 + R2}\right) Vc = (1 - \alpha) Vc$$

We have Rth1 = Rth2.

Similarly, considering the circuit when a negative signal is transmitted to the output when D2is ON and combining the equivalent circuits of the two halves, we finally have the circuit shown in Fig. 3.17.

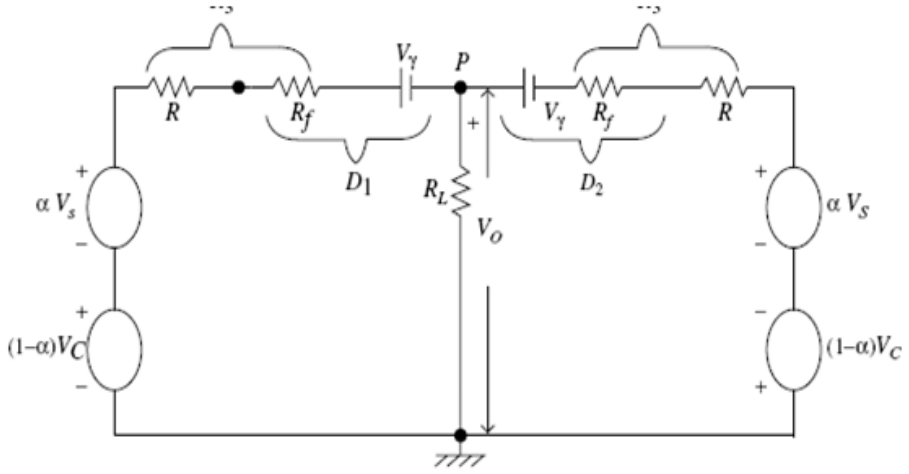


Fig.3.17: Equivalent circuit of Two Diode Bidirectional sampling Gate

Let R3 = R + R_f

Where α = R2 / R1+R2

We shall now define the gain of the transmission gate A (strictly speaking this is attenuation) as the ratio of Vo/Vs during transmission period. The control and small diode voltages do not contribute to any current in RL, the resultant simplified circuit is shown in Fig. 3.18.

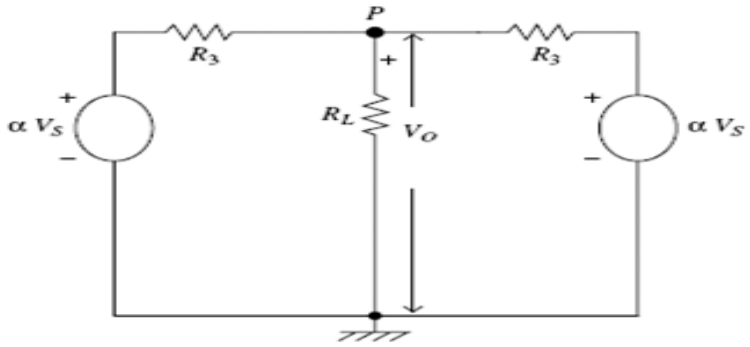


Fig.3.18: The simplified circuit of Fig. 3.16

The open circuit voltage between P and the ground is αVs and the Thevenin resistance is R3/2, as shown in Fig.3.19

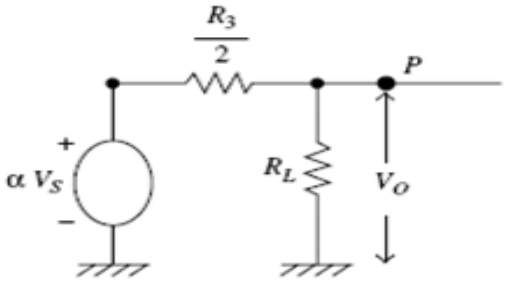


Fig.3.19 The circuit that enables the calculation of gain A

$$V\,0 = \alpha Vs \frac{Rl}{Rl + \frac{R\,3}{2}}$$

$$A = \frac{V\,0}{Vs} = \alpha \frac{Rl}{Rl + \frac{R\,3}{2}}$$

Therefore,

$$A = \frac{V\,0}{Vs} = \frac{R\,2}{R1 + R\,2} \frac{Rl}{Rl + \frac{R\,3}{2}}$$

Determination of Minimum Positive Control Voltage.

Minimum control voltage $V_{CP\ (min)}$ required to keep both the diodes *D*1 and *D*2ON: Let only the gating signals be present. The amplitude and polarity of the gating signals are such that both the diodes *D*1 and *D*2 conduct, and equal currents flow in these two diodes. When these equal and opposite currents flow in *RL*, the net voltage drop is zero and there is no pedestal. Let *Vs* be a positive signal. As the amplitude of the signal

goes on increasing, the current in $D1$goes on increasing and that in $D2$ goes on decreasing. As V_S increases further, the current in D2becomes zero (i.e., D2 is OFF). Thus, there is a minimum control voltage VC that will keep both the diodes ON. To calculate this $V_{CP\ (min)}$, let it be assumed that D2 has just stopped conducting i.e., the diode current has become zero, the drop across R3 is zero. Therefore, the output voltage across RL is the open circuit voltage, as shown in Fig. 3.20.

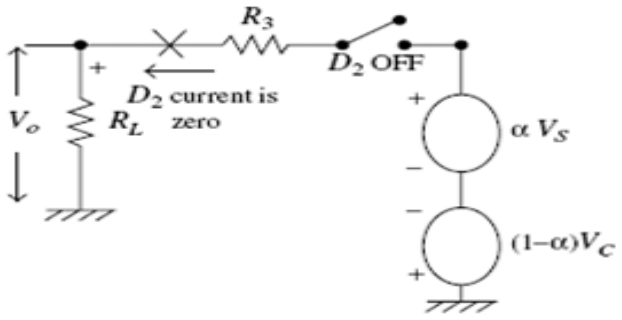


Fig.3.20: The voltage Vo when D2 is OFF

V0 = αVs – (1-α)Vc-------(1)

Now, calculating the output due to the left hand side signal source Vs and control signal (1 −α)VC, with the assumption that Vγ ≪ Vs (i.e., Vr ≈0), as shown Fig. 3.21.

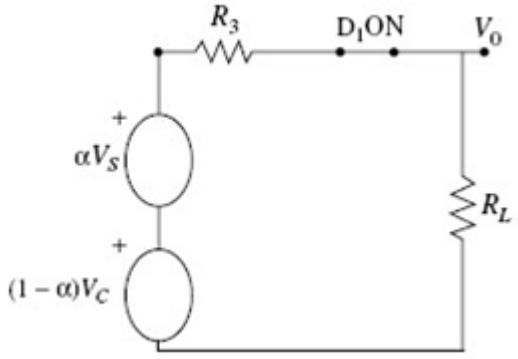


Fig.3.21: The voltage Vo when D1 is ON

From the above figure V0 is

$$V\,0 = \alpha Vs + (1-\alpha)Vc\,(\frac{Rl}{Rl + R3})$$

Now equate the equation 1 and above equation

$$V0 = \alpha Vs - (1-\alpha)\,Vc = \alpha Vs + (1-\alpha)Vc\,(\frac{Rl}{Rl + R3})$$

From the above equation identify the Vcp_{min}

Then

$$vcp_{\min} = \frac{R2}{R1} \times \left(\frac{R3}{R3 + 2Rl} \right) Vs$$

Note: $V_{Cp\,(min)}$ decreases with increasing RL.

Determination Of Minimum Negative Control Voltage:

To calculate the minimum control voltage Vcn(min) i.e., required to keep D1 and D2 OFF when no transmission takes place. If both the diodes are reverse-biased, the output voltage at point P is zero and P is at the ground potential, shown in Fig. 3. As D1 is reverse-biased, it behaves as an open circuit. As a result, the input appears at the output.

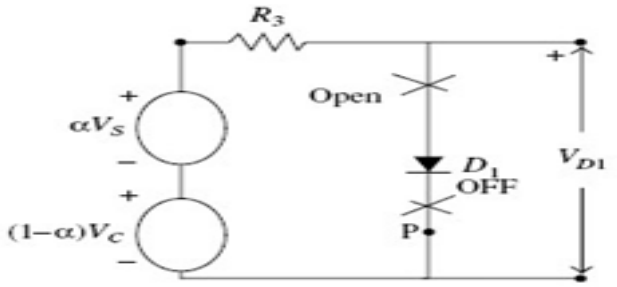


Fig.3.22: The gate circuit when D1 and D2 are reverse-biased

VD1 = Voltage across D1 = [αVs + (1 − α)VC]

If Vcn is the magnitude of VC at the lower level,

VD1 = [αVs + (1 − α)Vn]

For D1 to be OFF, VD1 must be either zero or negative. If VD1 is zero,

[αVs + (1 − α)Vn] =0

$$\text{Vcn} = \text{Vcn(min)} = \frac{\alpha}{1-\alpha} Vs$$

Therefore,

$$\text{Vcn(min)} = \frac{R2}{R1} \text{Vs}$$

Input Resistance:

The purpose of the control signal is to enable the gate and the current drawn from the signal source does not depend on the control voltage. This current depends on the state of the diodes, whether they are ON or OFF. Here we assume that *D*1 and *D*2 as ideal diodes.

(i) When *D*1 and *D*2 are OFF

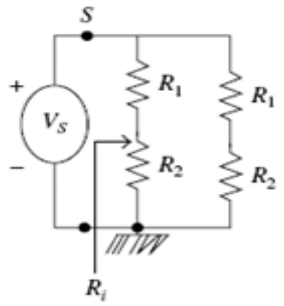


Fig.3.23 : when D1 and D2 are OFF

Ri = (R1+R2) || (R1+R2)

Then Ri = (R1+R2)/2

(ii) When D1 and D2 are ON

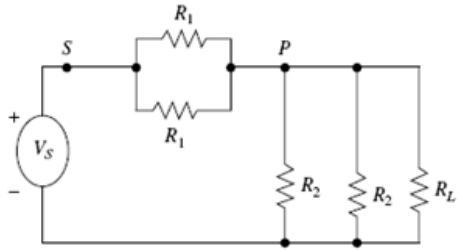


Fig.3.24: when D1 and D2 are ON

Where R1, R1 are parallel

Then equivalent resistance is R1/2.

From fig.5 R2, R2 & RL are parallel

Then total resistance is

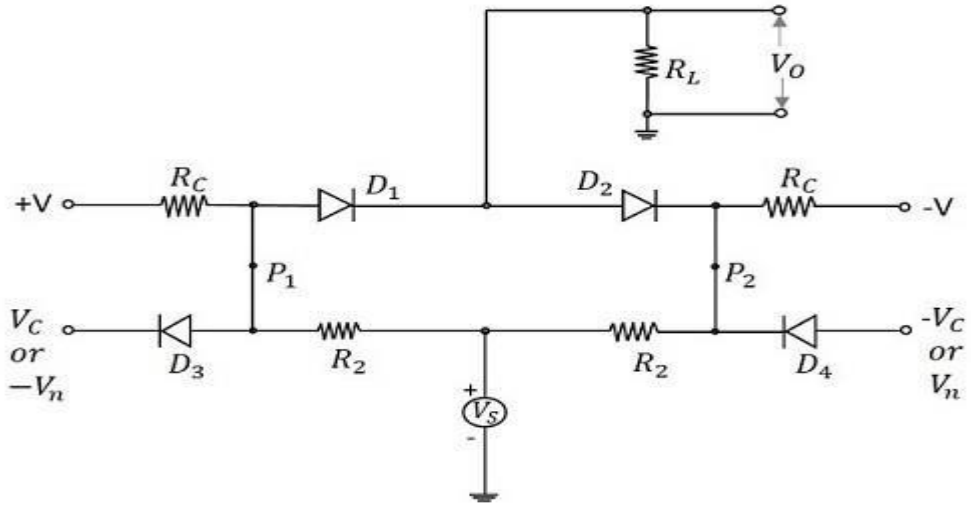
$$Ri = \left(\frac{R2\,Rl}{R2 + Rl} \right) \times \left(\frac{R1}{2} \right)$$

Four Diode Bidirectional Sampling Gate:

Bidirectional sampling gate circuit is made using diodes also. A two diode bidirectional sampling gate is the basic one in this model. But it has few disadvantages such as

- It has low gain
- It is sensitive to the imbalances of control voltage
- $V_{n\,(min)}$ may be excessive
- Diode capacitance leakage is present

A four diode bidirectional sampling gate was developed, improving these features. A two bidirectional sampling gate circuit was improved adding two more diodes and two balanced voltages +v or –v to make the circuit of a four diode bidirectional sampling gate as shown in the figure.



The control voltages V_C and $–V_C$ reverse bias the diodes D_3 and D_4 respectively. The voltages +v and –v forward bias the diodes D_1 and D_2 respectively. The signal source is coupled to the load through the resistors R_2 and the conducting diodes D_1 and D_2. As the diodes D_3 and D_4 are reverse biased, they are open and disconnect the control signals from gate. So, an imbalance in control signals will not affect the output.

When the control voltages applied are V_n and $–V_n$, then the diodes D_3 and D_4 conduct. The points P_2 and P_1 are clamped to these voltages, which make the diodes D_1 and D_2 revere biased. Now, the output is zero. During transmission, the diodes D_3 and D_4 are OFF. The gain A of the circuit is given by

$$A=R_CR_C+R2\times R_LR_L+(R_s/2)$$

Hence the choice of application of control voltages enables or disables the transmission. The signals of either polarities are transmitted depending upon the gating inputs.

Introduction to sweep circuits, general features of a time base signal:

A time-base generator is an electronic circuit which generates an output voltage or current waveform, a portion of which varies linearly with time. Ideally the output waveform should be a ramp. Time-base generators may be voltage time-base generators or current time-base generators. A voltage time-base generator is one that provides an output voltage waveform, a portion of which exhibits a linear variation with respect to time. A current time-base generator is one that provides an output current waveform, a portion of which exhibits a linear variation with respect to time. There are many important applications of time-base generators, such as in CROs, television and radar displays, in precise time measurements, and in time

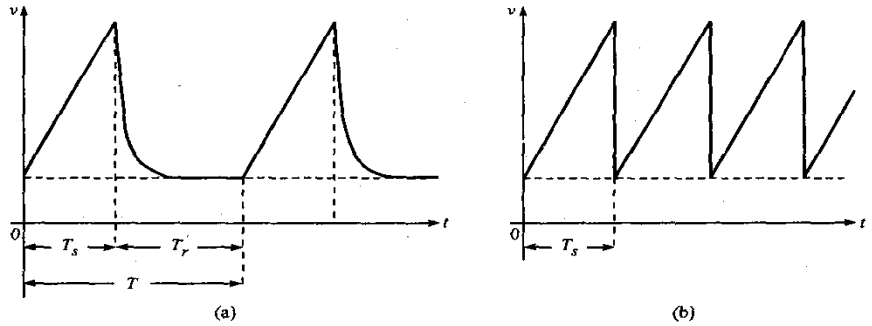
modulation. The most important application of a time-base generator is in CROs. To display the variation with respect to time of an arbitrary waveform on the screen of an oscilloscope it is required to apply to one set of deflecting plates a voltage which varies linearly with time. Since this waveform is used to sweep the electron beam horizontally across the screen it is called the *sweep voltage* and the time-base generators are called the *sweep* circuits.

General features of a time-base signal:

Figure (a) shows the typical waveform of a time-base voltage. As seen the voltage starting from some initial value increases linearly with time to a maximum value after which it returns again to its initial value. The time during which the output increases is called the sweep time and the time taken by the signal to return to its initial value is called the restoration time, the return time, or the fly back time. In most cases the shape of the waveform during restoration time and the restoration time itself are not of much consequence. However, in some cases a restoration time which is very small compared with the sweep time is required. If the restoration time is almost zero and the next linear voltage is initiated the moment the present one is terminated then a saw-tooth waveform shown in Figure (b) is generated.

The waveforms of the type shown in Figures (a) and (b) are generally called sweep waveforms even when they are used in applications not involving the deflection of an electron beam.

In fact, precisely linear sweep signals are difficult to generate by time-base generators and moreover nominally linear sweep signals may be distorted when transmitted through a coupling network.



Methods of generating a time-base waveform

In time-base circuits, sweep linearity is achieved by one of the following methods.

1. *Exponential charging.* In this method a capacitor is charged from a supply voltage through a resistor to a voltage which is small compared with the supply voltage.

2. *Constant current charging.* In this method a capacitor is charged linearly from a constant current source. Since the charging current is constant the voltage across the capacitor increases linearly.

3. *The Miller circuit.* In this method an operational integrator is used to convert an input step voltage into a ramp waveform.

4. *The Phantastron circuit.* In this method a pulse input is converted into a ramp. This is a version of the Miller circuit.

5. *The bootstrap circuit.* In this method a capacitor is charged linearly by a constant current which is obtained by maintaining a constant voltage across a fixed resistor in series with the capacitor.

6. *Compensating networks.* In this method a compensating circuit is introduced to improve the linearity of the basic Miller and bootstrap time-base generators.

7. *An inductor circuit.* In this method an *RLC* series circuit is used. Since an inductor does not allow the current passing through it to change instantaneously, the current through the capacitor more or less remains constant and hence a more linear sweep is obtained.

Unijunction Transistor:

As the name implies a UJT has only one p-n junction, unlike a BJT which has two p-n junctions. It has a p-type emitter alloyed to a lightly doped n-type material as shown in Figure 5.4(a). There are two bases: base B1 and base **B_2,** base B1 being closer to the emitter than base B_2. The p-n junction is formed between the p-type emitter and n-type silicon slab.

Originally this device was named as double base diode but now it is commercially known as UJT. The equivalent circuit of the UJT is shown in Figure 3.25 is the resistance between base B1 and the emitter, and it is basically a variable resistance, its value being dependent upon the emitter current is the resistance between base b2 and the emitter, and its value is fixed.

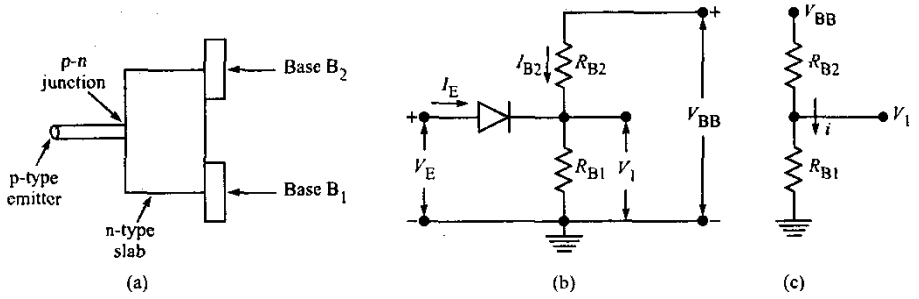


Figure 3.25 (a) Construction of UJT, (b) equivalent circuit of UJT, and (c) circuit when $i_E = 0$.

Sweep circuit using UJT

The supply voltage V_{yY} and the charging resistor *R* must be selected such that the load line intersects the input characteristic in the negative-resistance region. Assume that the UJT is OFF. The capacitor *C* charges from V_YY through *R*. When it is charged to the peak value V_P, the UJT turns ON and the capacitor now discharges through the UJT. When the capacitor discharges to the valley voltage V_v is UJT turns OFF, and again the capacitor starts charging and the cycle repeats.

Miller Sweep Generator:

The transistor Miller time base generator circuit is the popular Miller integrator circuit that produces a sweep waveform. This is mostly used in horizontal deflection circuits. Let us try to understand the construction and working of a Miller time base generator circuit.

Construction of Miller Sweep Generator:

The Miller time base generator circuit consists of a switch and a timing circuit in the initial stage, whose input is taken from the Schmitt gate generator circuit. The amplifier section is the following one which has three stages, first being an emitter follower, second an amplifier and the third one is also an emitter follower.

An emitter follower circuit usually acts as a Buffer amplifier. It has a low output impedance and a high input impedance. The low output impedance lets the circuit drive a heavy load. The high input impedance keeps the circuit from not loading its previous circuit. The last emitter follower section will not load the previous amplifier section. Because of this, the amplifier gain will be high.

The capacitor C placed between the base of Q_1 and the emitter of Q_3 is the timing capacitor. The values of R and C and the variation in the voltage level of V_{BB} changes the sweep speed. The figure below shows the circuit of a Miller time base generator.

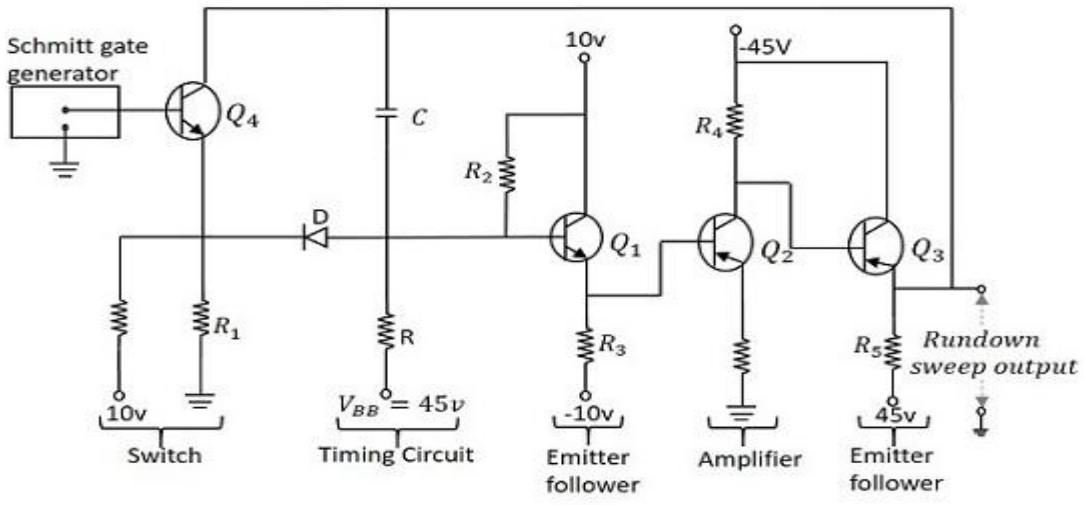


Figure 3.26: Miller Sweep Circuit

Operation of Miller Sweep Generator:

When the output of Schmitt trigger generator is a negative pulse, the transistor Q_4 turns ON and the emitter current flows through R_1. The emitter is at negative potential and the same is applied at the cathode of the diode D, which makes it forward biased. As the capacitor C is bypassed here, it is not charged.

The application of a trigger pulse, makes the Schmitt gate output high, which in turn, turns the transistor Q_4 OFF. Now, a voltage of 10v is applied at the emitter of Q_4 that makes the current flow through R_1 which also makes the diode D reverse biased. As the transistor Q_4 is in cutoff, the capacitor C gets charged from V_{BB} through R and provides a rundown sweep output at the emitter of Q_3. The capacitor C discharges through D and transistor Q_4 at the end of the sweep.

Considering the effect of capacitance C_1, the slope speed or sweep speed error is given by

$$es=VsV(1-A+RRi+CCi)$$

Applications:

Miller sweep circuits are the most commonly used integrator circuit in many devices. It is a widely used saw tooth generator.

Bootstap sweep circuit:

The boot strap time base generator circuit consists of two transistors, Q_1which acts as a switch and Q_2 which acts as an emitter follower. The transistor Q_1 is connected using an input capacitor C_B at its base and a resistor R_B through V_{CC}. The collector of the transistor Q_1 is connected to the base of the transistor Q_2. The collector of Q_2 is connected to V_{CC} while its emitter is provided with a resistor R_E across which the output is taken.

A diode D is taken whose anode is connected to V_{CC} while cathode is connected to the capacitor C_2 which is connected to the output. The cathode of diode D is also connected to a resistor R which is in turn connected to a capacitor C_1. This C_1 and R are connected through the base of Q_2 and collector of Q_1. The voltage that appears across the capacitor C_1 provides the output voltage V_o.

The following figure explains the construction of the boot strap time base generator.

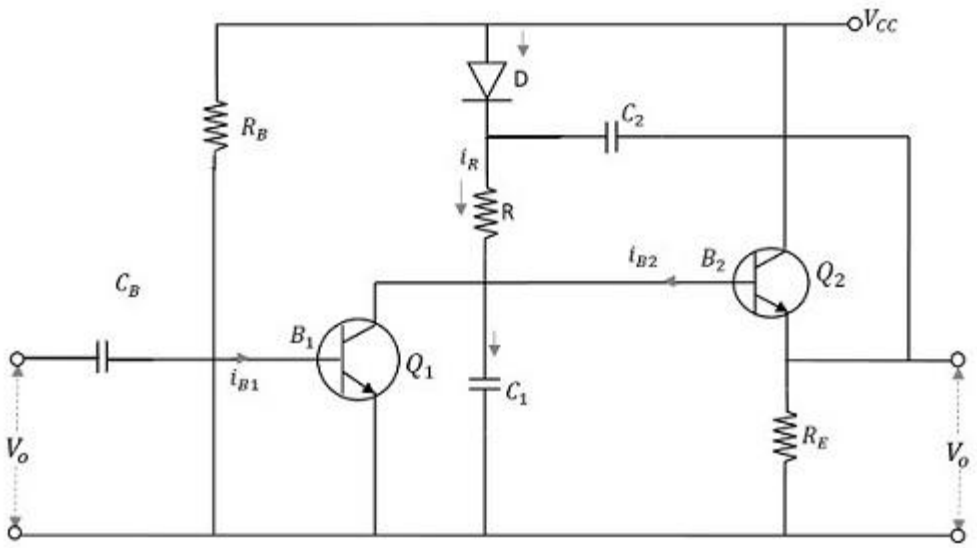


Figure 3.27: Bootstap sweep circuit

Operation of Bootstrap Time Base Generator

Before the application of gating waveform at t = 0, as the transistor gets enough base drive from V_{CC} through R_B, Q_1 is ON and Q_2 is OFF. The capacitor C_2 charges to V_{CC} through the diode D. Then a negative trigger pulse from the gating waveform of a Monostable Multivibrator is applied at the base of Q_1 which turns Q_1 OFF. The capacitor C_2 now discharges and the capacitor C_1 charges through the resistor R. As the capacitor C_2 has large value of capacitance, its voltage levels (charge and discharge) vary at a slower rate. Hence it discharges slowly and maintains a nearly constant value during the ramp generation at the output of Q_2.

During the ramp time, the diode D is reverse biased. The capacitor C_2provides a small current I_{C1} for the capacitor C_1 to charge. As the capacitance value is high, though it provides current, it doesn't make much difference in its charge. When Q_1 gets ON at the end of ramp time, C_1 discharges rapidly to its initial value. This voltage appears across V_O. Consequently, the diode D gets forward biased again and the capacitor C_2 gets a pulse of current to recover its small charge lost during the charging of C_1. Now, the circuit is ready to produce another ramp output.

The capacitor C2 which helps in providing some feedback current to the capacitor C1 acts as a boot strapping capacitor that provides constant current.

The output waveforms are obtained as shown in the following figure 3.28.

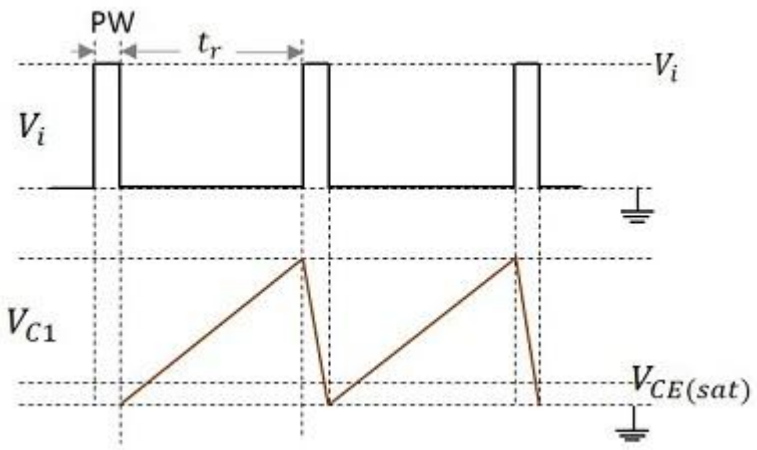


Figure 3.28: Output Waveforms

The pulse given at the input and the voltage V_{C1} which denotes the charging and discharging of the capacitor C_1 which contributes the output are shown in the figure above.

Advantage:

The main advantage of this boot strap ramp generator is that the output voltage ramp is very linear and the ramp amplitude reaches the supply voltage level.

UNIT – IV

SYNCHRONIZATION & FREQUENCY DIVISION

A pulse or digital system may involve several different basic waveform generators and the system may require that all these generators be operated synchronously—in step with one another, i.e. each one of them arrives at some reference point in the cycle at exactly the same time. Two or more waveform generators are said to operate in synchronism if each one of them arrives at some reference point in its cycle at the same time. Synchronization is the process of making two or more waveform generators arrive at some reference point in the cycle at exactly the same time. Synchronization may be on a one-to-one basis or with frequency division. Synchronization is said to be on a one-to-one basis if all the generators operate at exactly the same frequency and arrive at some reference point in the cycle exactly at the same time. Synchronization is said to be with frequency division if the generators operate at different frequencies which are integral multiples of each other but arrive at some reference point at the same time. The two processes, i.e. (i) synchronization and (ii) synchronization with frequency division are basically very nearly alike and no clear-cut distinction can be drawn between them. Counting circuits are an example of frequency division.

PULSE SYNCHRONIZATION OF RELAXATION DEVICES

Relaxation circuits are circuits in which the timing interval is established through the gradual charging of a capacitor, the timing interval being terminated by the sudden discharge (relaxation) of a capacitor. The multivibrator, the sweep generator, the blocking oscillator which we have discussed in earlier chapters are examples of relaxation circuits. All these circuits have in common a timing interval and a relaxation (or recovery) interval and each exists in an astable or monostable form. The mechanism of synchronization and frequency division is the same for all these devices.

In the monostable circuits the matter of synchronization is a trivial one. The monostable circuit normally remains in its quiescent condition and a single cycle of operation is initiated by the application of a triggering pulse. The only requirement is that the interval between triggers should be larger than the timing interval and the recovery period should be combined.

Figure 4.1 shows an arrangement for pulse synchronization of a sweep generator using UJT. In the absence of an external synch, signal, the capacitor stops charging when the voltage v_c reaches the peak or breakdown voltage V_P of the negative-resistance device. Thereafter, the capacitor discharges abruptly through the negative resistance device UJT. When the capacitor voltage v_c falls to the valley voltage Vy, the UJT goes OFF and the capacitor begins to recharge. A negative pulse applied at the base B_2 of the UJT will lower Vp. In fact, any current-controlled negative-resistance device such as a silicon-controlled switch, thyristor, etc. can be used in place of the UJT. In such a case, a positive pulse applied at the gate or base will lower the breakdown voltage.

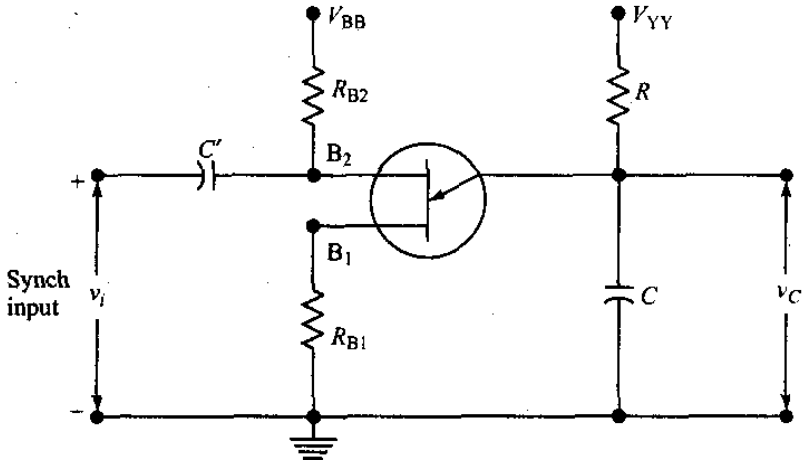
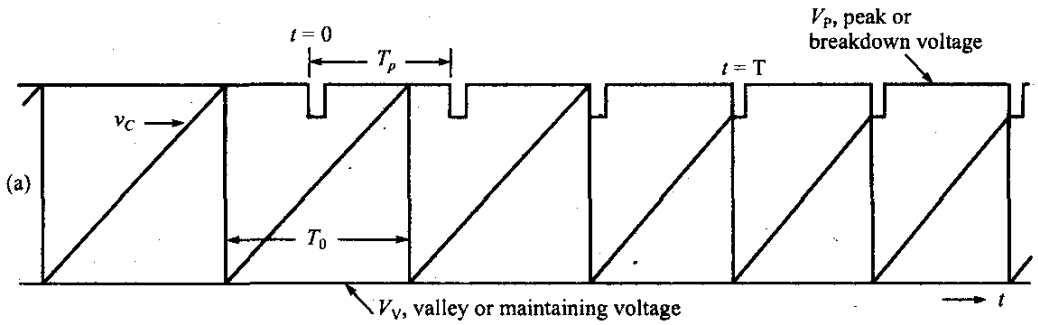


Figure 4.1 a sweep circuit with synchronization signal

Figure 4.2(a) shows the situation which results when synchronizing pulses are applied. The effect of the synchronization pulse is to lower the peak or breakdown voltage *Vp* for the duration of the pulse. A pulse train of regularly-spaced pulses is shown in Figure 4.2(a), starting at an arbitrary time $t = 0$. The first several pulses have no influence on the sweep generator, because the amplitude of the sweep at the occurrence of the pulse plus the amplitude of the pulse is less than V_P. Hence, the sweep generator runs unsynchronized. Eventually, however, the exact moment at which the UJT goes ON is determined by the instant of occurrence of a pulse [at time *T* in Figure 4.2(a)] as is also each succeeding beginning of the ON interval. From this point onwards, the sweep generator runs synchronously with the pulses.

For synchronization to result, the time of occurrence of the pulse should be such that it can serve to terminate the cycle prematurely. This requirement means that the interval between pulses T_{pt} must be less than the natural period T_0 of the generator. Figure 4.2(b) shows the case in which $T_p > T_0$. Here synchronization of each cycle does not occur. The pulses do serve to establish that four sweep cycles shall occur during the course of three pulse periods, but synchronization of this type is normally of no use.

Figure 4.2(c) shows a case in which $T_p < T_0$ as required, but synchronization does not result because the pulse amplitude is too small. In fact, even if the requirement $T_p < T_0$ is met, synchronization cannot result unless the pulse amplitude is at least large enough to bridge the gap between the quiescent breakdown voltage and the sweep voltage v_c.



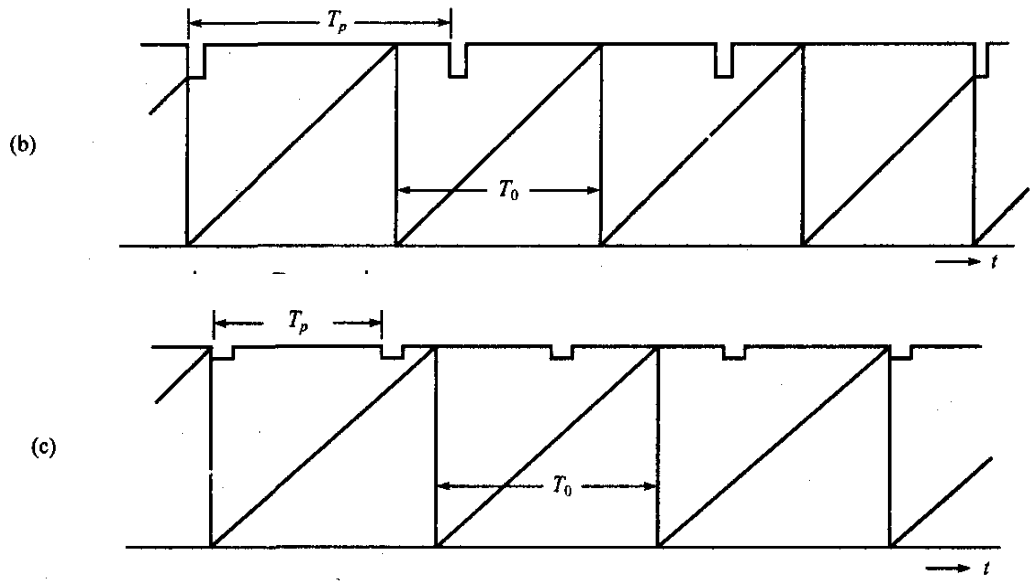


Figure 4.2 (a) $T_p < T_0$: synchronization results, (b) $T_p > T_Q$: no synchronization results and (c) $T_p < T_0$ but amplitude of synch pulse is small, hence no synchronization results.

Frequency Division in the Sweep Circuit

In Section 4.1 we saw that synchronization (1:1 division) occurs when $T_p < T_Q$ and the amplitude of the pulse is sufficient to terminate each cycle prematurely. Even if $T_p < T_0$, if the pulse amplitude is too small, then each cycle may not get terminated. Figure 4.3 shows a case in which the sweep cycles- are terminated only by alternate pulses marked "2". The pulses marked "1" would be required to have an amplitude at least equal to V_l if they were to be effective. The pulses marked "2" are effective because they occur closer to the time when the cycle would terminate of its own accord.

The sweep generator now acts as a divider, the division factor being 2, since exactly one sweep cycle occurs for every two synchronizing pulses. If T_s is the sweep generator period after synchronization, $TJT_p = 2$.

Observe that the amplitude V'_s of the sweep after synchronization is less than the unsynchronized amplitude V_s. Suppose T_p in Figure 4.3 is progressively decreased, eventually a point would be reached where even the alternate pulses would be too small in amplitude to fire the switch device. At this point, if $7"_0 > 3T_p$, division by a factor of 3 would result. If the condition $T_0 > 3T_p$ were not met, then again there would be no synchronization. On the other hand, if the pulse is made large enough, every (« + l)st pulse will be in a position to ensure synchronization before the nth pulse loses control.

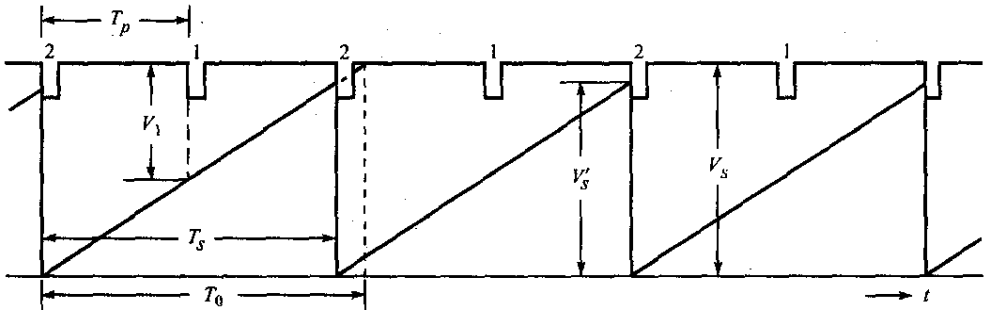


Figure 4.3 Frequency division by a factor of 2 in a sweep generator.

The basic principle of synchronization and use for counting purposes of other relaxation devices is same as the basic principle of synchronization of the sweep generator.

Other Astable Relaxation Circuits

Astable multivibrator

The astable multivibrator shown in Figure 4.4 may be synchronized or used as a divider by applying either positive or negative triggering pulses to either transistor or to both the transistors simultaneously. These pulses may be applied to the collector, base, or emitter. If for example, positive pulses are applied to B_2 or C_2 or negative pulses to E1, these triggers may produce synchronization by establishing the exact instant at which Q1 comes out of cut- off. If negative pulses are applied to B_2 or Q or positive pulses to E_2, then when Q_2 conducts, these pulses will be amplified and inverted and appear as positive pulses at B2.

Hence again the pulses may establish the instant when Qt comes out of cut-off. The negative pulses will not be effective unless they succeed in moving the transistor at least slightly into the active region. Therefore, such negative pulses must be large enough in amplitude and be supplied from a low impedance source to divert enough current from the base to draw the transistor out of saturation.

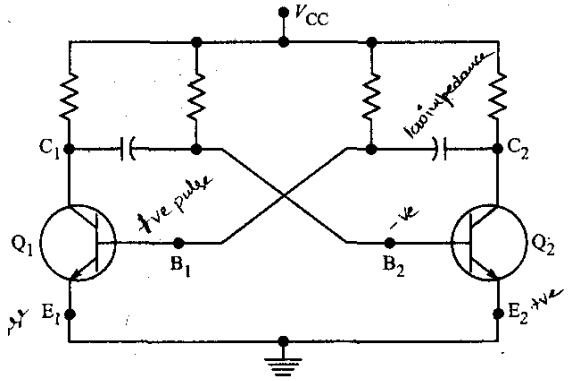


Figure 4.4 Astable Multi

Monostable Multivibrator

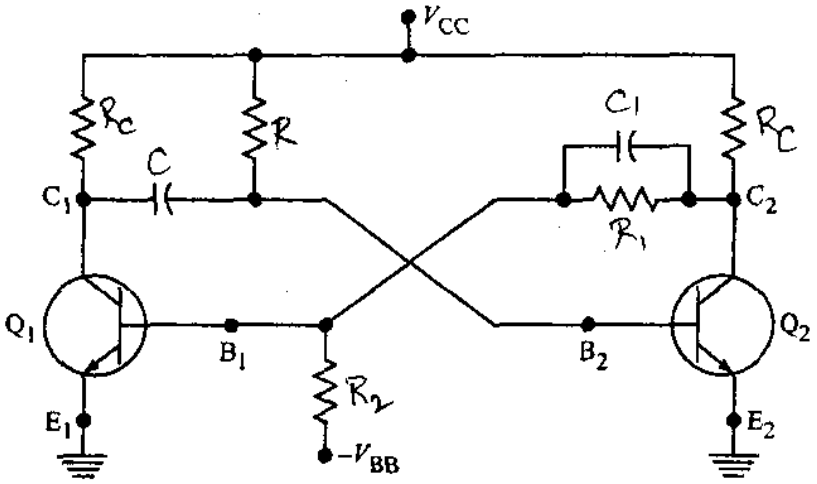


Figure 4.5 Monostable Multi

The monostable multivibrator shown in Figure may be synchronized or used as a divider by applying either positive or negative triggering pulses to either transistor or to both the transistors simultaneously. These pulses may be applied to the collector, base, or emitter. If for example, positive pulses are applied to B_t or C_2 or negative pulses to *E*, these triggers may produce synchronization by establishing the exact instant at which Q1 comes out of cut- off. If negative pulses are applied to B_2 or Q or positive pulses to E_2, then when Q_2 conducts, these pulses will be amplified and inverted and appear as positive pulses at B2. Hence again the pulses may establish the instant when Q2 comes out of cut-off. The negative pulses will not be effective unless they succeed in moving the transistor at least slightly into the active region. Therefore, such negative pulses must be large enough in amplitude and be supplied from a low impedance source to divert enough current from the base to draw the transistor out of saturation.

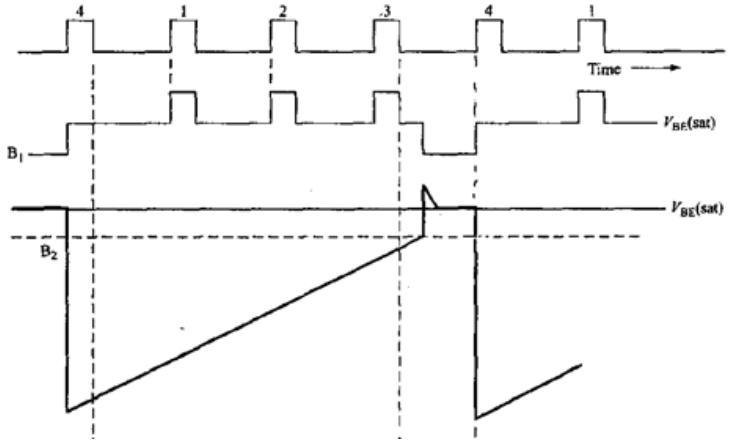


Fig.4.6: waveform at B2 with no pulse overshoot

The waveforms of Figure 4.6 shows the voltage at BI and B_2- Each fourth pulse causes a transition of the multivibrator, the remaining pulses occurring at a time when they are ineffective. Observe that while the total multivibrator cycle consisting of timing portion and recovery period is synchronized, the two separate portions are not synchronized. If positive pulses are applied, say, directly at B1 through a small capacitance from a low impedance source, the pulses are quasi differentiated during the conduction period of Qj. The negative overshoot is amplified and inverted by Q and appears as positive overshoot at B_2, and it may serve to terminate the cycle prematurely as shown in Figure 4.7.

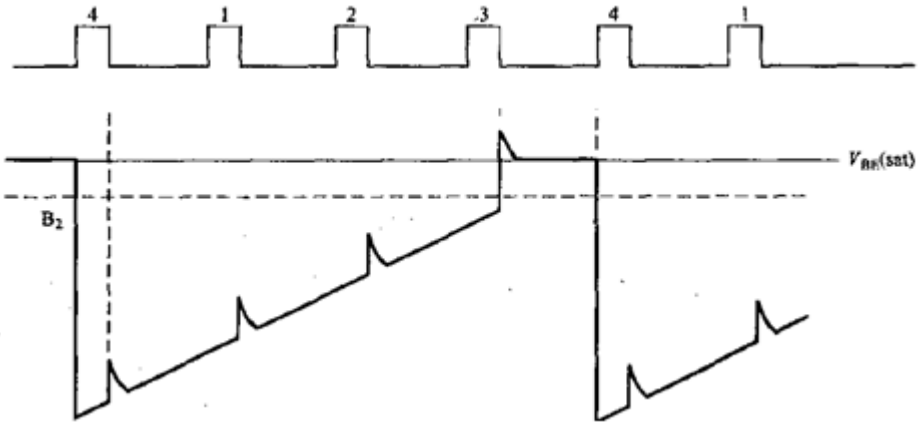


Fig.4.7: waveform at B2 with pulse overshoot

In this case, the two portions of the multivibrator waveform would be synchronized. Also, the counting ratio will change with increasing amplitude of pulse input. If the overshoot is large enough, the exponential will be terminated by the overshoot at-pulse 2 or pulse 1 and in which case the counting ratio will become respectively 3 or 2. Finally, with a large overshoot, the timing portion will terminate at the trailing edge of pulse 4, and the circuit will not operate as a multivibrator at all.

Phase Delay and Phase Jitters

The delay between the input pulse to a divider and the output pulse is referred to as *phase delay*. It results from the finite rise time of the input trigger pulse and the finite response time of the relaxation time devices. The phase delay may vary with time due to variations in device characteristics, supply voltages, etc. Occasionally some extraneous signal may be coupled unintentionally into the divider. Such a signal may have an influence on the exact moment at which a basic waveform, say, reaches cut-off. In this case the phase delay may be subject to periodic variations. All these factors which affect the phase delay give rise to what is termed phase jitter. In large-scale counters consisting of many stages, the phase jitter is compounded. In many applications, phase jitter is of no particular consequence but it constitutes an important difficulty in connection with nanosecond pulses.

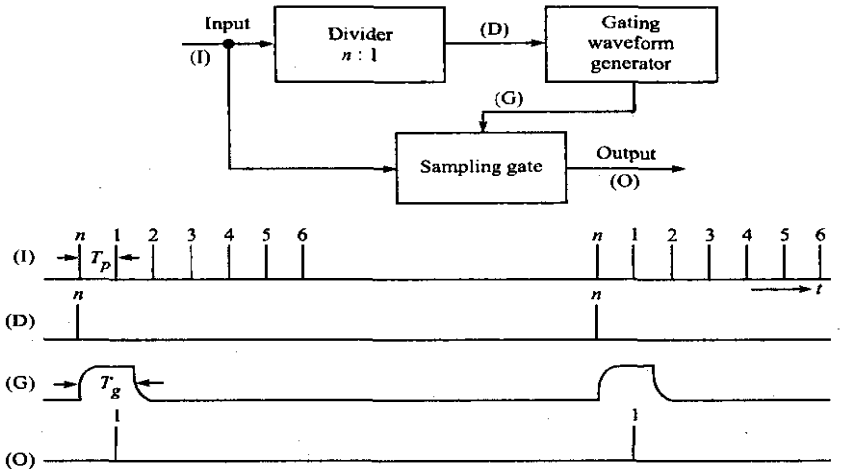


Fig.4.8 phase delay with signals

Synchronization Of A Sweep Circuit With Symmetrical Signals

In the previous sections we discussed the phenomenon of synchronization only for the case of pulse-type synchronizing signals. It was assumed that the synchronizing signal consists of a train of waveforms with leading edges which rise abruptly. In this section we will consider the case in which the voltage variation is gradual rather than abrupt. The mechanism of synchronization for a gradually varying synch signal is very nearly identical for all types of relaxation oscillators. Let us consider the synchronization of a ramp generator for illustration.

Sinusoidal synchronization signal

Consider the sweep generator of Figure 4.6, which uses a current-controlled negative-resistance device, a UJT, as a switch. Let us assume for simplicity that as a result of the synchronization signal, the breakdown voltage of the negative-resistance device varies sinusoidally. The polarity and the precise waveform required of the synchronization signal for such sinusoidal variation will depend on the particular negative-resistance device being employed. It is to be noted, however, that the circuit behavior to be described does not depend on the sinusoidal nature of the breakdown voltage variation. The results depend only on the relatively gradual variation of the breakdown voltage in contrast to the abrupt variation with pulse-type sync signals.

In Figure 4.9, the dashed voltage level V_{PO} is the breakdown voltage of the negative-resistance device in the absence of a synch signal and the solid curve V_p is the breakdown voltage in the presence of the synchronization signal. The sync signal has a period T, and the natural period is TQ. Consider that synchronization has been established with $T = TQ$.

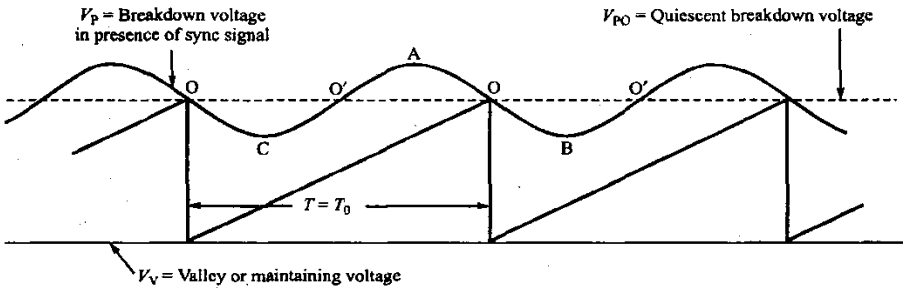


Figure 4.9 The timing relationship that must exist between V_P and the sweep voltage in a synchronized sweep when $T = T_0$.

Such synchronization requires that the period of the sweep shall not be changed in the sync signal. Hence the voltages which mark the limits of the excursion of the sweep voltage must remain unaltered. The sweep cycle must therefore continue to terminate at Vpo- This result, in turn, means that the intersection of the sweep voltage with the waveform V_p must occur as shown in Figure 4.8, at the time when V_P crosses Vpo, at the points labeled O in the figure. It is possible that the sweep will terminate at the points marked O' in the figure. In the case of pulse synchronization, we noted that synchronism could result only if the synch signal period was equal to or less than the natural period. This feature resulted from the fact that a pulse could serve reliably only to terminate a timing cycle prematurely and not to lengthen it. In the case of synchronization with symmetrical signals, however, synchronization is possible both when $T < TQ$ and when $T > TQ$. The timing relationship between the sweep voltage and the breakdown voltage for both the cases is shown in Figure 4.10 (a). The sweep voltage drawn as a solid line has a natural period $TQ > T$. The sweep voltage meets the V_P curve at a point below V_{PO} and is consequently prematurely terminated. The sweep voltage drawn as a dashed line has a natural period $T'Q < T$. This sweep meets the V_P curve at a point above VPQ and is consequently lengthened. In each case the synchronized period T_s equals the period 7".

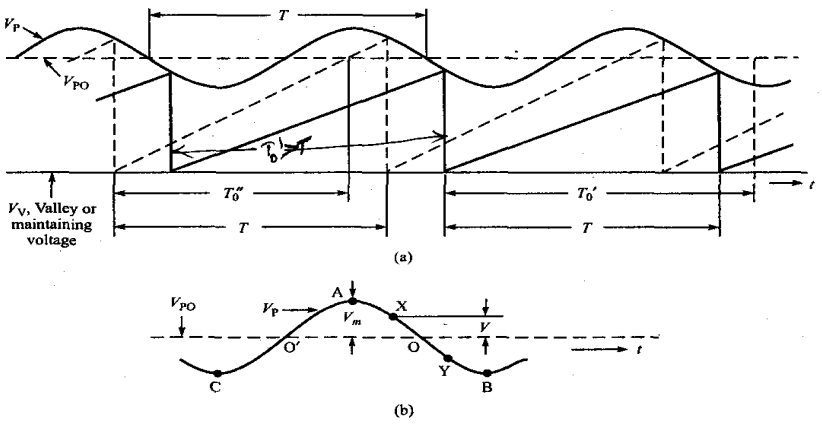


Figure 4.10(a) Shows the timing of the sweep voltage with respect to Vp for a case in which $T < TQ$ = TO (dashed line) and (b) pertains to the general case, $T * T_0$.

The general situation may be described by reference to Figure 4.10(b). When $T = TQ$, the sweep is terminated at point O, leaving the period unaltered. When $T > T_Q$, the sweep terminates at a point such as X—between O and the positive maximum A. When $T < T_Q$, the sweep terminates at a point such as Y between O and the negative maximum B. When the period T is such that the sweep terminates either at the point A or B, the limits of synchronization have been reached since at A the sweep period has been lengthened to the maximum extent possible whereas at B the shortening is at maximum.

UNIT – V

DIGITAL LOGIC FAMILIES

CMOS Inverter: It is complementary MOSFET obtained by using P-channel MOSPET and n- channel MOSFET simultaneously. The P and N channel are connected in series, their drains are connected together, output is taken from common drain point. Input is applied at common gate terminal. CMOS is very fast and consumes less power**.**

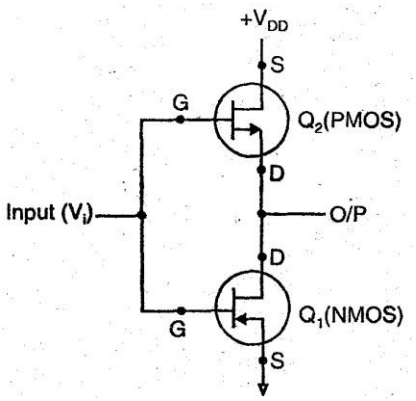


Figure 5.1 CMOS inverter

Case 1. When input Vi = 0. The Gate source voltage of Q1 will be 0 volt, it will be off. But Q2 will be ON; Hence output will be equal to +VDD or logic 1.

Case 2. When input Vi = 1, The V_{GS} (Gate source) voltage of Q2 will be 0 volt, it will be OFF, But Q1 will be ON. Hence output will be connected to• ground or logic 0. In this way, CMOS function as an inverter.

(i) **Tri-state logic:** When there are three states i.e. state 0, state 1 and high impendence i.e. called Tri-state logic. High impedance is considered as state when no current pass through circuit. Although in state 0 and state 1 circuit functions and current flows through it.

- Propagation delay is the average transition delay time for a pulse to propagate from input to output of a switching circuit.
- Fan-in is the number of inputs to the gate which it can handle.
- Fan-out is the number of loads the output of a gate can drive without effecting its operation.
- Power dissipation is the supply voltage required by the gate to operate with 50% duty cycle at a given frequency
- RTL, DTL, DTL are the logic families which are now obsolete.
- TTL is the most widely used logic family.

TTL gates may be

(a) Totem pole

(b) Open collector

(c) Tri-state .

- TTL is used in SSI and MSI Integrated circuits and is the fastest of all standard logic families.
- Totem pole TTL has the advantage of high speed and low power dissipation but its disadvantage is that it cannot be wired ANDed because of current spikes generation.
- Tri-state has three states .

  (a) High

  (b) Low

  (c) High Impedance

- ECL is the fastest of all logic families because its propagation delay is very small i.e. of about 2 nsec.
- ECL can be wired ORed.
- MOS logic is the simplest to fabricate.
- MOS transistor can be connected as a resistor.
- MOSFET circuitry are normally constructed from NMOS devices because they are 3 times faster than PMOS devices.
- CMOS uses both P-MOS and N-MOS.
- CMOS needs less power as compared to ECL as they need maximum power.
- Both NMOS and PMOS are more economical than CMOS because of their greater packing densities.
- Speed of CMOS gates increases with increase in VDD.
- CMOS has large fan-out because of its low output resistance.

Schematic of RTL NOR gate and its operation

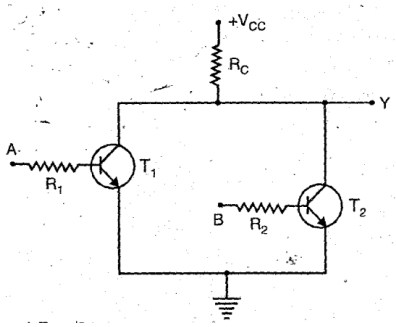


Figure 5.2 RTL NOR Gate

Working:

Case I: When A = B = 0.

Both T1 and T2 transistors are in cut off state because the voltage is insufficient to drive the transistors i.e. VBE < 0.6 V: Thus, output Y will be high, approximately equal to supply voltage Vcc. As no current flows through Rc and drop across Rc is also zero.

Thus, Y = 1, when A = B = 0.

Case II : When A = 0 and B = 1 or A = 1 and B = 0.

The transistor whose input is high goes into saturation where as other will goes to off cut state. This positive input to transistor increases the voltage drop across the collector resistor and decreasing the positive output voltage. Thus, Y = 0,when A= 0 and B = 1 or A = 1 and B = 0.

Case III : When A = B = 1. Both the transistors T1 and T2 goes into saturation and output voltage is equal to saturation voltage.

Thus, Y = 0, when A = B = 1

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Diode Transistor Logic

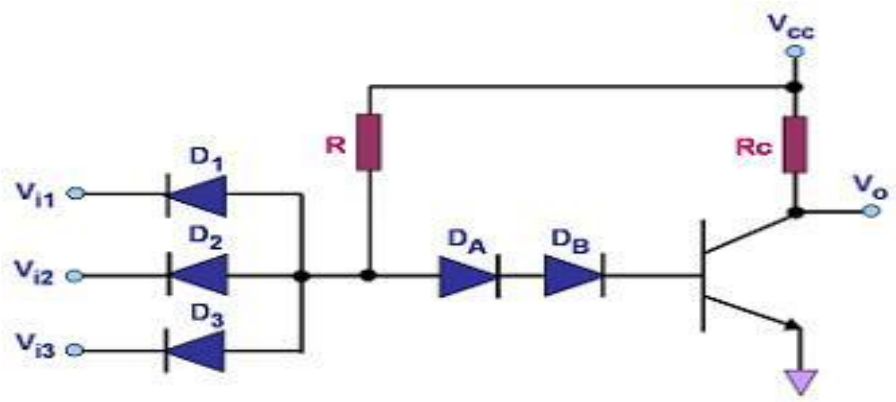


Figure 5.3. Diode Transistor Logic

In the NAND gate in Figure , the current through diodes DA and DB will only be large enough to drive the transistor into saturation and bring the output voltage Vo to logic '0' if all the input diodes D1-D3 are 'off', which is true when the inputs to all of them are logic '1'. This is because when D1-D3 are not conducting, all the current from Vcc through R will go through DA and DB and into the base of the transistor, turning it on and pulling Vo to near ground.

However, if any of the diodes D1-D3 gets an input voltage of logic '0', it gets forward-biased and starts conducting. This conducting diode 'shunts' almost all the current away from the reverse-biased DA and DB, limiting the transistor base current. This forces the transistor to turn off, bringing up the output voltage Vo to logic '1'.

Working:

Case I: When A = B = 0.

Both T1 and T2 transistors are in cut off state because the voltage is insufficient to drive the transistors i.e. VBE < 0.6 V: Thus, output Y will be high, approximately equal to supply voltage Vcc. As no current flows through Rc and drop across Rc is also zero.

Thus, Y = 1, when A = B = 0.

Case II: When A = 0 and B = 1 or A = 1 and B = 0.

The transistor whose input is high goes into saturation where as other will goes to off cut state. This positive input to transistor increases the voltage drop across the collector resistor and decreasing the positive output voltage.

Thus, Y = 0, when A= 0 and B = 1 or A = 1 and B = 0.

Case III: When A = B = 1**.** Both the transistors T1 and T2 goes into saturation and output voltage is equal to saturation voltage. Thus, Y = 0, when A = B = 1 Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Which is the output of NOR gate.

DCTL NAND gate with the help of suitable circuit diagram.

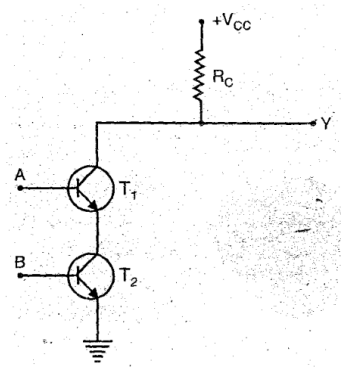


Figure 5.4: DCTL NAND Gate

Working

Case I: When A = B = 0. Both transistors T1 and T2 goes to cut off state. As the voltage is not sufficient to drive the transistor into saturation. Thus, the output voltage equal to Vcc.

When A = B = 0, output Y = 1

Case II: When A = 0 and B = 1 or A = 1 and, B = 0. The corresponding transistor goes to cut off state and the output voltage equals to Vcc.

Thus, When A = 0 and B = 1 or A = 1 and B = 0, Output Y = 1.

Case III: When A = B = 1. Both transistors T1 and T2 goes into saturation state and output voltage is insufficient to consider as '1'

Thus when A B = 1, output Y = 0. Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Compare standard TTL, Low power TTL and high speed TTL logic families.

Name of the logic family	Propagation delay (ns)	Power dissipation (mW)	Fan out	Max clock rate (Mhz)
Standard TTL	9	10	10	35
Low power TTL	33	1	20	3
High speed TTL	6	23	10	50

Characteristics and specification of CMOS.

1 Power supply (VDD) = 3 — 15 Volts

2. Power dissipation (Pd) = 10 nW

3. Propagation delay (td) = 25 ns

4. Noise margine (NM) = 45% of VDD

5, Fan out (FO) = >50

Two input ECL NOR gate

The circuit diagram of two input ECL NOR gate is as shown in figure 5.5

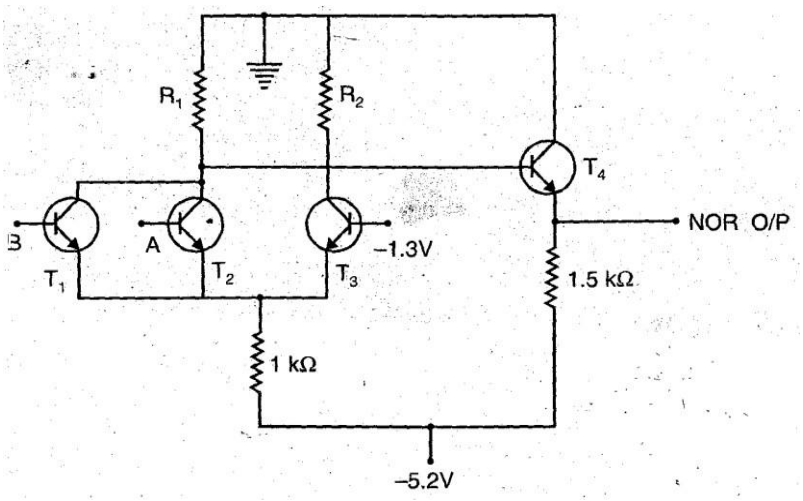


Figure 5.5: two input ECL NOR Gate

Working

Case I: When A = B = 0, the reference voltage of T3 is more forward biased then T1 and T2. Thus, T3 is ON and T1, T2 remains OFF. The value of R1 is such-that the output of NOR gate is high .i.e. '1'.

Case II: When A = 1 or B = 1 or A = B = 1, the corresponding transistors are ON, as they are more forward biased that T3 and thus T3 is OFF. Which makes the NOR output to be low i.e. '0'.
This shows that the circuit works as a NOR gate.

TTL inverter.

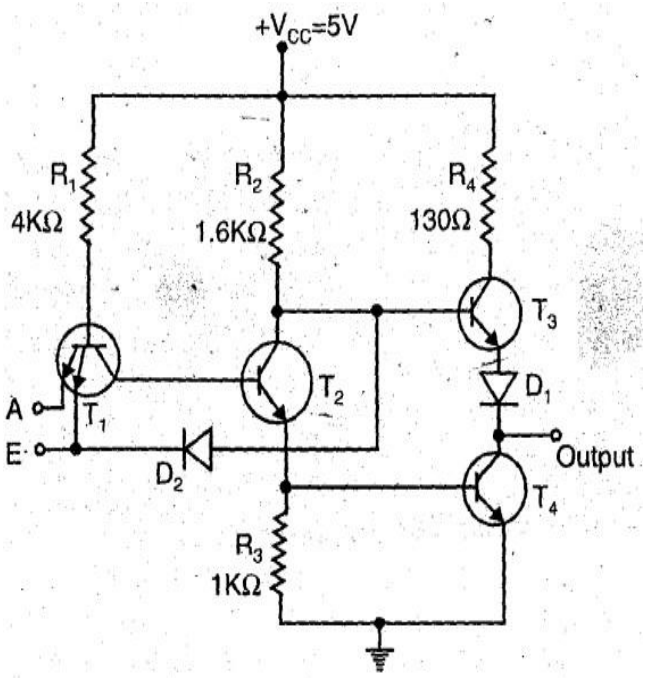


Figure 5.6: TTL Inverter

Tristate TTL inverter utilizer the high-speed operation of totem-pole arrangement while permitting outputs to be wired ANDed (connected together). It is called tristate TTL because it allows three possible output stages. HIGH, LOW and High-Impedance. We know that transistor T3 is ON when output is HIGH and T4 is ON when output is LOW. In the high impedance state both transistors, transistor T3 and T4 in the totem pole arrangement are med OFF. As a result the output is open or floating, it is neither LOW nor HIGH.

The above fig. shows the simplified tristate inverter. It has two inputs A and E. A is the normal logic input whereas E is an ENABLE input. When ENABLE input is HIGH, the circuit works as a normal inverter. Because when E is HIGH, the state-of the transistor T1 (either ON or OFF) depends on the logic input A and the additional component diode is open circuited as cathode is at logic HIGH. When ENABLE input is LOW, regardless of the state of logic input the base- emitter junction of T is forward biased and as a result it turns ON. This shunts the current through R1 away from T2 making it OFF. As T2 is OFF, there is no sufficient drive for T4 conduct and hence T4 turns OFF. The LOW at ENABLE input also forward biases diode D2, which shunt the current away from the base of T3, making it OFF. In this way, when ENABLE output is LOW, both transistors are OFF and output is at high impedance state.

ECL OR gate

ECL OR Gate: Emitter-coupled logic (ECL) is the fastest of all logic families and thus it is used in applications where very high speed is essential. High speeds have become possible in ECL because the transistors are used in difference amplifier configuration, in which they are never driven into saturation and thereby the storage time is eliminated. Here, rather than switching the transistors from ON to OFF and vice-versa, they are switched between cut-off and active regions. Propagation delays of less than 1 ns per gate have become possible in ECL.

Basically, ECL is realized using difference amplifier in which the emitters of the two transistors are connected and hence it referred to as emitter-coupled logic. A 3-input ECL gate is shown in Fig. 5.7 Which has three parts. The middle part is the difference amplifier which performs the logic operation.

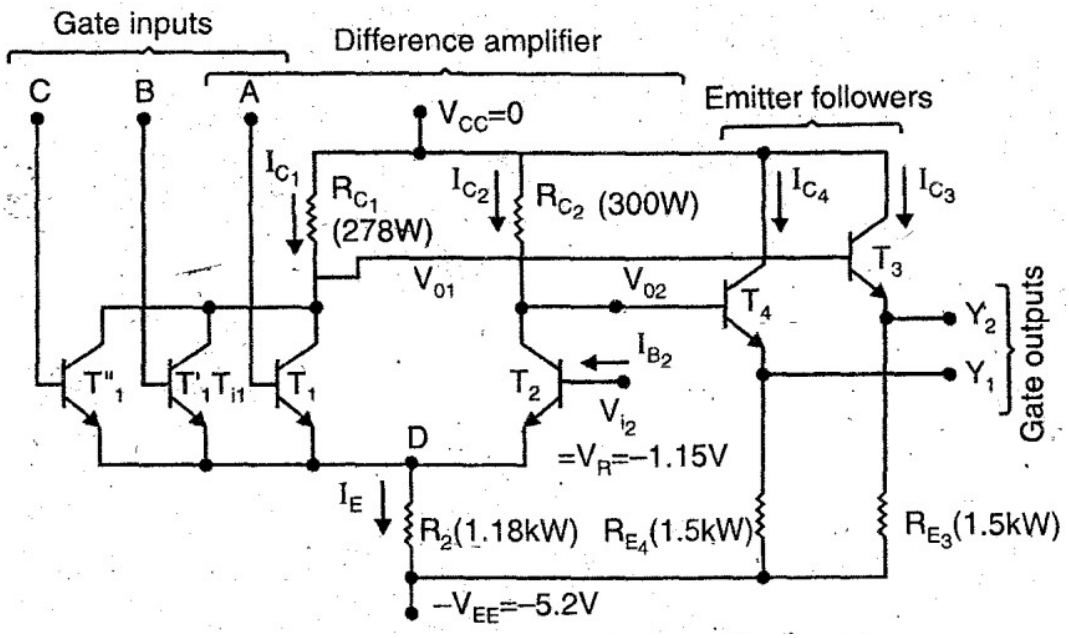


Figure 5.7: 3 input ECL OR/NOR Gate

Emitter followers are used for DC level shifting of the outputs, so that V (0) and V (1) are same for the inputs and the outputs. Note that two output Y1 and Y2 are available in this circuit which are complementary. Y1. Corresponds to OR logic and Y2 to NOR logic and hence it is named as an OR/NOR gate.

Additional transistors are used in parallel to T1 to get the required fan-in. There is a fundamental difference between all other logic families (including MOS logic) and ECL as far as the supply voltage is concerned. In ECL, the positive end of the supply is connected to ground in contrast to other logic families in which negative end of the supply is grounded. This is done to minimize the effect of noise induced in the power supply and protection of the gate from an accidental short circuit developing between the output of a gate and ground. The voltage corresponding to V (0) and V (1) are both negative due to positive end of the supply being connected to ground. The symbol of an ECL OR/NOR gate is shown in Fig.5.8

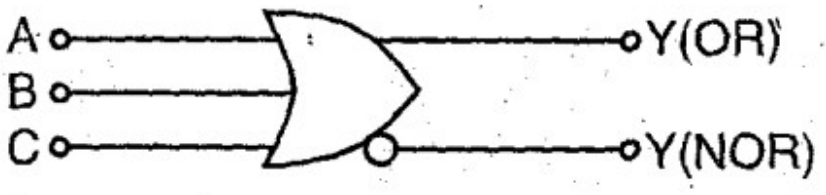


Figure 5.8: 3 input OR/NOR Gate

Open collector TTL NAND gate and explain its operation

The circuit diagram of 2-input NAND gate open-collector TTL gate is as shown:

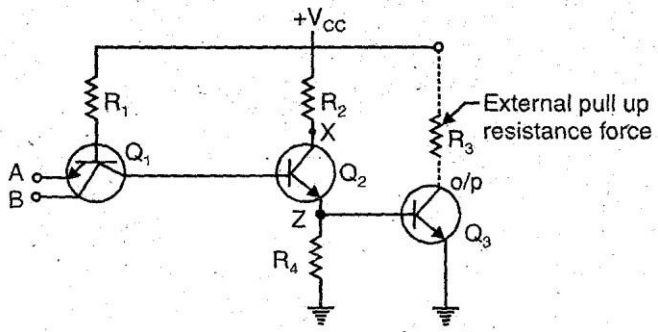


Figure 5.9: TTL NAND gate

Working

Case.1: When A = 0, B = 0

When both inputs A and B are low, both functions of Q1 are forward biased and Q2 remains off. So no current flows through R4 and Q3 is also off and its collector voltage is equal to Vcc i.e. Y= 1

Case2: When A = 0, B = 1 and **Case 3**: When A = 1, B = 0

When one input is high and. other is low, then one junction is forward biased so Q2 is off and Q3 is also off. So collector voltage is equal to Vcc i.e. Y = 1

Case 4: When A = 1, B = 1

When both inputs are high, Q1 is turned off and Q2 turned 'ON' Q3 goes into saturation and hence Y = 0. The open-collector output has main advantage that wired ANDing is possible in it.

TTL NAND gate

Two input TTL NAND gate-is given in fig.5.10, in this transistor T3 and T4 form a totem pole. Such type of configuration is called-as totem-pole output or active pull up output.

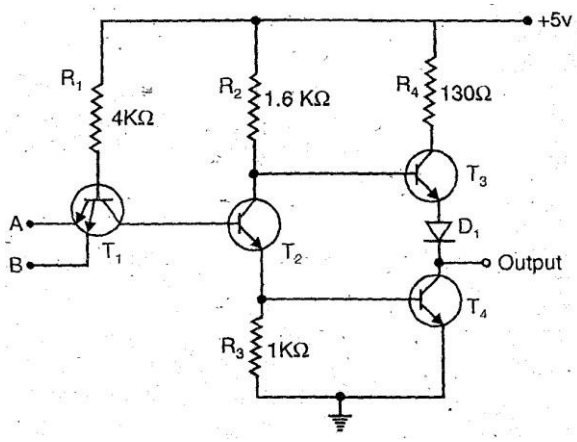


Figure 5.10: TTL NAND GAte

So, when A = 0 and B = 1 or (+5V). T1 conducts and T2 switch off. Since T2 is like an open

switch, no current flows through it. But the current flows through the resistor R2 and into the base of transistor T3 to turn it ON. T4 remains OFF because there is no path through which it can receive base current. The output current flows through resistor R4 and diode D1. Thus, we get high' output. When both inputs are high i.e. A = B = 1 or (+ 5V), T2 is ON and it drives T4 turning it ON. It is noted that the voltage at the base of T3 equals the sum of the base to emitter drop of T4 and VCE_{sat} of T2. The diode D1 does not allow base-emitter junction of T3 to be forward-biased and hence, T3 remains OFF when T4 is ON. Thus, we get low output, it works as TTL NAND gate.

Totem pole NAND gate

In TTL Totem pole NAND gate, multiple emitter transistor as input is used. The no. of inputs may be from 2 to 8 emitters. The circuit diagram is as shown

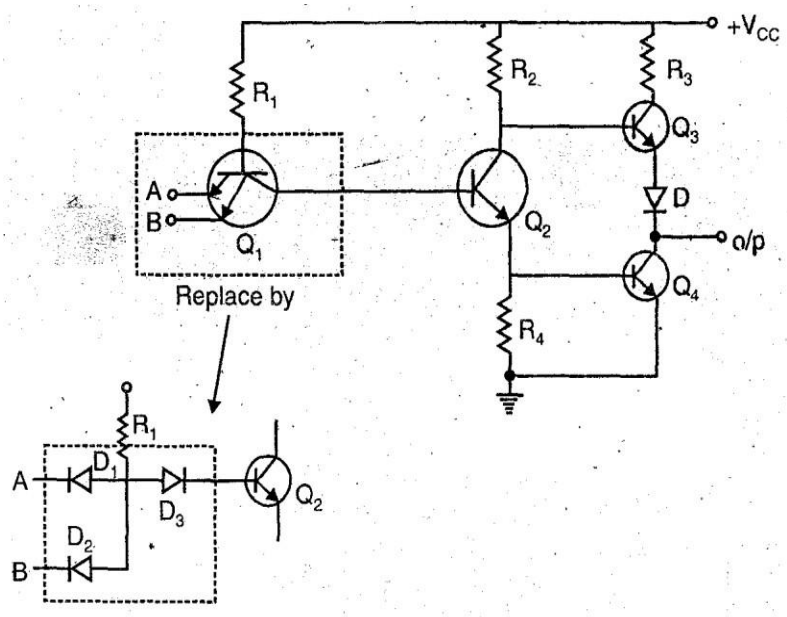


Figure 5.11 Totem pole NAND gate

Case 1:

When A = 0, B = 0

Now D1 and D2 both conduct, hence D3 will be off and make Q2 off. So its collector voltage rises and make Q3 'ON' and Q4 off; Hence output at Y = 1 (High)

Case 2 and Case 3:

If A = 0, B = 1 and A = 1, B=0

In both cases, the diode corresponding to low input will conduct and hence diode P3 will be OFF making Q2 OFF. In a similar way its collector voltage rises Q3 'ON' and Q4 'OFF'. Hence output voltage Y = 1 (High).

Case 4: A = 1, B = 1

Both diodes D1 and D2 will be off. D3 will be ‘ON’ and Q2 will ‘ON’ making Q4 also ‘ON’. But Q3 will be ‘OFF’. So output voltage Y = 0.

All the four cases shows that circuit operates as a NAND gate.

Totem pole can’t be Wired ANDed due to current spike problem. The transistors used in circuits may get damaged over a period of time though not immediately. Sometimes voltage level rises high than the allowable.