INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

TUTORIAL QUESTION BANK

Course Title	**INTEGRATED CIRCUITS APPLICATIONS**				
Course Code	AEC008				
Programme	B.Tech				
Semester	V	ECE | EEE			
Course Type	Core				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	-	3	3	2
Chief Coordinator	Ms.J Sravana, Assistant Professor				
Course Faculty	Ms. G Ajitha, Assistant Professor Mr. B Naresh, Assistant Professor Ms. N Anusha, Assistant Professor Mr. S Lakshmanachari, Assistant professor Ms. P Saritha, Assistant Professor Ms. KS Indrani, Assistant Professor				

COURSE OBJECTIVES

I	Be acquainted to principles and characteristics of op-amp and apply the techniques for the design of Comparators, instrumentation amplifier, integrator, differentiator, multivibrators, waveform generators, log and anti-log amplifiers.
II	Analyze and design filters, timer, analog to digital and digital to analog Converters.
III	Understand the functionality and characteristics of commercially available digital integrated circuits.

COURSE OUTCOMES (COs):

CO 1	Discuss the analysis of Op-Amp for different configurations and its properties.
CO 2	Analyze and design the linear and non linear applications of Op-Amp
CO 3	Design the various filters using Op-Amp and analysis of Multivibrators using 555 Timer
CO 4	Describe the various ADC and DAC techniques
CO 5	Explore the concepts of Combinational and sequential logic circuits using digital IC's

COURSE LEARNING OUTCOMES (CLOs):

CLO 1	Illustrate the block diagram, classifications, package types, temperature range, specifications and characteristics of Op-Amp.
CLO 2	Discuss various types of configurations in differential amplifier with balanced and unbalanced outputs.
CLO 3	Evaluate DC and AC analysis of dual input balanced output configuration and discuss the properties of differential amplifier and discuss the operation of cascaded differential amplifier.
CLO 4	Analyze and design linear applications like inverting amplifier, non-inverting amplifier, instrumentation amplifier and etc. using Op-Amp.
CLO 5	Analyze and design non linear applications like multiplier, comparator, log and anti log amplifiers, waveform generators and etc, using Op-Amp.
CLO 6	Discuss various active filter configurations based on frequency response and construct using 741 Op- Amp.
CLO 7	Design bistable, monostable and astable multivibrators operation by using IC 555 timer and study their applications.
CLO 8	Determine the lock range and capture range of PLL and use in various applications of communications.
CLO 9	Understand the classifications, characteristics and need of data converters such as ADC and DAC.
CLO 10	Analyze the digital to analog converter technique such as weighted resistor DAC, R-2R ladder DAC, inverted R-2R ladder DAC and IC 1408 DAC.
CLO 11	Analyze the analog to digital converter technique such as integrating, successive approximation and flash converters.
CLO 12	Design adders, multiplexers, demultiplexers, decoders, encoders by using TTL/CMOS integrated circuits and study the TTL and CMOS logic families.
CLO 13	Design input/output interfacing with transistor – transistor logic or complementary metal oxide semiconductor integrated circuits.
CLO 14	Understand the operation of SR, JK, T and D flip-flops with their truth tables and characteristic equations. Design TTL/CMOS sequential circuits.
CLO 15	Design synchronous, asynchronous and decade counter circuits and also design registers like shift registers and universal shift registers.

TUTORIAL QUESTION BANK

S.No	QUESTION	Blooms taxonomy level	Course Outcomes	Course Learning Outcomes
UNIT-I INTEGRATED CIRCUITS				
Part - A(Short Answer Questions)				
1	Mention the advantages of integrated circuits over discrete component circuit.	Remember	CO 1	AEC008.01
2	Classify the integrated circuits.	Remember	CO 1	AEC008.01
3	Name the different types if IC packages.	Remember	CO 1	AEC008.01
4	Define differential amplifier.	Understand	CO 1	AEC008.02
5	Mention the characteristics of an ideal op-amp.	Remember	CO 1	AEC008.02
6	Sketch the equivalent circuit of op-amp.	Remember	CO 1	AEC008.02
7	List the functions of level translator.	Remember	CO 1	AEC008.02
8	List the AC characteristics of op amp.	Remember	CO 1	AEC008.03
9	List the properties of differential amplifier.	Remember	CO 1	AEC008.02
10	Define input bias current.	Understand	CO 1	AEC008.03
11	Define slew rate.	Understand	CO 1	AEC008.03
12	Define CMRR	Understand	CO 1	AEC008.03
13	Define thermal drift.	Understand	CO 1	AEC008.03
14	List the specifications of practical op amp.	Remember	CO 1	AEC008.03
15	Define PSSR.	Understand	CO 1	AEC008.03
16	List the different temperature ranges of IC 741packages?	Remember	CO 1	AEC008.01
17	Give the classification of differential amplifier.	Remember	CO 1	AEC008.02
18	Write the equation for A_{CM} and CMRR	Remember	CO 1	AEC008.03
19	What is the difference between open loop and closed loop gain of op amp.	Remember	CO 1	AEC008.03
20	Write the ideal values of CMRR and input offset voltage.	Understand	CO 1	AEC008.03
Part - B (Long Answer Questions)				
1	Discus the operation of Differential amplifier with neat circuit diagram and list the types of differential amplifiers.	Remember	CO 1	AEC008.02
2	Analyze the input bias current compensation in an inverting amplifier with the help of circuit diagram.	Understand	CO 1	AEC008.03
3	Describe the following terms in an OP-AMP. 1. Input Bias current 2. Input offset voltage 3. Input offset current	Remember	CO 1	AEC008.03
4	Analyze the circuits for improving Common Mode Rejection Ratio for differential amplifier circuits.	Understand	CO 1	AEC008.03
5	Explain the external frequency compensation methods of operational amplifier circuit.	Remember	CO 1	AEC008.03
6	Calculate slew rate of a voltage follower op amp circuit for a given sinusoidal input.	Understand	CO 1	AEC008.03
7	Define stability. Discuss the stability of operational amplifier with neat circuit diagrams.	Remember	CO 1	AEC008.02
8	List and compare ideal and practical characteristics of an operational amplifier circuit.	Remember	CO 1	AEC008.03
9	Analyze the dual input balanced output configuration of Differential amplifier circuit.	Understand	CO 1	AEC008.02
10	Briefly Discuss the AC analysis of dual input balanced output differential amplifier circuit.	Remember	CO 1	AEC008.03
11	Explain the use of constant current bias method for Dual input balanced output differential amplifier.	Understand	CO 1	AEC008.03
12	Explain level translator of cascaded differential amplifier with neat circuit diagram.	Remember	CO 1	AEC008.03
13	Discuss common mode rejection ratio and Supply voltage rejection ratio for a given operational amplifier.	Understand	CO 1	AEC008.03

S.No	QUESTION	Blooms taxonomy level	Course Outcomes	Course Learning Outcomes
14	List out different configurations of differential amplifier. Explain any one of them in detail.	Remember	CO 1	AEC008.02
15	Explain two open loop op-amp configurations of operational amplifier with neat circuit diagrams.	Understand	CO 1	AEC008.02
16	Explain the difference between constant current bias and current mirror?	Remember	CO 1	AEC008.03
17	Why is RE replaced by a constant current bias circuit in a diffential amplifier?	Remember	CO 1	AEC008.03
18	Explain with figures how two supply V^+ and V^- are obtained from a single supply ?	Understand	CO 1	AEC008.01
19	Explain why CMRR $\rightarrow \infty$ for an emitter coupled differential amplifier when $R_E \rightarrow \infty$.	Remember	CO 1	AEC008.03
20	What is cross over distortion and how it is eliminated?	Remember	CO 1	AEC008.03
	Part - C (Analytical Questions)			
1	Determine the output voltage of the differential amplifier having input Voltages V1=1mV and V2=2 mV. The amplifier has a differential gain of 5000 and CMRR 1000.	Understand	CO 1	AEC008.02
2	An op-amp with a slew rate = 0.5V/µS is used as an inverting amplifier to obtain a gain of 100. The voltage gain Vs frequency characteristic of the amplifier is flat up to 10 KHz. Determine i. The maximum peak-to-peak input signal that can be applied without any distortion to the output ii. The maximum frequency of the input signal to obtain a sine wave output of 2V peak.	Remember	CO 1	AEC008.03
3	(a) Derive slew rate equation and discuss the effect of slew rate in applications of op-amp. (b) Explain the term thermal drift. Find the output voltage of a non- inverting amplifier if the temperature rises to 50oC for an offset voltage drift of 0.15mV/oC if it was nulled at 25oC.	Remember	CO 1	AEC008.03
4	A differential amplifier has (i) CMRR = 1000 and (ii) CMRR = 10000. The first set of inputs is V_1 = 100 V and V_2 = -100 V. The second set of inputs is V_1 = 1100 V and V_2 = 900 V. Calculate the percentage difference in output voltages obtained for the two sets of input voltage and also comment on this.	Understand	CO 1	AEC008.03
5	For an op-amp PSRR =60 db(min), CMRR= 10^4 and the differential mode gain is 10^5, the voltage changes by 20 V in 4 µ sec. calculate (i) numerical value of the PSRR (ii) common mode gain. (iii) Slew rate.	Remember	CO 1	AEC008.03
6	For a differential amplifier R_C=1 KΩ, R_S=1 K Ω, h_{ie}=1 K Ω, h_{fe}=50, the emitter resistance of 2.5 M Ω while the differential input of 1 mV. Calculate the output voltage and CMRR in db. If the common mode input is 20 mV. Assume single ended output.	Understand	CO 1	AEC008.02
7	An op - amp has a slew rate of 1.5V/µs. What is the maximum frequency of an output sinusoid of peak value 10 V at which the distortion sets in due to the slew rate limitation?	Remember	CO 1	AEC008.03
8	Derive the output voltage of an op-amp based differential amplifier.	Understand	CO 1	AEC008.02
9	An op-amp has a differential gain of 80 dB and CMRR of 95 Db. If V1=2µV and V2=1.6µV.then calculate differential and common mode output values.	Remember	CO 1	AEC008.03
10	The input signal to an op-amp is $0.03\sin(1.5\times10^5)t$. calculate maximum gain of an op-amp with the slew rate of 0.4V/µ sec.	Understand	CO 1	AEC008.03
	UNIT - II **APPLICATIONS OF OP-AMPS**			
	Part – A (Short Answer Questions)			

1	List the applications of IC741?	Remember	CO 2	AEC008.04
2	Draw the circuit diagram of integrator?	Remember	CO 2	AEC008.04
3	Define voltage follower?	Understand	CO 2	AEC008.04
4	Give the applications of comparator?	Remember	CO 2	AEC008.05
5	Draw the circuit diagram of differentiator?	Remember	CO 2	AEC008.04
6	What are the applications of DC amplifier?	Remember	CO 2	AEC008.05
7	What do you mean by summing amplifier?	Understand	CO 2	AEC008.04
8	Draw the diagram of inverting adder?	Remember	CO 2	AEC008.04
9	How op-amps can be used to subtract the two input voltages?	Remember	CO 2	AEC008.04
10	What are the applications of log amplifier?	Understand	CO 2	AEC008.05
11	What are the applications of AC amplifier?	Remember	CO 2	AEC008.05
12	What are the limitations of differentiator?	Understand	CO 2	AEC008.04
13	Give the applications of anti-log amplifier?	Remember	CO 2	AEC008.05
14	What are the limitations of integrator?	Understand	CO 2	AEC008.04
15	Explain why integrators are preferred over differentiators in analog computers?	Remember	CO 2	AEC008.04
Part - B (Long Answer Questions)				
1	What is the instrumentation amplifier? What are the required parameters of an instrumentation amplifier? Explain the working of instrumentation amplifier with neat circuit diagram.	Remember	CO 2	AEC008.04
2	Derive the gain expression for inverting operational amplifier and non inverting operational amplifier.	Understand	CO 2	AEC008.04
3	With circuit and waveforms explain the application of OPAMP as Differentiator and write the advantages of practical differentiator.	Remember	CO 2	AEC008.04
4	Explain practical integrator circuit using IC 741 and list the advantages of practical integrator over ideal integrator.	Understand	CO 2	AEC008.04
5	Explain the operation of AC amplifier and obtain its transfer function.	Understand	CO 2	AEC008.05
6	Draw the circuit of a log amplifier using two op-amps and explain its operation?	Remember	CO 2	AEC008.05
7	Draw and explain the operation of square wave generator using op amp 741and give necessary equations.	Remember	CO 2	AEC008.05
8	What are the limitations of an ordinary op-amp differentiator? Draw the circuit of a practical differentiator that will eliminate these limitations?	Remember	CO 2	AEC008.04
9	Explain the operation of monostable multivibrator using op amp and derive the expression for pulse width.	Understand	CO 2	AEC008.05
10	Draw and explain the operation of triangular waveform generator using necessary equations.	Remember	CO 2	AEC008.05
Part - C (Analytical Questions)				
1	Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 1 KHz. If a sine wave of 1V peak at 1000 Hz is applied to this differentiator draw the output waveforms.	Remember	CO 2	AEC008.04
2	Draw the output waveform for a sine wave of 1V peak at 100Hz applied to the differentiator.	Remember	CO 2	AEC008.04
3	Design an op-amp differentiator that will differentiate an Input signal with fmax = 100Hz.	Remember	CO 2	AEC008.04
4	Find R_1 and R_f in the lossy integrator so that the peak gain is 20dB and the gain is 3dB down from its peak when ω = 10,000 rad/sec. use a capacitance of 0.01micro farads.	Remember	CO 2	AEC008.04
5	Design an op-amp differentiator that will differentiate an Input signal with f_{max} = 1000Hz	Remember	CO 2	AEC008.04
6	Design a square wave generator using op amp to oscillate frequency f_o = 1KHz and dc supply voltage = ±12V.	Remember	CO 2	AEC008.05
7	Draw the output waveform for a sine wave of 2V peak at 1000Hz applied to the differentiator.	Remember	CO 2	AEC008.05

S.No	QUESTION	Blooms taxonomy level	Course Outcomes	Course Learning Outcomes
8	Design a comparator circuit for input voltage = $2V_{pp}$ sine wave at 1KHz, V_{ref}=500mV, R=100Ω, and supply voltage= ±15V.Draw the output waveform.	Remember	CO 2	AEC008.05
9	Design a differential instrumentation amplifier using a transducer bridge. Given data R_1=1kΩ, R_f=4.7 kΩ, R_A=R_B=R_C=100 kΩ, V_{DC}=5v,and op- amp supply voltages = ±15V.The transducer is a thermistor with the following specifications: R_T=100 kΩ at a reference temperature of 25°C; temperature coefficient of resistance = -1kΩ/°C or 1%/°C. Determine the output voltage at 0°Cand at 100°C .	Remember	CO 2	AEC008.04
10	For a non inverting single supply AC amplifier R_{in}=50 Ω, C_i=0.1µF, C_1=0.1µF, R_1=R_2=R_3=100K Ω, R_f= 1M Ω and V_{CC}= +12 V. Determine the bandwidth of the amplifier and maximum voltage swing.	Remember	CO 2	AEC008.05
UNIT-III ACTIVE FILTERS AND TIMERS				
Part - A (Short Answer Questions)				
1	Illustrate why active filters are preferred?	Understand	CO 3	AEC008.06
2	What is meant by cut off frequency of a high pass filter and how it is found out in a first order high pass filter?	Remember	CO 3	AEC008.06
3	Define an electronic filter.	Remember	CO 3	AEC008.06
4	Define pass band and stop band of a filter.	Remember	CO 3	AEC008.06
5	Discuss the disadvantages of passive filters?	Understand	CO 3	AEC008.06
6	Define pass band of a filter?	Remember	CO 3	AEC008.06
7	Define stop band of a filter?	Understand	CO 3	AEC008.06
8	What is the roll-off rate of a first order filter?	Remember	CO 3	AEC008.06
9	Why do we use a high order filters?	Understand	CO 3	AEC008.06
10	Give the applications of wideband pass filter?	Remember	CO 3	AEC008.06
11	Define figure of merit or Q factor in terms of bandwidth?	Understand	CO 3	AEC008.06
12	Draw the circuit diagram of 1st order low pass filter?	Remember	CO 3	AEC008.06
13	Draw the circuit diagram of 1st order high pass filter?	Understand	CO 3	AEC008.06
14	What are the applications of band rejet filters?	Remember	CO 3	AEC008.06
15	Define Notch filter?	Remember	CO 3	AEC008.06
CIE-II				
1	List the applications of 555 timer in Monostable mode of operation	Remember	CO 3	AEC008.08
2	Give the pin configuration of 555 IC?	Understand	CO 3	AEC008.08
3	What are the basic blocks in PLL?	Remember	CO 3	AEC008.08
4	List the applications of 565 PLL	Remember	CO 3	AEC008.08
5	Define lock range in PLL	Remember	CO 3	AEC008.08
6	Define capture range in PLL	Remember	CO 3	AEC008.08
7	Give the different types of phase detectors?	Understand	CO 3	AEC008.08
8	Define pull-in-time?	Remember	CO 3	AEC008.08
9	What are the major differences between digital and analog PLLs	Remember	CO 3	AEC008.08
10	What are the applications of Monostable multivibrator?	Remember	CO 3	AEC008.07
11	What are the applications of Astable multivibrator?	Remember	CO 3	AEC008.07
12	What are the applications of Schmitt trigger?	Remember	CO 3	AEC008.07
13	Define duty cycle?	Remember	CO 3	AEC008.08
14	Give the pin configuration of voltage controlled oscillator - IC566	Understand	CO 3	AEC008.08
15	Give the applications of Comparator?	Understand	CO 3	AEC008.08
Part - B (Long Answer Questions)				
1	Describe a second order low pass filter with circuit diagram and derive its transfer function.	Understand	CO 3	AEC008.06

2	Draw the circuit of a first order low pass filter and derive its transfer function using necessary equations.	Remember	CO 3	AEC008.06
3	Draw the circuit of a narrow band pass filter and derive its transfer function using necessary equations.	Remember	CO 3	AEC008.06
4	Draw the circuit of a all pass filter and derive its transfer function using necessary equations.	Remember	CO 3	AEC008.06
5	Explain second order high pass filter and derive its transfer function using necessary equations.	Understand	CO 3	AEC008.06
7	Draw the circuit of a first order high pass filter and derive its transfer function	Remember	CO 3	AEC008.06
8	Draw the circuit of a narrow band reject filter and derive its transfer function.	Understand	CO 3	AEC008.06
9	Draw the circuit of a wide band pass filter and derive its transfer function using necessary equations.	Remember	CO 3	AEC008.06
10	Illustrate the differences between wide band pass and narrow band pass filters?	Understand	CO 3	AEC008.06
CIE-II				
1	Explain each block of the functional block diagram of 555 timer and list the advantages of 555 timer.	Understand	3	AEC008.07
2	Explain working principle of Phase locked loop using appropriate block diagram and equations.	Understand	CO 3	AEC008.08
3	Draw the block diagram of an Astable multivibrator using 555timer and derive an expression for its frequency of oscillation	Remember	CO 3	AEC008.07
4	Derive the expression for i) capture range in PLL ii) Lock in ranging Phase locked loop.	Remember	CO 3	AEC008.08
5	Draw the schematic diagram of voltage controlled oscillator and explain its working principle?	Remember	CO 3	AEC008.08
6	Derive the expression for pulse width of monostable multi using 555 timer.	Remember	CO 3	AEC008.07
7	Explain any two applications of monostable multi using 555 timer with the help of diagrams.	Understand	CO 3	AEC008.07
8	Derive the expression for lock in range of phase locked loop.	Remember	CO 3	AEC008.08
9	Explain the operation of frequency multiplier using phase locked loop with neat circuit diagram.	Understand	CO 3	AEC008.08
10	Explain any two applications of IC565 with neat circuit diagrams.	Understand	CO 3	AEC008.08
Part - C (Analytical Questions)				
1	Design a second order Butterworth low-pass filter having upper cut-off frequency 1 kHz. Then determine its frequency response. Given parameters: f_h=1 kHz, C=0.1μF, R=1.6KΩ and damping factor α=1.414.	Understand	CO 3	AEC008.06
2	Design a second order Butterworth High-pass filter having lower cut-off frequency 1 kHz. Given parameters: f_h=1 kHz, C=0.1μF, R=1.6KΩ and damping factor α=1.414. Calculate R_F & R_i and also determine its frequency response.	Remember	CO 3	AEC008.06
3	Design a wide band pass filter having f_l=400Hz, f_h=2kHz and pass band gain of 4. Find the value of Q factor of the filter.	Understand	CO 3	AEC008.06
4	Design a wide band reject filter having f_h=400Hz, f_l=2kHz and pass band gain of 2. Find the value of Q factor of the filter.	Remember	CO 3	AEC008.06
5	Design 1st order wideband pass filter if lower cut off frequency is 500Hz, and upper cut off frequency is 2KHz.	Remember	CO 3	AEC008.06
6	Design a 2nd order HPF at a cutoff frequency of 2 KHz.	Understand	CO 3	AEC008.06
7	Design a 2nd order LPF at a cutoff frequency of 4 KHz.	Remember	CO 3	AEC008.06
CIE-II				
1	Design an Astable Multivibrator using 555 Timer to produce 1Khz square wave form for duty cycle=0.50	Understand	CO 3	AEC008.07

S.No	QUESTION	Blooms taxonomy level	Course Outcomes	Course Learning Outcomes
2	Design a 555 based square wave generator to produce an asymmetrical square wave of 2 KHz. If Vcc=12V, draw the voltage curve across the timing capacitor and output waveform.	Remember	CO 3	AEC008.07
3	Design and draw the wave forms of 1KHZ square waveform generator using555 Timer for duty cycle D=25% .	Understand	CO 3	AEC008.07
UNIT-IV DATA CONVERTERS				
Part - A (Short Answer Questions)				
1	Illustrate the need of data converters	Understand	CO 4	AEC008.09
2	Illustrate the different type of DAC techniques.	Understand	CO 4	AEC008.10
3	Give applications of data converters.	Remember	CO 4	AEC008.09
4	Give the drawbacks of weighted resistor type DAC.	Remember	CO 4	AEC008.10
5	Give the advantages of weighted resistor type DAC.	Remember	CO 4	AEC008.10
6	Calculate basic step of 9 bit DAC is 10.3 mV. If 000000000 represents 0V, what output produced if the input is 101101111?	Remember	CO 4	AEC008.10
7	What output voltage would be produced by monolithic DAC whose output range is 0 to 10V and whose input binary is 10111100?	Remember	CO 4	AEC008.10
8	Define off set error in DAC.	Remember	CO 4	AEC008.10
9	What are the main advantages of integrating type ADCs?	Remember	CO 4	AEC008.11
10	Define linearity error in DAC.	Remember	CO 4	AEC008.10
11	Define resolution in DAC.	Remember	CO 4	AEC008.10
12	List out the direct type ADCs	Understand	CO 4	AEC008.11
13	Explain in brief the principle of operation of successive approximation ADC	Understand	CO 4	AEC008.11
14	List the broad classification of ADCs	Understand	CO 4	AEC008.11
15	Calculate the values of the full scale output for an 8 bit DAC for the 0 to 10V range	Understand	CO 4	AEC008.10
16	Define integrating type ADCs?	Remember	CO 4	AEC008.10
17	Define nonlinearlity in output of adc/dac	Remember	CO 4	AEC008.10
18	List out the drawback to overcome charge balancing ADC?	Understand	CO 4	AEC008.11
19	What is settling time	Remember	CO 4	AEC008.10
20	Define full scale error	Remember	CO 4	AEC008.10
Part – B (Long Answer Questions)				
1	Explain the working of a Weighted resistor D/A converter using neat circuit diagram.	Understand	CO 4	AEC008.10
2	Discuss the successive approximation A/D converter and list the advantages of successive approximation A/D converter	Understand	CO 4	AEC008.11
3	Discuss the working principal of a dual slope A/D converter with neat circuit diagram	Understand	CO 4	AEC008.11
4	With neat diagram, explain the working principle of inverter R-2R ladder DAC.	Understand	CO 4	AEC008.10
5	Explain the working of a counter type A/D converter and state it's important feature	Understand	CO 4	AEC008.11
6	Describe the specifications, advantages and applications of Digital to Analog converters.	Remember	CO 4	AEC008.09
7	With neat diagram, explain the working principle of R-2R ladder type DAC.	Remember	CO 4	AEC008.10
8	Discuss the operation of parallel comparator type ADC with circuit diagram.	Remember	CO 4	AEC008.11
9	Discuss 4 bit weighted resistor DAC with neat circuit diagram and list the advantages.	Understand	CO 4	AEC008.10
10	Explain How many equal intervals are present in a 14-bit D-A converter?	Understand	CO 4	AEC008.11

S.No	QUESTION	Blooms taxonomy level	Course Outcomes	Course Learning Outcomes
11	A 10-bit D/A converter have an output range from 0-9v. Calculate the output voltage produced when the input binary number is 1110001010.	Understand	CO 4	AEC008.11
12	Explain the working and principle of a ic1408 with a neat pin diagram	Understand	CO 4	AEC008.11
13	Explain the DAC applications of digital circuit has provide an analog voltage or current to drive an analog device?	Understand	CO 4	AEC008.11
14	Explain the digital ramp ADC by binary counter and allow clock to increment the counter?	Understand	CO 4	AEC008.11
15	Explain settling time, linearity error, resolution	Understand	CO 4	AEC008.11
16	Discuss the function of the EOC signal and SOC signal	Understand	CO 4	AEC008.11
17	Explain and Draw digital ramp ADC and write down its operation.	Understand	CO 4	AEC008.11
18	Describe offset error and its effect on a DAC output.	Understand	CO 4	AEC008.11
19	Explain the applicatin of ADC and DAC in signal reconstrcution	Understand	CO 4	AEC008.11
20	Discuss the application of data converters interfacing with the analog world	Understand	CO 4	AEC008.11
	Part - C (Analytical Questions)			
1	Calculate basic step of 9 bit DAC is 10.3 mV. If 000000000 represents 0V, what output produced if the input is 101101111.	Understand	CO 4	AEC008.10
2	Design a dual slope ADC uses a16-bit counter and a 4MHz clock rate. The maximum input voltage is+10v. The maximum integrator output voltage should be-8v when the counter has cycled through 2n counts. The capacitor used in the integrator is 0.1 µF Find the value of the resistor R of the integrator.	Remember	CO 4	AEC008.11
3	Design a dual slope ADC uses an 18 bit counter with a 5MHz clock. The maximum integrator input voltage in +12V and maximum integrator output voltage at 2n count is -10V. If R=100KΩ, find the size of the capacitor to be used for integrator.	Remember	CO 4	AEC008.11
4	Calculate the values of the LSB,MSB and full scale output for an 8 bit DAC for the 0 to 10V range.	Remember	CO 4	AEC008.10
5	How many levels are possible in a two bit DAC what is its resolution if the output range is 0 to 3V.	Understand	CO 4	AEC008.10
6	Calculate what is the conversion time of a 10 bit successive approximation A/D converter if its 6.85V.	Remember	CO 4	AEC008.11
7	Calculate basic step of 9 bit DAC is 10.3 mV. If 000000000 represents 0V, what output produced if the input is 100101101	Remember	CO 4	AEC008.10
8	Calculate the values of the LSB,MSB and full scale output for an 8 bit DAC for the 0 to 5V range	Understand	CO 4	AEC008.10
9	How many levels are possible in a two bit DAC what is its resolution if the output range is 0 to 4V.	Remember	CO 4	AEC008.11
10	Design a dual slope ADC uses an 18 bit counter with a 2MHz clock. The maximum integrator input voltage in +12V and maximum integrator output voltage at 2n count is -10V. If R=100KΩ, find the size of the capacitor to be used for integrator.	Remember	CO 4	AEC008.11
	UNIT-V DIGITAL IC APPLICATIONS			
	Part - A (Short Answer Questions)			
1	Name the three types of TTL gate.	Remember	CO 5	AEC008.13
2	Define noise margin of a logic family.	Remember	CO 5	AEC008.13
3	Define combinational circuit.	Understand	CO 5	AEC008.12
4	Define sequential circuit.	Remember	CO 5	AEC008.14
5	Give the differences between combinational design and sequential design.	Understand	CO 5	AEC008.12
6	Compare latch and flip flop.	Understand	CO 5	AEC008.14

S.No	QUESTION	Blooms taxonomy level	Course Outcomes	Course Learning Outcomes
7	Sketch the 1 X 2 demux.	Understand	CO 5	AEC008.12
8	Define counter.	Understand	CO 5	AEC008.15
9	Describe the differences between synchronous counters and asynchronous counters	Understand	CO 5	AEC008.15
10	Explain Johnson counter.	Understand	CO 5	AEC008.15
11	What is ring counter.	Understand	CO 5	AEC008.15
12	Define priority encoder.	Understand	CO 5	AEC008.12
13	How many select lines are needed to construct 16 X 1 mux.	Remember	CO 5	AEC008.12
14	What is race around condition?	Remember	CO 5	AEC008.14
15	How many flip flops are required to construct Mod-12 counter.	Remember	CO 5	AEC008.15
16	Explain full- adder in brief	Remember	CO 5	AEC008.12
17	Explain the working of decoders	Remember	CO 5	AEC008.14
18	Difference between combinational logic circuit and sequential logic circuit	Remember	CO 5	AEC008.15
19	Discuss the applications of shift registers.	Remember	CO 5	AEC008.12
20	Difference between Synchronous and asynchronous counters	Remember	CO 5	AEC008.12
Part - B (Long Answer Questions)				
1	Compare CMOS, TTL and ECL with reference to logic levels, DC noise margin, propagation delay and fan-out.	Remember	CO 5	AEC008.13
2	Discuss the following terms with reference to CMOS logic. i. Logic Levels ii. Noise margin iii. Power supply rails iv. Propagation delay	Understand	CO 5	AEC008.13
3	Implement BCD to 7 segment display decoder using common cathode using 4:16 decoder.	Remember	CO 5	AEC008.12
4	Explain the operation of priority encoder IC 74XX148 using pin diagram and truth table.	Remember	CO 5	AEC008.12
5	Design 32X1 multiplexer using four 74X151 multiplexers and one 74X139 decoder.	Remember	CO 5	AEC008.12
6	Explain 4 bit binary parallel adder IC 74LS83/74LS283 with logic diagram.	Remember	CO 5	AEC008.12
7	Explain the working of Master Slave flip jk flop using diagram	Remember	CO 5	AEC008.14
8	Explain the working of clocked T flip flop.	Understand	CO 5	AEC008.14
9	Construct a JK flip flop using a D flip flop .	Remember	CO 5	AEC008.14
10	Design 16 bit adder using two 7483 ICs.	Remember	CO 5	AEC008.12
11	Compare synchronous counters and asynchronous counters.	Understand	CO 5	AEC008.15
12	Draw and explain the operation 4 bit asynchronous down counter with timing diagrams.	Remember	CO 5	AEC008.15
13	Explain and design asynchronous MOD 10 (decade) counter.	Remember	CO 5	AEC008.15
14	Explain the operation of universal shift register using IC 74194 with logic diagram.	Remember	CO 5	AEC008.15
15	Explain the operation ring counter using truth table and timing diagrams.	Understand	CO 5	AEC008.15
16	Design and explain the 3 to 8 decoder using 2 to 4 decoders.	Remember	CO 5	AEC008.12
17	Implement 16x1 Multiplexer using 8x1 Multiplexers and 2x1 Multiplexer.	Understand	CO 5	AEC008.15
18	Using D-Flip flops and waveforms explain the working of a 4-bit SISO shift register.	Remember	CO 5	AEC008.15
19	Using a suitable logic diagram explain the working of a 1-to-8 de multiplexer.	Remember	CO 5	AEC008.15
20	What is a half-adder? Explain a half-adder with the help of truth-table and logic diagram.	Remember	CO 5	AEC008.15
Part - C (Analytical Questions)				

S.No	QUESTION	Blooms taxonomy level	Course Outcomes	Course Learning Outcomes
1	Implement the following function with 8: 1 MUX (74XX151) and two 4X1 MUX. $F(W,X,Y,Z) = \sum m (2,4,6,7,10,11,12,13,14)$	Remember	CO 5	AEC008.12
2	Design an 8 bit adder using two 4 bit parallel adders IC74283.	Understand	CO 5	AEC008.12
3	Design 4 to 16 decoder using two 74X138 decoders.	Remember	CO 5	AEC008.12
4	Realize the following expression using 74X151 ICs and 74X139 IC $F(Z)=A^1BCD+AB^1CD+ABC^1D+A^1BDE+ACDE^1+AB^1CE+AB CD^1$	Remember	CO 5	AEC008.12
5	Design 4 bit up/down ripple counter with a control for up/down counting.	Understand	CO 5	AEC008.15
6	Determine f_{max} for 4 bit synchronous counter if t_{pd} for each flip flop is 50 ns and t_{pd} for each AND gate is 20 ns. Compare this with f_{max} for a MOD-16 ripple counter.	Remember	CO 5	AEC008.15
7	Design divide by 20 counter using IC 7490 and also draw the internal architecture of IC 7490.	Remember	CO 5	AEC008.15
8	Explain any two applications of counters in detail.	Understand	CO 5	AEC008.15
9	How many flip flops are required to design binary counter that counts from 0 to 1023 and also determine the frequency at which output of last (MSB) flip flop for an input clock frequency of 2 Mhz.	Remember	CO 5	AEC008.15
10	Draw the timing diagrams at the output of each flip flop if each flip flop has propagation delay of 20 ns	Remember	CO 5	AEC008.14
11	Design a 4 bit ,4 state ring counter using 74X194 with neat timing diagrams.	Understand	CO 5	AEC008.15

Prepared By:

Ms. P Saritha, Assistant Professor

HOD, ECE