INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

TUTORIAL QUESTION BANK

Course Title	**DIGITAL SIGNAL PROCESSORS AND ARCHITECTURE**				
Course Code	**AEC507**				
Programme	B. Tech				
Semester	VIII	ECE			
Course Type	Elective				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	-	3	-	-
Chief Coordinator	Mrs. C.Devisupraja, Assistant Professor, ECE				
Course Faculty	Mrs. C.Devisupraja, Assistant Professor, ECE				

COURSE OBJECTIVES

The course should enable the students to:	
I	Impart the knowledge of basic DSP concepts and number systems to be used, different types of A/D, D/A conversion errors.
II	Learn the architectural differences between DSP and General purpose processor.
III	Learn about interfacing of serial & parallel communication devices to the processor.
IV	Implement the DSP & FFT algorithms.

COURSE OUTCOMES (COs):

CO 1	Understand the basics of Digital Signal Processing and transforms.
CO 2	Able to distinguish between the architectural features of General purpose processors and DSP processors.
CO 3	Understand the architectures of TMS320C54xx devices and Acquire knowledge about various addressing modes of DSP TMS320C54XX.
CO 4	Discuss about various memory and parallel I/O interfaces.
CO 5	Design and implement basic DSP algorithms.

COURSE LEARNING OUTCOMES (CLOs):

Students, who complete the course, will have demonstrated the ability to do the following:

AEC507.01	Understand how digital to analog (D/A) and analog to digital (A/D) converters operate on a signal and be able to model these operations mathematically.
AEC507.02	Understand the inter-relationship between DFT and various transforms.
AEC507.03	Understand the IEE-754 floating point and source of errors in DSP implementations.
AEC507.04	Understand the fast computation of DFT and appreciate the FFT Processing.
AEC507.05	Understand the concept of multiplier and multiplier Accumulator.
AEC507.06	Design SMID ,VLIW architectures.
AEC507.07	Understand the modified bus structures and memory access in PDSPs.
AEC507.08	Understand the special addressing modes in PDSPs.
AEC507.09	Understand the architecture of TMS320C54XX DSPs.
AEC507.10	Understand the addressing modes and memory space of TMS320C54XX DSPs.
AEC507.11	Understand the various interrupts and pipeline operation of TMS320C54XX processors.
AEC507.12	Analyze the Program control, instruction set and programming.
AEC507.13	Understand the concept of on-chip Peripherals.
AEC507.14	Understand the significance of memory space organization.
AEC507.15	Analyze external bus interfacing signals.
AEC507.16	Explain about parallel I/O interface, programmed I/O.
AEC507.17	Understand the significance of Interrupts and Direct Memory Access.
AEC507.18	Understand the basic concepts of convolution and correlation.
AEC507.19	Compare the characteristics of IIR and FIR filters.
AEC507.20	Analyze the concepts of interpolation and decimation filters.

TUTORIAL QUESTION BANK

S.No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course Learning Outcomes
UNIT-I INTRODUCTION TO DIGITAL SIGNAL PROCESSING				
Part - A(Short Answer Questions)				
1	Define Discrete Fourier Transform (DFT)and Inverse DFT of a discrete time sequence.	Remember	CO 1	AEC507.01
2	List any four properties of DFT	Remember	CO 1	AEC507.02
3	What do you understand by circular convolution	Remember	CO 1	AEC507.01
4	What is zero padding? What are its uses?	Understand	CO 1	AEC507.03
5	What is meant by radix-2 Fast Fourier transform (FFT)?	Understand	CO 1	AEC507.01
6	What are the applications of FFT algorithm	Remember	CO 1	AEC507.02
7	Distinguish between linear convolution and circular convolution of two sequences.	Remember	CO 1	AEC507.01

S.No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course Learning Outcomes
8	What are the differences and similarities between Decimation in Frequency Transform (DIF) and Decimation in Time (DIT) algorithms.	Understand	CO 1	AEC507.03
9	What is meant by in place computation in DIT and DIF FFT algorithm?	Understand	CO 1	AEC507.02
10	How to obtain same result from linear convolution and circular convolution?	Understand	CO 1	AEC507.02
11	What is the disadvantage of direct computation of DFT	Remember	CO 1	AEC507.02
12	What is the way to reduce number of arithmetic operations during DFT computation	Remember	CO 1	AEC507.03
13	What are the properties of twiddle factor?	Remember	CO 1	AEC507.04
14	Explain the importance of butterfly computation for computing of DFT using FFT algorithm?	Remember	CO 1	AEC507.04
15	Draw the basic butterfly diagram for DIT FFT and DIF FFT algorithm.	Remember	CO 1	AEC507.04
16	What is the need of aliasing filter before A/D conversion?	Understand	CO 1	AEC507.04
17	What is bias in IEEE 754 format?	Understand	CO 1	AEC507.05
18	How can we reduce the amplitude error in D/A conversion?	Remember	CO 1	AEC507.05
19	What is IEEE 754 floating point representation ?	Understand	CO 1	AEC507.05
20	List various sources of error in DSP implementations?	Understand	CO 1	AEC507.05
Part - B (Long Answer Questions)				
1	Explain the scheme of the DSP system with a neat diagram?	Understand	CO 1	AEC507.01
2	What is DSP? What are the important issues to be considered in designing and implementing a DSP system? Explain in detail	Understand	CO 1	AEC507.02
3	Why signal sampling is required? Explain the sampling process?	Understand	CO 1	AEC507.02
4	List out the differences between Convolution and correlation	Understand	CO 1	AEC507.03
5	List the major architectural features used in DSP system to achieve high speed program execution?	Remember	CO 1	AEC507.03
6	Assuming X(K) as a complex sequence determine the number of complex real multiplies for computing IDFT using direct and Radix-2 FT algorithms?	Understand	CO 1	AEC507.03
7	Explain about A/D conversion errors in a DSP system and derive expressions for mean, variance and SNR?	Understand	CO 1	AEC507.04
8	Explain about the different number formats for signals &coefficients?	Remember	CO 1	AEC507.04
9	Compute the dynamic range and percentage resolution of Signal that uses a) 16 point Fixed point format b) 32 point floating Point with 24 bits for the mantissa and 8 bits for the exponent?	Remember	CO 1	AEC507.04
10	Calculate the dynamic range and precision of each of the following number representation formats a) 48 bit double precision fixed point format b) a floating point format with a 16 bit mantissa and a 8 bit exponent?	Remember	CO 1	AEC507.04

S.No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course Learning Outcomes
11	Explain the term Aliasing with an illustration .How can Aliasing be overcome in a DSP system?	Understand	CO 1	AEC507.03
12	Explain the architectural differences between DSP processors and Microprocessors?	Understand	CO 1	AEC507.03
13	Explain Different number formats in DSP?	Remember	CO 1	AEC507.03
14	Explain the significance of Fast Transform techniques. What are the advantages over DFT?	Remember	CO 1	AEC507.02
15	Find DFT of a sequence x(n) = { 0,1,1,-1,,-1,0,-1,1} using DIFFFT algorithm.	Understand	CO 1	AEC507.01
16	Explain the importance of butterfly computation for computing of DFT using FFT algorithm?	Understand	CO 1	AEC507.03
17	Compute the eight-point DFT of the following sequence by using DIT and DIF algorithm x (n) = 1 $0 \leq n \leq 7$ = 0 otherwise	Understand	CO 1	AEC507.03
18	Compute an 8 point DFT of the sequence x (n) = (1, 0, 1, -1, 1, -1, 0, 1).	Remember	CO 1	AEC507.03
19	Explain about the concept of frequency sampling for developing discrete Time Fourier Transform.	Remember	CO 1	AEC507.02
20	What are the differences and similarities between DIT and DIF FFT algorithms?	Understand	CO 1	AEC507.01
	Part - C (Analytical Questions)			
1	Write short Notes on Analysis and Design tools for DSP?	Understand	CO 1	AEC507.01
2	Write short notes on, i. Bit reversal order ii.Inplace computation	Understand	CO 1	AEC507.02
3	Compute the linear convolution of finite duration sequences h (n) = {1, 2} and x(n) = {1, 2, -1, 2,3, -2, -3, -1, 1, 1, 2, -1 } by overlap add method.	Understand	CO 1	AEC507.03
4	Find the output y(n) of a filter whose impulse response is h(n) = {1, 1, 1 } and input signal x(n) = {3, -1, 0,1,3,2,0,1,2,1} overlap save method.	Understand	CO 1	AEC507.04
5	Determine the convolution of the pairs of signals by means of z-transform X1(n)=(1/2)n u(n), X2(n)= cosπn u(n)	Understand	CO 1	AEC507.04
6	State and prove the properties of DFT?	Understand	CO 1	AEC507.03
7	Let x(n), for $0 \leq n \leq N-1$, be a real N-point signal. The DFT coefficients are X(k), for $0 \leq k \leq N-1$. (a) Show that X(0) is a real number. (b) Assume N is an even number. Is X(N/2) real, imaginary, or a generic complex number?	Understand	CO 1	AEC507.03
8	consider the N-point sequence x(n) defined for n= 0,...,N−1. Show that if x(n) is real, then the N-point DFTX(k) satisfies X(N−k) =X(k), k= 0,...,N−1,(1)where the over line notation denotes the complex conjugate	Remember	CO 1	AEC507.03
9	Sketch the signal x = sin(2*pi*[0:7]/8);and find the DFT of x. Do not use direct computation of the DFT.	Remember	CO 1	AEC507.02
10	Find the DFT of the N-point discrete-time signal, x(n) = cos(2πNn+θ), n= 0,1,...,N−1.	Understand	CO 1	AEC507.01

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UNIT-II ARCHITECTURE OF PROGRAMMABLE DSPs				
Part - A (Short Answer Questions)				
1	What is the role of Barrel shifter in Programmable DSP?	Remember	CO 2	AEC507.06
2	Explain guard bits in a MAC unit of Programmable DSP.	Remember	CO 2	AEC507.06
3	List the various Applications of Programmable DSP.	Remember	CO 2	AEC507.06
4	What are the types of Programmable DSPs	Understand	CO 2	AEC507.06
5	What are the Specialized addressing modes in Programmable DSPs	Understand	CO 2	AEC507.06
6	Write about Circular Buffers of Programmable DSPs	Understand	CO 2	AEC507.07
7	Define Harvard architecture of Programmable DSP Processors	Understand	CO 2	AEC507.07
8	List the architectural features of Programmable DSP Processors.	Remember	CO 2	AEC507.07
9	Write about Bit-reversed addressing of Programmable DSPs	Remember	CO 2	AEC507.07
10	Draw the VLIW architecture.	Remember	CO 2	AEC507.07
11	List the advantages of VLIW architecture.	Understand	CO 2	AEC507.08
12	List the disadvantages of VLIW architecture.	Remember	CO 2	AEC507.08
13	What is pipelining technique?	Remember	CO 2	AEC507.08
14	What are the different stages in pipelining?	Remember	CO 2	AEC507.08
15	Draw the SIMD architecture.	Understand	CO 2	AEC507.08
16	Define underflow condition	Remember	CO 2	AEC507.08
17	Define overflow condition	Remember	CO 2	AEC507.05
18	List out various special Addressing modes	Remember	CO 2	AEC507.05
19	Explain working of bit reversed Addressing mode	Understand	CO 2	AEC507.05
20	Explain About Indirect Addressing mode	Remember	CO 2	AEC507.05
Part - B (Long Answer Questions)				
1	What are the DSP computational building blocks? Explain with diagrams any two of them.	Understand	CO 2	AEC507.06
2	Explain with a neat diagram the functioning of a Barrel Shifter.	Understand	CO 2	AEC507.06
3	Discuss in detail about the concept of Multiplier?	Understand	CO 2	AEC507.06
4	Discuss in detail about the concept of Parallel Multiplier?	Understand	CO 2	AEC507.06
5	Explain the structure of a 4x4 Braun Multiplier?	Remember	CO 2	AEC507.07

S.No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course Learning Outcomes
6	Explain the concept of Multiply and Accumulate unit?	Understand	CO 2	AEC507.07
7	Illustrate the concept of Shifter?	Understand	CO 2	AEC507.07
8	Explain in detail about overflow and under flow conditions?	Understand	CO 2	AEC507.07
9	Explain the concept of saturation logic in detail?	Remember	CO 2	AEC507.07
10	Explain the concept of ALU in DSPs?	Understand	CO 2	AEC507.08
11	Discuss in detail about the Bus Architecture and memory?	Understand	CO 2	AEC507.08
12	Explain the concept of On-Chip Peripherals?	Remember	CO 2	AEC507.08
13	Explain the concept of Data Addressing capabilities	Understand	CO 2	AEC507.08
14	Explain the Special Addressing Modes?	Understand	CO 2	AEC507.08
15	Explain in detail about Address Generation unit?	Remember	CO 2	AEC507.08
16	Explain in detail about Multiport Memory	Remember	CO 2	AEC507.05
17	Illustrate about SMID Architecture	Understand	CO 2	AEC507.04
18	Illustrate about VLIW Architecture	Understand	CO 2	AEC507.05
19	Explain about circular addressing mode of Programmable DSP Processors?	Remember	CO 2	AEC507.06
20	Describe the Harvard architecture of Programmable DSP Processors.	Remember	CO 2	AEC507.06
Part - C (Analytical Questions)				
1	Explain in detail about the on chip peripherals and processor benchmarking	Remember	CO 2	AEC507.06
2	Explain the function of a MAC unit and also explain how overflow and underflow conditions can be avoided in MAC operations.	Understand	CO 2	AEC507.06
3	Explain what is meant by instruction pipelining. How pipelining increases the throughput efficiency	Remember	CO 2	AEC507.07
4	Consider a MAC unit whose inputs are 16 bit numbers. If 256 products are to be summed up in this MAC, how many guard bits should be provided for the accumulator to prevent overflow condition from occurring?	Remember	CO 2	AEC507.08
5	Describe the Applications of Programmable DSP Processors	Remember	CO 2	AEC507.06
6	Explain about circular addressing mode of Programmable DSP Processors?	Understand	CO 2	AEC507.06
7	Explain the assembly instructions memory addressing of VLIW processor with examples.	Remember	CO 2	AEC507.07
8	Describe the advantages and disadvantages of VLIW architecture	Remember	CO 2	AEC507.08
9	Explain the implementation of 4-bit shift right barrel shifter, with a diagram.	Remember	CO 2	AEC507.06

S.No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course Learning Outcomes
10	If a sum of 256 products is to be computed using a pipelined MAC unit, and if the MAC execution time of the unit is 100nsec, what will be the total time required to complete the operation?	Remember	CO 2	AEC507.08
UNIT-III OVERVIEW OF TMS320C54XX PROCESSOR				
Part - A (Short Answer Questions)				
1	Define Accumulator	Remember	CO 3	AEC507.09
2	Define Multiplier	Remember	CO 3	AEC507.09
3	Define Shifter	Understand	CO 3	AEC507.09
4	Define Immediate addressing Mode	Remember	CO 3	AEC507.09
5	Define Absolute addressing Mode	Understand	CO 3	AEC507.09
6	Define Accumulator addressing Mode	Understand	CO 3	AEC507.09
7	Define Direct addressing Mode	Understand	CO 3	AEC507.09
8	Define Indirect addressing Mode	Understand	CO 3	AEC507.09
9	Define Memory mapped addressing Mode	Remember	CO 3	AEC507.09
10	Define Stack addressing Mode	Remember	CO 3	AEC507.10
11	List Various Addressing Modes	Remember	CO 3	AEC507.10
12	Define Circular Addressing Mode	Remember	CO 3	AEC507.10
13	Define opcode field in Dual-Operand Addressing	Understand	CO 3	AEC507.10
14	Define XMOD field in Dual-Operand Addressing	Remember	CO 3	AEC507.10
15	Define XAR field in Dual-Operand Addressing	Understand	CO 3	AEC507.11
16	Define YMOD field in Dual-Operand Addressing	Remember	CO 3	AEC507.11
17	Define YAR field in Dual-Operand Addressing	Remember	CO 3	AEC507.11
18	Define Program Control	Understand	CO 3	AEC507.11
19	Define Stack Pointer	Remember	CO 3	AEC507.11
20	Define Status Register	Understand	CO 3	AEC507.11
Part - B (Long Answer Questions)				
1	Explain the functional Block diagram of the TMS320C54XX Processor	Remember	CO 3	AEC507.11
2	Explain the functional Diagram of CPU of the TMS320C54XX Processor	Understand	CO 3	AEC507.09
3	Explain the functional Diagram of barrel Shifter of the TMS320C54XX Processor	Remember	CO 3	AEC507.09

S.No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course Learning Outcomes
4	Explain the functional Diagram of Adder unit /Multiplier of the TMS320C54XX Processor	Remember	CO 3	AEC507.10
5	Illustrate the concept of Internal memory and memory mapped Registers of the TMS320C54XX Processor	Understand	CO 3	AEC507.09
6	Illustrate the concept of Data Addressing modes of TMS320C54XX Processor		CO 3	AEC507.10
7	Explain in detail about Direct Addressing mode of the TMS320C54XX Processor	Understand	CO 3	AEC507.11
8	Explain in detail about Indirect Addressing mode of the TMS320C54XX Processor	Understand	CO 3	AEC507.11
9	Explain in detail about Indirect Addressing mode of the TMS320C54XX Processor using Dual memory operands	Understand	CO 3	AEC507.10
10	Write a sequence of TMS320C54xx instructions to configure a circular buffer with a start address at 0200h and an end address at 021fh with current buffer pointer (AR6) pointing to address 0205h.	Understand	CO 3	AEC507.10
11	What will be the contents of accumulator A after the execution of the instruction LD * AR4, 4, A if the current AR4 points to a memory location whose contents are 8b0eh and the SXM bit of the status register STI is set?	Understand	CO 3	AEC507.10
12	Briefly explain about program control unit of TMS320C54XX processor	Understand	CO 3	AEC507.10
13	Explain about memory space of the TMS320C54XX processor	Understand	CO 3	AEC507.11
14	Explain in detail about memory map for the TMS320C54XX processor	Remember	CO 3	AEC507.11
15	Explain in detail about Circular Addressing mode of the TMS320C54XX Processor	Remember	CO 3	AEC507.11
16	Explain in detail about Bit reversed Addressing mode of the TMS320C54XX Processor	Understand	CO 3	AEC507.12
17	Assuming the current content of AR3 to be 200h, what will be its contents after each of the following TMS320C54xx addressing modes is used? Assume that the contents of AR0 are 20h.	Understand	CO 3	AEC507.12
18	Assume that the current content of AR3 is 400h, what will be its contents after each of the following. Assume that the content of AR0 is 40h.	Understand	CO 3	AEC507.13
19	Differentiate between stack and pipeline.	Remember	CO 3	AEC507.13
20	Describe the following on-chip peripherals of TMS320C54xx processors. (a) Hardware Timer (b) Host port interface	Remember	CO 3	AEC507.13
Part - C (Analytical Questions)				
1	With an example each, explain immediate, absolute, and direct addressing mode.	Remember	CO 3	AEC507.11
2	Compare architectural features of TMS320C25 and DSP6000 fixed point digital signal processors.	Understand	CO 3	AEC507.09
3	Briefly describe the following instructions of TMS320C54XX processors with an example. i) MAC *AR5, +*AR6+, A, B ii) RPT Smem iii) RPTB Pmad iv) BANZ	Remember	CO 3	AEC507.10
4	Explain the 6 level pipeline operation of TMS320C54XX	Remember	CO 3	AEC507.11
5	Assuming the current content of AR3 to be 220h, what will be its contents after each of the following TMS320C54xx addressing modes is used? Assume that the contents of AR0	Understand	CO 3	AEC507.11

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	are 10h. a. *AR3+0 b. *AR3-0 c. *AR3+ d. *AR3 e. *AR3 - f. *+AR3 (40h)			
6	Explain the PMST register of TMS320C54XX Processor	Understand	CO 3	AEC507.12
7	Explain the Pipeline Operation of the below given sequence of instructions. Indicate the contents of registers AR1,T and accumulator A after the completion of each cycle.The initial values of AR1,AR3,AR4 and A are 2000h,1000h,400h and 0 respectively. The contents of memory location 2000h,1000h and 400h are 9,5 and 8 respectively. LD *AR1+,A MPY *AR3,*AR4,A STH A,*AR1	Understand	CO 3	AEC507.11
8	Describe the operation of the following with respect to C54XX processor i) MAS*AR3- , * AR4+ ,B,A ii)LD *AR4,4,A iii)MPY #01234,A iv)MPY v)STH A,1,*AR1	Understand	CO 3	AEC507.13
9	Describe host port interface and explain its signals?	Remember	CO 3	AEC507.11
10	Explain about On-chip Peripherals in detail?	Remember	CO 3	AEC507.11
UNIT-IV INTERFACING MEMORY AND I/O PERIPHERALS TO PDSPs				
Part - A (Short Answer Questions)				
1	What are interrupts?	Understand	CO 4	AEC507.14
2	Describe DMA with respect to TMS320C54XX processors	Remember	CO 4	AEC507.14
3	Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode	Remember	CO 4	AEC507.15
4	Explain the memory interface block diagram for the TMS 320 C54xx processor	Remember	CO 4	AEC507.15
5	Draw the I/O interface timing diagram for read – write read sequence of operation.	Remember	CO 4	AEC507.14
6	List various external bus interfacing signals.	Remember	CO 4	AEC507.16
7	Write short notes on memory interfacing	Remember	CO 4	AEC507.15
8	Discuss parallel I/O interface.	Remember	CO 4	AEC507.14
9	Write short notes on programmed I/O	Understand	CO 4	AEC507.14
10	Give the advantages of DMA	Understand	CO 4	AEC507.16
11	Give the disadvantages of DMA	Remember	CO 4	AEC507.14
12	Discuss Serial Interface	Understand	CO 4	AEC507.16
13	Difference between serial Interface and Parallel Interface	Remember	CO 4	AEC507.14
14	Define Fetch unit	Understand	CO 4	AEC507.14

S.No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course Learning Outcomes
15	Define Execute unit	Understand	CO 4	AEC507.14
16	Define Decode unit	Remember	CO 4	AEC507.15
17	Define a register	Understand	CO 4	AEC507.15
18	Define Flag	Understand	CO 4	AEC507.15
19	Define Interrupt Flag Register	Understand	CO 4	AEC507.15
20	Define Interrupt Mask Register	Remember	CO 4	AEC507.15
Part – B (Long Answer Questions)				
1	Explain in detail about memory space organization?	Understand	CO 4	AEC507.15
2	Explain about Bus Interfacing Signals?	Remember	CO 4	AEC507.14
3	Describe Memory interface for TMS320C5416 Processor	Understand	CO 4	AEC507.14
4	Draw the timing diagram for memory interface for read-read-write sequence of operation. Explain the purpose of each signal involved?	Understand	CO 4	AEC507.15
5	How does DMA help in increasing the processing speed of a DSP processor?	Remember	CO 4	AEC507.16
6	Briefly explain parallel I/O interface?	Understand	CO 4	AEC507.14
7	Write short notes on the following a. Basic peripherals b. DMA	Remember	CO 4	AEC507.15
8	Briefly Explain the programmed I/O in TMS320C54XX Processor?	Understand	CO 4	AEC507.14
9	Design a data memory system with address range 00800h-000FFFh for a C5416. Use 2k x 8 RAM memory chips	Understand	CO 4	AEC507.14
10	Interface 8k x 16 ROM to the C5416 DSP in the address range 7FE000h-7FFFFFh	Remember	CO 4	AEC507.15
11	Briefly explain Programmed I/O Interface?	Understand	CO 4	AEC507.14
12	Explain about Register Sub Address Technique?	Remember	CO 4	AEC507.17
13	Design an interface to connect a 64K x 16 flash memory to a TMS320C54XX processor. The processor address bus to be used is A0-A15	Understand	CO 4	AEC507.15
14	Explain instruction set of TMS320C54XX Processor	Understand	CO 4	AEC507.15
15	write an assembly language program of TMS320C54XX processors to compute the sum of three product terms given by the equation y(n)=h(0)x(n)+h(1)x(n-1)+h(2)x(n-2) with usual notations. Find y (n) for signed 16 bit data samples and 16 bit constants.	Remember	CO 4	AEC507.17
16	Explain the operation of serial I/O ports and hardware timer of TMS320C54XX on chip peripherals	Understand	CO 4	AEC507.14
17	Write short notes on Flash memory interface to the DSP Processor	Understand	CO 4	AEC507.16
18	Differentiate between Serial I/O interface and parallel I/O interface	Remember	CO 4	AEC507.17

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19	Design a circuit to interface 4K x 16 and a 2K x 16 memory chip to realize program memory space for the TMS320C54xx processor in the address Ranges 03F000h-03FFFFh and 05F800h-05FFFFh, respectively.	Understand	CO 4	AEC507.14
20	Is it possible to connect a memory device without Decode (interfacing) Circuit? If so, connect 8k x 16 SRAM to TMS320C54xx. What are the merits & demerits of the solution?	Remember	CO 4	AEC507.15
Part - C (Analytical Questions)				
1	Design a circuit to interface 64k words of the program memory space from 0FFFFFh to 0F0000h for the TMS320C5416 processor using 16K x 16 memory chips	Understand	CO 4	AEC507.14
2	Define interrupt. Write a flow chart of interrupt handling by C54xx processor.	Understand	CO 4	AEC507.15
3	Design an interface to connect flash memory to a TMS320C54XX processor. The processor address bus is A_0-A_{15}	Understand	CO 4	AEC507.17
4	Draw the I/O interface timing diagram for read write read sequence of operation and also explain the signals that are involved in an I/O transaction.	Understand	CO 4	AEC507.17
5	Describe DMA with respect to TMS320C54XX processors.	Understand	CO 4	AEC507.15
6	Discuss in detail the interrupt handling in the C54XX processor.	Understand	CO 4	AEC507.16
7	Explain the use of DMA Register. Write code to show how the DMA channel 5 context registers can be initialized. Choose arbitrary values to be written in the registers.	Understand	CO 4	AEC507.15
8	Write short notes on (a) Direct Memory Access (b) Flash Memory Interface to DSP Processor.	Understand	CO 4	AEC507.16
9	What are interrupts? How interrupts are handled by C54xx DSP Processors.	Understand	CO 4	AEC507.14
10	Explain with example the flash memory interface for the TMS320C54XX DSP.	Understand	CO 4	AEC507.16
UNIT-V IMPLEMENTATIONS OF BASIC DSP ALGORITHMS				
Part - A (Short Answer Questions)				
1	Define Q-Notation	Understand	CO 5	AEC507.18
2	Define Decimation	Understand	CO 5	AEC507.18
3	Define Interpolation	Understand	CO 5	AEC507.18
4	Define Filter	Understand	CO 5	AEC507.18
5	Define FIR Filter	Understand	CO 5	AEC507.19
6	Define IIR Filter	Understand	CO 5	AEC507.19
7	Define FFT	Remember	CO 5	AEC507.19
8	Define DFT	Remember	CO 5	AEC507.19
9	Define DIT-FFT	Understand	CO 5	AEC507.19
10	Define DFT-FFT	Remember	CO 5	AEC507.19

S.No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course Learning Outcomes
11	Difference Between DFT and FFT	Remember	CO 5	AEC507.19
12	Difference Between DIT-FFT and DIF-FFT	Understand	CO 5	AEC507.18
13	Difference Between IIR and FIR Filters	Remember	CO 5	AEC507.19
14	Difference Between DIT-FFT and DIF-FFT	Understand	CO 5	AEC507.18
15	Difference Between Decimation and Interpolation	Remember	CO 5	AEC507.19
16	Draw the Block Diagram of Decimation	Remember	CO 5	AEC507.19
17	Draw the Block Diagram of Interpolation	Remember	CO 5	AEC507.19
18	Define Sampling	Understand	CO 5	AEC507.20
19	Define up-sampling	Remember	CO 5	AEC507.20
20	Define Down-Samplings	Understand	CO 5	AEC507.20
Part – B (Long Answer Questions)				
1	Explain in detail about Q-Notation	Understand	CO 5	AEC507.18
2	Explain in detail about FIR filters in DSP implementation	Understand	CO 5	AEC507.19
3	Implementation of FIR filter of the TMS320C54XX processor	Remember	CO 5	AEC507.18
4	Explain in detail about IIR filters in DSP implementation	Remember	CO 5	AEC507.18
5	Implementation of second order IIR filter of the TMS320C54XX processor	Understand	CO 5	AEC507.19
6	Explain in detail about Interpolation filter	Understand	CO 5	AEC507.18
7	Explain in detail about Decimation filter	Understand	CO 5	AEC507.19
8	Explain in detail about FFT algorithm for DFT computation	Remember	CO 5	AEC507.20
9	Explain in detail about 2-Point DFT computation of TMS320C54XX processor	Remember	CO 5	AEC507.18
10	Write short notes on Overflow and Scaling	Understand	CO 5	AEC507.18
11	Mention the procedure to implement 8-point FFT algorithm on TMS320C54XX processor	Understand	CO 5	AEC507.19
12	Write a pseudo code to determine 8 point DFT using DIT-FFT algorithm invoking butterfly subroutine in a nested loop for each stage?	Remember	CO 5	AEC507.19
13	Explain in detail about 4-Point DFT computation of TMS320C54XX processor	Remember	CO 5	AEC507.18
14	Explain about Bit reversed Indexed Generation of TMS320C54XX processor	Understand	CO 5	AEC507.18
15	What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and polyphase sub filter	Understand	CO 5	AEC507.19

S.No	QUESTION	Blooms Taxonomy Level	Course Outcomes	Course Learning Outcomes
16	Explain with the help of a block diagram and mathematical equations the implementation of a second order IIR filter. No program code is required.(	Understand	CO 5	AEC507.18
17	Determine the value of each of the following 16- bit numbers represented using the given Q- notations: (i) 4400h as a Q10 number (ii) 4400h as a Q7 number (iii) 0.3125 as a Q15 number (iv) - 0.3125 as a Q15 number.	Remember	CO 5	AEC507.18
18	Explain how the bit reversed index generation can be done in 8 pt FFT. Also write a TMS320C54xx program for 8 pt DIT-FFT bit reversed index generation. .	Understand	CO 5	AEC507.19
19	Determine the following for a 128-point FFT computation: (i) number of stages (ii) number of butterflies in each stage (iii) number of butterflies needed for the entire computation (iv) number of butterflies that need no twiddle factors (v) number of butterflies that require real twiddle factors (vi) number of butterflies that require complex twiddle factors.	Understand	CO 5	AEC507.19
20	Determine the number of stages and number of butterflies in each stage and the total number of butterflies needed for the entire computation of 512 point FFT	Understand	CO 5	AEC507.20
	Part - C (Analytical Questions)			
1	Write a program to multiply two Q15 numbers i.e N1*N2=N1xN2 where N1 and N2 are 16 bit numbers & N1xN2 is the 16 bit result in Q15 notation	Remember	CO 5	AEC507.18
2	What values are represented by the 16-bit fixed point number=4000h in the Q15 and Q7 notations	Remember	CO 5	AEC507.19
3	Implementation of Interpolating FIR filter. The filter length is 15 and the interpolating factor is 5.It implements the equation y(m)=h(10)x(n-2)+h(5)x(n-1)+h(0)x(n)……lly y(m+1)……y(m+4)= h(14)x(n-2)+h(9)x(n-1)+h(4)x(n)	Remember	CO 5	AEC507.20
4	Implementation of an 8-point FFT of the TMS320C54XX processor	Understand	CO 5	AEC507.20
5	Derive the optimum overflow and scaling in DIT-FFT Algorithm	Understand	CO 5	AEC507.20
6	Write a program for signal spectrum in DIT-FFT Algorithm using TMS320C54XX processor	Remember	CO 5	AEC507.18
7	Write a program for Butterfly computation in DIT-FFT Algorithm using TMS320C54XX processor	Remember	CO 5	AEC507.19
8	Explain in detail about Decimation in Time and Decimation in Frequency FFT Algorithms	Remember	CO 5	AEC507.20
9	Describe the importance of Q-notation in DSP algorithm implementation with examples. What are the values represented by 16- bit fixed point number N=4000h in Q15, Q10, Q7 notations?	Understand	CO 5	AEC507.20
10	How many add/subtract and multiply operations are needed to compute the butterfly structure?	Remember	CO 5	AEC507.18

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