INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

ELECTRONICS AND COMMUNICATION ENGINEERING

TUTORIAL QUESTION BANK

Course Title	**VLSI DESIGN**				
Course Code	AEC017				
Programme	B.Tech				
Semester	VII	ECE			
Course Type	Core				
Regulation	IARE - R16				
Course Structure	**Theory**			**Practical**	
	Lectures	**Tutorials**	**Credits**	**Laboratory**	**Credits**
	3	1	4	3	2
Chief Coordinator	Ms. K S Indrani , Assistant Professor				
Course Faculty	Mr. V R Seshagiri Rao , Associate Professor Dr. V Vijay, Associate Professor Dr. M Manisha, Associate Professor				

COURSE OBJECTIVES:

The course should enable the students to:	
I	Have skills to use concepts of MOS devices for the fabrication of integrated chips (IC's).
II	Familiarize CMOS layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
III	Demonstrate the ability to design static CMOS combinational and sequential logic at the transistor level, including mask layout.
IV	Focus in selecting appropriate building blocks of data path for given system.

COURSE OUTCOMES (COs):

CO 1	Explore the basic operations of MOSFET, parameters to be considered which effects the operation of MOS, effect of scaling on MOS devices, how to overcome draw back.
CO 2	Understand various VLSI design styles, fabrication process of MOS, able to analyze the inverter

	characteristics, understand the delay, noise margin and power dissipation of MOS transistor.
CO 3	Use Physical design rules to be followed for MOS designs, understand drawbacks of interconnects reliability issues and the effect of CMOS latch-up.
CO 4	Understand various gate level designs, analyze various performance parameters like area, speed and capacitance and study the Fan-In and Fan-out..
CO 5	Understand design options for common datapath operators, various memories, low power memories. Analyze various timing issues, clocking strategies of VLSI designs and study various digital designs.

COURSE LEARNING OUTCOMES:

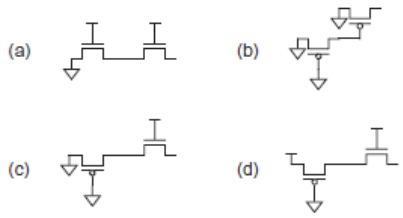
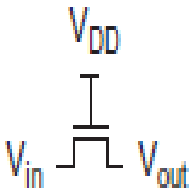
AEC017.01	Understand fundamentals of MOS devices and its V-I characteristics.
AEC017.02	Analyze the effect of parasitic elements on MOS device, effect of threshold voltage MOSFET.
AEC017.03	Understand the importance and effect of scaling on MOS devices; analyze the latest trends in CMOS technology.
AEC017.04	Understand the basic CMOS nano technology and the importance of it.
AEC017.05	Understand the fabrications steps involved in the MOS transistor.
AEC017.06	Study various inverter characteristics of NMOS, CMOS.
AEC017.07	Understand the effect of delay, noise margin and power dissipation of MOS devices.
AEC017.08	Understand implementation of logic designs using MOS transistors series & parallel circuits.
AEC017.09	Study other logic families like pass transistor logic, Bi-CMOS logic, and various pull-up networks
AEC017.10	Understand to implement layers using stick diagram along with the color representation
AEC017.11	Study the design rules of transistors, wires , contacts and layouts with respect to width, length and spacing based on type of technology.
AEC017.12	Understand effects on VLSI Interconnects and electron migration.
AEC017.13	Study the latch up problems and reliability issues of CMOS
AEC017.14	Understand various gate level designs for the logics and study about Fan-In and Fan-out.
AEC017.15	Analyze the effect of various capacitances of MOS devices on propagation delay and study about the reduction of RC values based on the choice of layers in the MOS devices.
AEC017.16	Understand the implementation strategies of VLSI design.
AEC017.17	Understand the design of programmable logic devices and analyze the speed and area tradeoffs.
AEC017.18	Understand data path subsystem designs, array subsystem designs.
AEC017.19	Understand the operation of various static and dynamic latches and registers.
AEC017.20	Analyze the timing issues and the clock strategies of VLSI designs.
AEC017.21	Understand the purpose and operation of Low power memory Circuits
AEC017.22	Study various Synchronous and asynchronous circuit design; understand the operation of static and dynamic latches and registers.

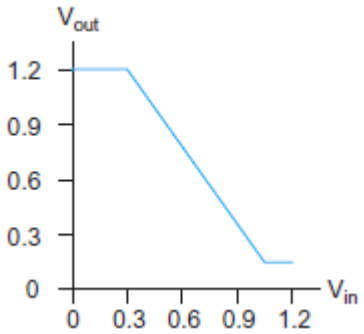
TUTORIAL QUESTION BANK

MODULE-I				
MOSFETS				
PART-A (SHORT ANSWER QUESTIONS)				
S. No	**Questions**	**Blooms Taxonomy Level**	**Course Objective**	**Course learning Outcome**
1	What is sub threshold region	Understand	CO1	AEC017.01
2	Define sub-threshold current	Remember	CO1	AEC017.02
3	What is super threshold region	Understand	CO1	AEC017.02
4	Write down mathematical expression of drain current in saturation region of MOSFET	Remember	CO1	AEC017.01
5	Write down mathematical expression of drain current non saturation region of operation in MOSFET	Remember	CO1	AEC017.01
6	State why nMOS technology is preferred more than PMOS technology	Understand	CO1	AEC017.01
7	What are the operating regions for an MOSFET.	Understand	CO1	AEC017.01
8	Define threshold voltage of MOSFET	Remember	CO1	AEC017.02
9	Define channel length modulation	Remember	CO1	AEC017.02
10	State Moore's Law	Understand	CO1	AEC017.01
11	Compare enhancement and depletion mode of MOSFET	Understand	CO1	AEC017.01
12	What is the effect of scaling on channel resistance ?	Understand	CO1	AEC017.04
13	Why Moore's law is ending?	Understand	CO1	AEC017.04
14	What is BiCMOS technology?	Understand	CO1	AEC017.03
15	How MOSFET is better than BJT?	Understand	CO1	AEC017.01
16	Define body effect	Remember	CO1	AEC017.03
17	Define accumulation of Mos structure?	Understand	CO1	AEC017.01
18	Define inversion of Mos structure?	Understand	CO1	AEC017.01
19	Define depletion of Mos structure?	Understand	CO1	AEC017.01
20	Define gate capacitance?	Understand	CO1	AEC017.01
PART-B (LONG ANSWER QUESTIONS)				
1	Derive the expression for drain current of MOSFET in linear region?	Understand	CO1	AEC017.01
2	Draw V-I characteristics and explain the operation of nMOS enhancement MOSFET.	Understand	CO1	AEC017.01
3	Draw V-I characteristics and explain the operation of nMOS depletion MOSFET.	Remember	CO1	AEC017.01
4	Derive the threshold voltage for NMOS enhancement transistor.	Understand	CO1	AEC017.01
5	Discuss in detail about Short Channel Effects	Remember	CO1	AEC017.04
6	Discuss in detail about the effects of scaling of MOS devices	Understand	CO1	AEC017.04
7	Explain in detail about transistor scaling and any four parameters.	Understand	CO1	AEC017.04
8	Derive the formula for MOS transistor trans-conductance	Understand	CO1	AEC017.01
9	Explain about the projections in VLSI design & technology	Understand	CO1	AEC017.03
10	Explain Bi-CMOS fabrication in an n-well process	Understand	CO1	AEC017.03
11	Write the Comparision between CMOS and bipolar technologies.	Understand	CO1	AEC017.01
12	Illustrate the CMOS inverter DC characteristics and obtain the relationship for output voltage at different	Understand	CO1	AEC017.03

	region in the transfer characteristics.			
13	Explain Enhancement mode transistor action for different cases of Vgs, Vds ?	Understand	CO1	AEC017.01
14	Explain how a bipolar NPN transistor is included in n-well CMOS processing. Draw the cross section of Bi-CMOS.	Understand	CO1	AEC017.03
15	Show mathematically the effect of scaling on gate capacitance, Delay, IDSS and channel resistance.	Understand	CO1	AEC017.04
16	If the threshold of an nMOS transistor is to be raised, Should a positive or negative substrate bias be used? Explain?	Understand	CO1	AEC017.04
17	Briefly Explain about MOSFET parasitic?	Understand	CO1	AEC017.04
18	Briefly Explain about CMOS nanotechnology?	Understand	CO1	AEC017.04
19	Differentiate CMOS technology and nano technology?	Understand	CO1	AEC017.04
20	Demonstrate Accumulation, depletion and inversion of MOS structure with neat diagram?	Understand	CO1	AEC017.04
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)				
1	An nMOS transistor is operating in saturation region with the following parameters. V_{GS} =5V, V_T=1.2V, W/L =10, $\mu_n C_{ox}$=110 μ A/V^2. Find trans-conductance and output conductance of the device.	Understand	CO1	AEC017.01
2	Analyze the effect of scaling on channel résistance and maximum operating frequency	Understand	CO1	AEC017.02
3	Analyze the effect of substrate bias voltage on threshold voltage for n-MOSFET depletion transistor.	Understand	CO1	AEC017.02
4	Consider the nMOS transistor in a 180 nm process with a nominal threshold voltage of 0.4 V and a doping level of 8×1017 cm^{-3}. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 1.1 V instead of 0?	Remember	CO1	AEC017.02
5	Consider an nMOS transistor in a 0.6 μm process with W/L = 4/2 λ (i.e., 1.2/0.6 μm). In this process, the gate oxide thickness is 100 A and the mobility of electrons is 350 cm2/V· s. The threshold voltage is 0.7 V. Plot I_{ds} vs. V_{DS} for V_{GS} = 0, 1, 2, 3, 4, and 5 V.	Understand	CO1	AEC017.02
6	An nMOS transistor is operating in non-saturation region with the following parameters. V_{GS} =4V, V_T=1.0V, W/L =100, $\mu_n C_{ox}$=90 μ A/V^2. Find drain current and drain to source resistance	Understand	CO1	AEC017.01
7	llustrate the relationship between *I*DS versus *V*DS of for various region of operations..	Understand	CO1	AEC017.01
8	A pMOS transistor is operating in non-saturation region with the following parameters. V_{GS} = - 4.5V, V_T = - 1.0V, W/L =95, $\mu_n C_{ox}$=95 μ A/V^2. Find drain current and drain to source resistance.	Understand	CO1	AEC017.02
9	For a CMOS inverter, calculate the shift in the transfer characteristic curve when β_n/β_p ratio is varied from 1/1 to 10/1.	Understand	CO1	AEC017.02
10	An nMOS transistor is operating in saturation region with the following parameters. V_{GS} =5V, V_T=1.2V, W/L =10, $\mu_n C_{ox}$=110 μ A/V^2. Find transconductance of the device.	Understand	CO1	AEC017.01
UNIT-II				
VLSI DESIGN STYLES				
PART-A(SHORT ANSWER QUESTIONS)				
1	State the different types of CMOS processes	Remember	CO2	AEC017.05

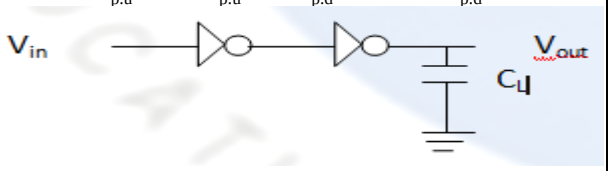
2	Explain about pull down device	Remember	CO2	AEC017.09
3	Explain about pull up device	Remember	CO2	AEC017.09
4	Illustrate the steps involved in twin-tub process	Remember	CO2	AEC017.05
5	List the advantages of CMOS process	Remember	CO2	AEC017.06
6	Draw pass transistor logic symbol for NMOS and PMOS transistor.	Remember	CO2	AEC017.05
7	What is level restorer?	Understand	CO2	AEC017.07
8	What is propagation delay time? Write down mathematical expression for propagation delay?	Understand	CO2	AEC017.07
9	What is rise time	Remember	CO2	AEC017.07
10	What is fall time	Remember	CO2	AEC017.07
11	What is total power consumption?	Remember	CO2	AEC017.07
12	Define leakage power consumption	Understand	CO2	AEC017.07
13	Define switching power consumption	Remember	CO2	AEC017.07
14	Define Short circuit power consumption	Remember	CO2	AEC017.07
15	What are the limitations of nMOS inverter circuit using enhancement mode transistor pullup	Remember	CO2	AEC017.07
16	What are the causes of static power dissipation?	Remember	CO2	AEC017.07
17	Write the expression for total power dissipation?	Remember	CO2	AEC017.07
18	Define short circuit power dissipation?	Remember	CO2	AEC017.07
19	Draw the circuit diagram and characteristic of nMOS depletion mode transistor pull-up?	Remember	CO2	AEC017.08
20	Draw the circuit diagram and transfer characteristic of CMOS transistor pull-up?	Remember	CO2	AEC017.08
PART-B (LONG ANSWER QUESTIONS				
1	Define Noise margin and what is the effect of it on MOS transistor?	Remember	CO2	AEC017.09
2	Explain about NMOS fabrication Process with neat diagrams	Understand	CO2	AEC017.05
3	Explain about PMOS fabrication flow	Understand	CO2	AEC017.05
4	Explain about various masking steps in P-well process of CMOS ?	Understand	CO2	AEC017.05
5	Explain about nMOS inverter operation with neat circuit diagram?	Remember	CO2	AEC017.06
6	Explain about pass transistor logic, what are the advantages and disadvantages of it?	Remember	CO2	AEC017.06
7	Explain the terms figure of merit of MOSFET and output conductance, using necessary equations.	Remember	CO2	AEC017.07
8	Illustrate the CMOS inverter DC characteristics and obtain the relationship for output voltage at different region in the transfer characteristics.	Understand	CO2	AEC017.06
9	Explain the various forms of pull-ups with circuit diagram and characterstics?	Remember	CO2	AEC017.09
10	Draw and explain basic operation of simple Bi-CMOS inverter	Understand	CO2	AEC017.05
11	Briefly explain about static power dissipation with neat diagram?	Remember	CO2	AEC017.07
12	Briefly explain about Dynamic power dissipation ?	Remember	CO2	AEC017.07
13	Derive the expression for V_{in} in terms of β ratio for CMOS inverter and also draw various transfer characteristics for different β ratios?	Remember	CO2	AEC017.06
14	What are the draw backs of simple Bi-CMOS inverter how to overcome the draw backs?	Remember	CO2	AEC017.06
15	Explain about nMOS inverter transfer characterstics with neat diagram?	Remember	CO2	AEC017.06

16	What are the advantages of Bi-CMOS Technology?	Remember	CO2	AEC017.06
17	Explain about various steps in n-well process of CMOS ?	Understand	CO2	AEC017.05
18	Derive the necessary condition for the dimensions of 'Wp and Wn' of CMOS inverter for satisfactory operation	Remember	CO2	AEC017.06
19	For a CMOS inverter, calculate the shift in the transfer characteristic curve when β_n/β_p ratio is varied from 2/1 to 10/1.	Remember	CO2	AEC017.06
20	Derive the equation for rise time for CMOS inverter	Remember	CO2	AEC017.06
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)				
1	Explain the fabrication process of Bi-CMOS by comparing with CMOS fabrication.	Remember	CO2	AEC017.05
2	Explain Bi-CMOS inverter, properties and various forms of Bi-CMOS inverters to overcome drawbacks?	Remember	CO2	AEC017.05
3	Interpret the Pull-up to pull-down ratio (Zpu/Zpd) for an nMOS inverter driven through one or more Pass Transistors.	Remember	CO2	AEC017.05
4	Interpret the Pull-up to pull-down ratio (Z_{pu}/Z_{pd}) for an nMOS inverter driven by another nMOS inverter	Remember	CO2	AEC017.05
5	Explain different series and parallel combinations of pull-up and pull-down networks.	Understand	CO2	AEC017.09
6	Give an expression for the output voltage for the pass transistor networks shown in Figure Neglect the body effect. 	Remember	CO2	AEC017.06
7	Suppose V_{DD}=1.2 V and V_t=0.4 V. Determine V_{out} in Figure for the following. Neglect the body effect. a) Vin =0 V b) Vin =0.6 V c) Vin =0.9 V d) Vin =1.2 V. 	Remember	CO2	AEC017.06
8	For a CMOS inverter, calculate the shift in the transfer characteristic curve when β_n/β_p ratio is varied from 1/1 to 10/1	Understand	CO2	AEC017.06
9	A novel inverter has the transfer characteristics shown in Figure What are the values of *VIL*, *VIH*, *VOL*, and *VOH* that give best noise margins? What are these high and low noise margins?	Understand	CO2	AEC017.07

				
10	Show that Wp = 2.5 Wn for satisfactory operation of CMOS inverter	Remember	CO2	AEC017.06
UNIT-III				
VLSI PHYSICAL DESIGN				
PART-A (SHORT ANSWER QUESTIONS)				
1	Define Stick Diagram ?	Understand	CO3	AEC017.10
2	what is the use of Stick diagram	Remember	CO3	AEC017.10
3	Draw the schematic diagram and stick diagram of nMOS depletion mode inverter?	Remember	CO3	AEC017.10
4	Draw the stick encoding ?	Understand	CO3	AEC017.10
5	What are the properties of stick diagram?	Understand	CO3	AEC017.10
6	Sketch the stick diagram for 2 input nMOS nor gate.	Understand	CO3	AEC017.11
7	List out the components not shown by stick diagram	Understand	CO3	AEC017.10
8	Give the colour representation of various layers?	Understand	CO3	AEC017.10
9	Define hot carriers?	Understand	CO3	AEC017.12
10	Define hot spots?	Understand	CO3	AEC017.12
CIE II				
1	Write a short notes on electron migration?	Understand	CO3	AEC017.12
2	Explain about transistor design rules for NMOS.	Remember	CO3	AEC017.11
3	Design layout diagram for nMOS inverter.	Understand	CO3	AEC017.11
4	What are the remedies to avoid Latch-up?	Remember	CO3	AEC017.13
5	Give Lambda based rules for different layers by specifying its spacing and width?	Remember	CO3	AEC017.11
6	Give Lambda based rules for VDD and VSS contacts?	Understand	CO3	AEC017.11
7	What is the effect of resistance, inductance of a wire on delay?	Remember	CO3	AEC017.12
8	List out all hard errors that causes in Integrated circuits?	Understand	CO3	AEC017.12
9	Write the equation for MTTF and write about each term?	Understand	CO3	AEC017.12
10	Define soft errors?	Understand	CO3	AEC017.12
PART-B(LONG ANSWER QUESTIONS)				
1	Explain clearly the nMOS Design rules with an example.	Understand	CO3	AEC017.11
2	Explain clearly the CMOS Design rules with an example.	Remember	CO3	AEC017.11
3	What are contact cuts? Explain buried and but contacts with cross sectional and top view diagrams	Remember	CO3	AEC017.11
4	Discuss CMOS design style. Compare with NMOS design style.	Understand	CO3	AEC017.11
5	Sketch the transistor level diagram for the expression Y=AB+CD and also draw the corresponding Stick diagram representation using CMOS logic.	Understand	CO3	AEC017.10
6	What is stick diagram and what are Rules for drawing Stick Diagrams?	Understand	CO3	AEC017.10

7	Draw the simple metal nMOS process rules?	Understand	CO3	AEC017.11
8	Draw the encodings for double metal CMOS p-well process ?	Understand	CO3	AEC017.11
9	Explain about Euler's rule for physical design with an example?	Understand	CO3	AEC017.11
10	Explain design rules for wires, n-diffusion, p-diffusion, n-well?	Understand	CO3	AEC017.11
CIE-II				
1	Explain the latch up in CMOS in detail with neat diagram.	Understand	CO3	AEC017.13
2	Explain with neat diagrams about 2 µm CMOS Design rules for wires, Contacts and transistors?	Understand	CO3	AEC017.11
3	Explain about various reliability issues in CMOS VLSI using bathtub curve?	Understand	CO3	AEC017.13
4	What is Interconnects and explain the effect of it on circuit?	Remember	CO3	AEC017.12
5	Define various failure mechanisms that occurs in traditional VLSI?	Remember	CO3	AEC017.13
6	Explain design rules for transistors (nMOS, pMOS, CMOS)?	Understand	CO3	AEC017.12
7	Briefly explain about delay that occurs due to interconnects?	Remember	CO3	AEC017.12
8	Explain about cross talk and its effects?	Remember	CO3	AEC017.12
9	Explain the effect of resistance on the interconnect?	Remember	CO3	AEC017.12
10	Sketch a transistor-level schematic for a compound CMOS logic gate for each of the following functions: $Y = (AB + C) \cdot D$ and draw the layout diagram of it.	Understand	CO3	AEC017.12
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)				
1	Draw the nMOS diagram and stick diagram for **$y=(AB + CD)^1$**	Understand	CO3	AEC017.10
2	Draw the circuit schematic and stick diagram of CMOS 2-Input NAND Gate	Understand	CO3	AEC017.10
3	Design a stick diagram for NMOS EX-OR gate along with transistor schematic	Understand	CO3	AEC017.10
4	Draw the schematic diagram and stick diagram of 4:1 Multiplexer?	Understand	CO3	AEC017.10
5	Design a stick diagram for CMOS EX-NOR gate along with transistor schematic	Understand	CO3	AEC017.10
CIE-II				
1	Design a layout diagram for the pMOS logic Y= (AB+AC+BC)'.	Understand	CO3	AEC017.11
2	Design a stick diagram and layout for two input CMOS NOR gate indicating all the width and spacing layers.	Understand	CO3	AEC017.11
3	Draw the stick diagram and mask layout for a CMOS two input NOR gate.	Understand	CO3	AEC017.11
4	Design a layout diagram for the pMOS logic Y= A(B +C.) '	Understand	CO3	AEC017.11
5	Draw the diagram of $y=(A+BC+CD)^1$ using Euler's rule and represent layout diagram?	Understand	CO3	AEC017.11
UNIT-IV				
LOGIC DESIGN AND IMPLEMENTATION STRATEGIES				
PART-A (SHORT ANSWER QUESTIONS)				
1	Draw the standard configuration of any logic circuit in C MOS logic	Remember	CO4	AEC017.16
2	Draw the standard configuration of any logic circuit in	Remember	CO4	AEC017.16

	NMOS logic			
3	What is the basic difference between dynamic and static CMOS logic ?	Understand	CO4	AEC017.16
4	Explain pass transistor using N MOSFET	Remember	CO4	AEC017.16
5	Explain pass transistor using P MOSFET	Remember	CO4	AEC017.16
6	How AND gate can be formed with pass transistors.	Remember	CO4	AEC017.16
7	What is the relative advantage of pseudo n-MOS logic compared to n-MOS logic ?	Understand	CO4	AEC017.16
8	State the formula for n-MOS inverter pair time delay	Remember	CO4	AEC017.15
9	State the formula for p-MOS inverter pair time delay	Remember	CO4	AEC017.15
10	What is firinge field capacitance ?	Understand	CO4	AEC017.15
11	What is interlayer capacitance ?	Understand	CO4	AEC017.15
12	What is peripheral capacitance	Understand	CO4	AEC017.15
13	Differentiate between fan-in and fan-out	Understand	CO4	AEC017.14
14	Which layer is preferred for supply voltages in VLSI	Remember	CO4	AEC017.15
15	Explain PAL with a neat block diagram	Understand	CO4	AEC017.17
16	Explain PLA with a neat block diagram	Understand	CO4	AEC017.17
17	What is dynamic CMOS logic?	Understand	CO4	AEC017.19
18	What are the disadvantages of dynamic logic?	Understand	CO4	AEC017.19
19	What are the causes of dynamic power dissipation?	Understand	CO4	AEC017.19
20	Why single phase dynamic logic structure cannot be cascaded? Justify.	Understand	CO4	AEC017.19
PART-B (LONG ANSWER QUESTIONS)				
1	Design a 2-input multiplexer using CMOS transmission gates.	Understand	CO4	AEC017.16
2	Explain clocked CMOS logic and n-p CMOS logic. Mention their advantages and disad vantages.	Remember	CO4	AEC017.16
3	Draw the dynamic CMOS logic three input nand gate and elaborate it's operation	Understand	CO4	AEC017.16
4	What is CMOS domino logic and give its advantages and disadvantages.	Remember	CO4	AEC017.16
5	Design two input nand gate in pseudo nMOS Logic and derive the expression for Zpu/Zpd for pseudo inverter MOS pair	Understand	CO4	AEC017.16
6	Define time delay unit and derive the expression for nMOS inverter pair time delay	Remember	CO4	AEC017.15
7	Define time delay unit and derive the expression for CMOS inverter pair time delay	Remember	CO4	AEC017.15
8	Derive the conditions for equal rise and fall times for CMOS inverter	Remember	CO4	AEC017.15
9	Discuss in detail different types of capacitances in MOSFETs	Understand	CO4	AEC017.15
10	State and explain different factors influencing choice of layers .	Remember	CO4	AEC017.15
11	Draw and explain the functional block diagram of CPLD with it's applications	Remember	CO4	AEC017.17
12	Describe and differentiate the properties of full custom and semi custom design.	Understand	CO4	AEC017.17
13	Describe and differentiate the properties of full custom and semi custom design	Understand	CO4	AEC017.17
14	Write the design style classification of Semi custom design ASICs	Remember	CO4	AEC017.17
15	Describe and differentiate between channeled gate array and channel less gate array	Remember	CO4	AEC017.17
16	Describe the features of FPGA with functional block	Understand	CO4	AEC017.17

	diagram			
17	Explain boolean function realization using PLA with an example	Understand	CO4	AEC017.17
18	Illustrate any boolean function realization using PALwith an example	Understand	CO4	AEC017.17
19	Design three input nand gate in pseudo nMOS Logic and derive the expression for Zpu/Zpd for pseudo inverter MOS pair	Understand	CO4	AEC017.16
20	Design a 3-input multiplexer using CMOS transmission gates.	Understand	CO4	AEC017.16
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)				
1	Realize the function f=(AB+CD)' using nMOS and CMOS logic.	Remember	CO4	AEC017.16
2	Realize the function f =A+BC using pseudo –nMOS logic.	Remember	CO4	AEC017.16
3	Derive the expression for rise and fall time of CMOS inverter. Comment on the expression derived.	Understand	CO4	AEC017.16
4	Draw and explain the circuit for function f=A+B+C+D using domino logic.	Remember	CO4	AEC017.16
5	Draw and explain the circuit for function f=(A+B)' using clocked C MOS logic	Remember	CO4	AEC017.16
6	Design 4:1MUX using transmission gate.	Understand	CO4	AEC017.16
7	Calculate the gate capacitance value of 5mm technology minimum size transistor with gate to channel capacitance value is 0.0004 pF/um^2.	Understand	CO4	AEC017.16
8	Two NMOS inverters are cascaded to drive a capacitive load $C_L=14C_g$ as shown in figure. Calculate the pair delay V_{in} to V_{out} interms of τ for the data given. Inverter A:$L_{p.u}=12\lambda$ $W_{p.u}=4\lambda$ $L_{p.d}=1\lambda$ $W_{p.d}=1\lambda$ Inverter B: $L_{p.u}=4\lambda$ $W_{p.u}=4\lambda$ $L_{p.d}=2\lambda$ $W_{p.d}=8\lambda$ 	Understand	CO4	AEC017.16
9	Implement the the following functions using PLA F1=AB'C'+AB'C+ABC; F2=A'BC+AB'C+ABC	Understand	CO4	AEC017.17
10	Implement JK flip flop using PLA	Understand	CO4	AEC017.17
UNIT-V				
SUB SYSTEM DESIGN				
PART-A (SHORT ANSWER QUESTIONS)				
1	What are digital functions categories?	Remember	CO 5	AEC017.19
2	What are datapath operators?	Remember	CO 5	AEC017.19
3	What are memory elements?	Remember	CO 5	AEC017.19
4	What are control structures?	Remember	CO 5	AEC017.19
5	What are single-bit adders?	Remember	CO 5	AEC017.20
6	What is carry lookahead adder?	Remember	CO 5	AEC017.20
7	What are Special-purpose cells?	Remember	CO 5	AEC017.20
8	What is Manchester carry chain?	Remember	CO 5	AEC017.20
9	What is wallace tree multiplication?	Understand	CO 5	AEC017.20
10	What is Parity generator?	Remember	CO 5	AEC017.21
11	What is three transistor dynamic RAM?	Remember	CO 5	AEC017.21
12	What are the classifications of binary counters?	Remember	CO 5	AEC017.21
13	Draw the 4-bit ripple carry adder.	Understand	CO 5	AEC017.22

14	Write about single-bit adders.	Remember	CO 5	AEC017.22
15	Write short notes on ALUs	Understand	CO 5	AEC017.22
PART-B (LONG ANSWER QUESTIONS)				
1	Design a 4-bit asynchronous Up-Counter with T Flip-Flops.	Understand	CO 5	AEC017.19
2	Design a 4-bit asynchronous Down-Counter with T Flip-Flops.	Remember	CO 5	AEC017.19
3	Design a 4-bit synchronous Up-Counter with T Flip-Flops.	Understand	CO 5	AEC017.19
4	Design a 4-bit synchronous Down-Counter with T Flip-Flops.	Remember	CO 5	AEC017.20
5	Discuss about master-slave edge-triggered register.	Understand	CO 5	AEC017.20
6	Discuss about dynamic transmission-gate edge-triggered registers.	Remember	CO 5	AEC017.20
7	Design a 1-bit digital comparator.	Understand	CO 5	AEC017.21
8	Discuss about Zero/One detector.	Understand	CO 5	AEC017.21
9	Describe in detail about parity generators.	Remember	CO 5	AEC017.22
10	Draw the schematic for tiny XOR gate and explain its operation.	Remember	CO 5	AEC017.22
11	How the read operation occurs in DRAM cell?	Understand	CO 5	AEC017.21
12	Draw the diagram of Pseudo –nMOS ROM and explain function of it?	Understand	CO 5	AEC017.21
13	Draw the diagram of shift registers and how it will do operation on data?	Understand	CO 5	AEC017.21
14	Explain various queue operations with diagram?	Understand	CO 5	AEC017.21
15	How the multiplication occurs using booth encoding?	Understand	CO 5	AEC017.21
16	Explain the operation of programmable ROM?	Understand	CO 5	AEC017.21
17	Explain the operation of NAND ROM?	Understand	CO 5	AEC017.21
18	Write short notes on the following Full adder and draw the MOS diagram of it?	Remember	CO 5	AEC017.22
19	Explain the design principles of pipelining.	Understand	CO 5	AEC017.21
20	Write notes on the Ripple-carry adder.	Remember	CO 5	AEC017.22
PART-C (PROBLEM SOLVING AND CRITICAL THINKING QUESTIONS)				
1	Explain the path-delay measurement of combinational logic circuits.	Understand	CO 5	AEC017.19
2	With example, explain what do you mean by transistor sizing?	Understand	CO 5	AEC017.19
3	Explain about power distribution and clock distribution of routing procedure.	Remember	CO 5	AEC017.20
4	Compare dynamic and re-circulating latches.	Understand	CO 5	AEC017.20
5	Explain any one routing algorithm with suitable example.	Understand	CO 5	AEC017.21
6	Draw and explain the structure of a carry look ahead adder.	Understand	CO 5	AEC017.21
7	Why is static 6-transistor cell used for average CMOS system design?	Understand	CO 5	AEC017.21
8	Write notes on the Manchester carry chain	Remember	CO 5	AEC017.22
9	Design a schematic for an 8-word * 2-bit NAND ROM that serves a lookup table to Implement a full adder	Understand	CO 5	AEC017.22
10	Draw the structure of a serial-parallel multiplier and explain it.	Understand	CO 5	AEC017.22

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