# INSTITUTE OF AERONAUTICAL ENGINEERING

**(Autonomous)**

Dundigal, Hyderabad -500 043

## ELECTRICAL AND ELECTRONICS ENGINEERING

## COURSE DESCRIPTOR

| | | | | | |
|---|---|---|---|---|---|
| **Course Title** | **MICROCONTROLLER AND DIGITAL SIGNAL PROCESSING** | | | | |
| **Course Code** | AEC022 | | | | |
| **Programme** | B.Tech | | | | |
| **Semester** | VI | EEE | | | |
| **Course Type** | Foundation | | | | |
| **Regulation** | IARE - R16 | | | | |
| **Course Structure** | **Theory** | | | **Practical** | |
| | **Lectures** | **Tutorials** | **Credits** | **Laboratory** | **Credits** |
| | 3 | 1 | 4 | 3 | 2 |
| **Chief Coordinator** | Ms. J. Sravana, Assistant Professor | | | | |
| **Course Faculty** | Ms. J. Sravana, Assistant Professor | | | | |

## I. COURSE OVERVIEW:

Microcontrollers and digital signal processing course is intended to introduce the architecture, programming of microprocessors, microcontrollers and interfacing various hardware circuits to microprocessors and microcontrollers. The topics covered are architecture, addressing modes, instruction set of 8086 and 8051**.** Understand need of microprocessors, microcontrollers in development of various projects and to know complete architectural, programming, interfacing details of 8086 microprocessor-8051 microcontroller.

## II. COURSE PRE-REQUISITES:

| Level | Course Code | Semester | Prerequisites |
|---|---|---|---|
| UG | AEC019 | IV | Digital and pulse circuits |

## III. MARKS DISTRIBUTION:

| Subject | SEE Examination | CIA Examination | Total Marks |
|---|---|---|---|
| Microcontroller and digital signal processing | 70 Marks | 30 Marks | 100 |

## IV. DELIVERY / INSTRUCTIONAL METHODOLOGIES:

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ✘ | Chalk & Talk | ✔ | Quiz | ✔ | Assignments | ✘ | MOOCs |
| ✔ | LCD / PPT | ✔ | Seminars | ✘ | Mini Project | ✔ | Videos |
| ✘ | Open Ended Experiments | | | | | | |

## V. EVALUATION METHODOLOGY:

The course will be evaluated for a total of 100 marks, with 30 marks for Continuous Internal Assessment (CIA) and 70 marks for Semester End Examination (SEE). Out of 30 marks allotted for CIA during the semester, marks are awarded by taking average of two CIA examinations or the marks scored in the make-up examination.

**Semester End Examination (SEE):** The SEE is conducted for 70 marks of 3 hours duration. The syllabus for the theory courses is divided into FIVE units and each unit carries equal weightage in terms of marks distribution. The question paper pattern is as follows. Two full questions with "either" or "choice" will be drawn from each module. Each question carries 14 marks. There could be a maximum of two sub divisions in a question.

The emphasis on the questions is broadly based on the following criteria:

| | |
|---|---|
| 50 % | To test the objectiveness of the concept. |
| 50 % | To test the analytical skill of the concept OR to test the application skill of the concept. |

**Continuous Internal Assessment (CIA):**

CIA is conducted for a total of 30 marks (Table 1), with 20 marks for Continuous Internal Examination (CIE), 05 marks for Quiz and 05 marks for Alternative Assessment Tool (AAT).

Table 1: Assessment pattern for CIA

| Component | Theory | | | Total Marks |
|---|---|---|---|---|
| **Type of Assessment** | CIE Exam | Quiz | AAT | |
| **CIA Marks** | 20 | 05 | 05 | 30 |

**Continuous Internal Examination (CIE):**

Two CIE exams shall be conducted at the end of the 8th and 16th week of the semester respectively. The CIE exam is conducted for 20 marks of 2 hours duration consisting of five descriptive type questions out of which four questions have to be answered where, each question carries 5 marks. Marks are awarded by taking average of marks scored in two CIE exams.

**Quiz - Online Examination**

Two Quiz exams shall be online examination consisting of 25 multiple choice questions and are to be answered by choosing the correct answer from a given set of choices (commonly four). Such a question paper shall be useful in testing of knowledge, skills, application, analysis, evaluation and understanding of the students. Marks shall be awarded considering the average of two quiz examinations for every course.

**Alternative Assessment Tool (AAT)**

This AAT enables faculty to design own assessment patterns during the CIA. The AAT converts the classroom into an effective learning centre. The AAT may include tutorial hours/classes, seminars, assignments, term paper, open ended experiments, METE (Modeling and Experimental Tools in Engineering), five minutes video, MOOCs etc.

## VI. HOW PROGRAM OUTCOMES ARE ASSESSED:

| Program Outcomes (POs) | | Strength | Proficiency assessed by |
|---|---|---|---|
| PO 1 | **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems. | 2 | Lectures, Assignments |
| PO 2 | **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences. | 2 | Assignments. |
| PO 5 | **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations. | 2 | Lab related Exercises |
| PO 12 | **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change. | 2 | Seminars |

**3 = High; 2 = Medium; 1 = Low**

## VII. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

| Program Specific Outcomes (PSOs) | | Strength | Proficiency assessed by |
|---|---|---|---|
| PSO 1 | **Problem Solving**: Exploit the knowledge of high voltage engineering in collaboration with power systems in innovative, dynamic and challenging environment, for the research based team work. | 1 | Seminar |
| PSO 2 | **Professional Skills:** Identify the scientific theories, ideas, methodologies and the new cutting edge technologies in renewable energy engineering, and use this erudition in their professional development and gain sufficient competence to solve the current and future energy problems universally. | - | - |
| PSO 3 | **Modern Tools in Electrical Engineering:** Comprehend the technologies like PLC, PMC, process controllers, transducers and HMI and design, install, test, maintain power systems and industrial applications. | - | - |

**3 = High; 2 = Medium; 1 = Low**

## VIII. COURSE OBJECTIVES :

| **The course should enable the students to:** | |
|---|---|
| I | Enrich the knowledge of evolution of processor. |
| II | Apply the concept of assembly language programs for different applications. |
| III | Analyze and apply the concepts of discrete signals using discrete fourier transform. |
| IV | Analyze and design IIR and FIR digital filters. |

## IX. COURSE OUTCOMES (COs):

| COs | Course Outcome | CLOs | Course Learning Outcome |
|---|---|---|---|
| CO 1 | Apply a basic concept of digital fundamentals to Microprocessor based personal computer system | CLO 1 | Understand and Describe the evolution and basic architecture of 8086 |
| | | CLO 2 | Discuss the segmentation and programming model and List out the register organization |
| | | CLO 3 | Understand the difference between microprocessors and microcontrollers |
| CO 2 | Describe the architecture and instruction set of 8051 microcontroller | CLO 4 | Understand and describe input/output ports of 8051 and register organization |

| COs | Course Outcome | CLOs | Course Learning Outcome |
|---|---|---|---|
| | | CLO 5 | Describe different types of memory like special function register for program memory and data memory |
| | | CLO 6 | Discuss the addressing modes of 8051 microcontroller |
| | | CLO 7 | Discuss the instruction set of 8051 microcontroller |
| | | CLO 8 | Develop assembly language program for 8051 based operations. |
| CO 3 | Describe the architecture and instruction set of 8051 microcontroller Design and implement 8051 microcontroller based systems. | CLO 9 | Discuss and illustrate the Timers/counters, serial communication |
| | | CLO 10 | Understand and discuss external memory |
| | | CLO 11 | Understand and discuss clock circuits and i/o memory |
| | | CLO 12 | Develop assembly code for real time control. |
| | | CLO 13 | Develop assembly code for real time control to interfacing ADC and DAC |
| CO 4 | Analyze the fundamentals and concepts in assess the effect of LTI systems on signals passing through them in frequency and time domains | CLO 14 | Understand the frequency domain representation and discrete Fourier transforms |
| CO 5 | Discriminate the Fourier, Laplace and Z-transforms as appropriate for various signals and systems | CLO 15 | Understand the FFT and FFT algorithms, inverse FFT and FFT with general radix- N. |
| | | CLO 16 | Analyze and design of FIR digital filters |
| | | CLO 17 | Analyze and design of IIR filters and digital filters using window techniques |

## X. COURSE LEARNING OUTCOMES (CLOs):

| CLO Code | CLO's | At the end of the course, the student will have the ability to: | PO's Mapped | Strength of Mapping |
|---|---|---|---|---|
| AEC022.01 | CLO 1 | Understand and Describe the evolution and basic architecture of 8086 | PO 1<br>PO 2 | 2 |
| AEC022.02 | CLO 2 | Discuss the segmentation and programming model and List out the register organization | PO 1<br>PO 2 | 2 |
| AEC022.03 | CLO 3 | Understand the difference between microprocessors and microcontrollers | PO 1 | 3 |
| AEC022.04 | CLO 4 | Understand and describe input/output ports of 8051 and register organization | PO 1 | 2 |
| AEC022.05 | CLO 5 | Describe different types of memory like special function register for program memory and data memory | PO 2 | 2 |
| AEC022.06 | CLO 6 | Discuss the addressing modes of 8051 microcontroller | PO 1 | 3 |
| AEC022.07 | CLO 7 | Discuss the instruction set of 8051 microcontroller | PO 1 | 3 |
| AEC022.08 | CLO 8 | Develop assembly language program for 8051 based operations. | PO 1 | 2 |
| AEC022.09 | CLO 9 | Discuss and illustrate the Timers/counters, serial communication | PO 1 | 2 |
| AEC022.10 | CLO 10 | Understand and discuss external memory | PO 1<br>PO 12 | 3 |

| CLO Code | CLO's | At the end of the course, the student will have the ability to: | PO's Mapped | Strength of Mapping |
|---|---|---|---|---|
| AEC022.11 | CLO 11 | Understand and discuss clock circuits and i/o memory | PO 1 | 1 |
| AEC022.12 | CLO 12 | Develop assembly code for real time control. | PO 5<br>PO 12 | 1 |
| AEC022.13 | CLO 13 | Develop assembly code for real time control to interfacing ADC and DAC | PO 1<br>PO 2 | 2 |
| AEC022.14 | CLO 14 | Understand the frequency domain representation and discrete Fourier transforms | PO 1<br>PO 12 | 3 |
| AEC022.15 | CLO 15 | Understand the FFT and FFT algorithms, inverse FFT and FFT with general radix- N. | PO 5 | 3 |
| AEC022.16 | CLO 16 | Analyze and design of FIR digital filters | PO 2<br>PO 12 | 2 |
| AEC022.17 | CLO 17 | Analyze and design of IIR filters and digital filters using window techniques | PO 2 | 2 |

**3= High; 2 = Medium; 1 = Low**

## XI. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES

| Course Outcomes (COs) | Program Outcomes (POs) | | | |
|---|---|---|---|---|
| | PO 1 | PO 2 | PO 4 | PSO1 |
| CO 1 | 2 | 2 | | |
| CO 2 | | | 1 | |
| CO 3 | 3 | 2 | | 1 |
| CO 4 | 2 | | | 1 |
| CO 5 | 3 | 2 | **1** | **1** |

## XII. APPING COURSE LEARNING OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

| Course Learning Outcomes (CLOs) | Program Outcomes (POs) | | | | | | | | | | | | Program Specific Outcomes (PSOs) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 | PSO3 |
| CLO 1 | 3 | 2 | | | | | | | | | | | 1 | | |
| CLO 2 | 2 | 3 | | | | | | | | | | | 1 | | |
| CLO 3 | 3 | | | | | | | | | | | | 1 | | |
| CLO 4 | | | | | | | | | | | | | | | |
| CLO 5 | | 2 | | | | | | | | | | | | | |
| CLO 6 | | | | | | | | | | | | | 1 | | |
| CLO 7 | 3 | | | | | | | | | | | 2 | 1 | | |
| CLO 8 | 2 | | | | | | | | | | | | | | |
| CLO 9 | 2 | | | | | | | | | | | 2 | | | |
| CLO 10 | 3 | | | | | | | | | | | | | | |

| Course Learning Outcomes (CLOs) | Program Outcomes (POs) | | | | | | | | | | | | Program Specific Outcomes (PSOs) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 | PSO3 |
| CLO 11 | 1 | | | | | | | | | | | 2 | 1 | | |
| CLO 12 | | | | | 1 | | | | | | | | | | |
| CLO 13 | 2 | 2 | | | | | | | | | | 2 | | | |
| CLO 14 | 3 | | | | | | | | | | | | | | |
| CLO 15 | 3 | | | | 1 | | | | | | | | | | |
| CLO 16 | | 2 | | | | | | | | | | | | | |
| CLO 17 | | 2 | | | | | | | | | | | | | |

**3 = High; 2 = Medium; 1 = Low**

## XIII. SSESSMENT METHODOLOGIES – DIRECT

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| CIE Exams | PO1, PO2, PO4,PO12 | SEE Exams | PO1, PO2, PO4,PSO1 | Assignments | PO 1, PO 2 | Seminars | PO12 |
| Laboratory Practices | PO 5 | Student Viva | - | Mini Project | - | Certification | - |
| Term Paper | | | | | | | |

## XIV. ASSESSMENT METHODOLOGIES - INDIRECT

| | | | |
|---|---|---|---|
| ✔ | Early Semester Feedback | ✔ | End Semester OBE Feedback |
| ✘ | Assessment of Mini Projects by Experts | | |

## XV. SYLLABUS

| | |
|---|---|
| **Unit-I** | **MICROPROCESSORS AND MICROCONTROLLER** |
| Evaluation of processors, 8086 architecture, functional diagram, register organization, memory segmentation, microcontrollers, comparison of microprocessors and microcontrollers, microcontroller survey, 8051 architecture, pin diagram of 8051, I/O ports, memory organization, counters and timers, serial data input / output, interrupts | |
| **Unit-II** | **INSTRUCTION SET AND PROGRAMMING OF 8051** |
| Addressing modes, Instruction set of 8051, programming of 8051, timers and counters, serial communication. | |
| **Unit-III** | **8051 MICRO CONTROLLER DESIGN** |
| Microcontroller design: External memory and memory space decoding, clock circuits, memory mapped I/O.<br><br>Keyboard Interface, Seven segment numeric display interface, D/A and A/D converter interface to 8051. | |
| **Unit-IV** | **INTRODUCTION TO DIGITAL SIGNAL PROCESSING AND FAST FOURIER TRANSFORMS** |
| Discrete time signals and sequences, linear shift invariant systems, stability and causality, frequency domain representation of discrete time signals and systems, review of discrete Fourier transforms, Fast Fourier transforms, radix2 decimation in time and decimation in frequency, FFT algorithms, inverse FFT | |

| | |
|---|---|
| and FFT with general radix- N. | |
| **Unit-V** | **IIR AND FIR DIGITAL FILTERS** |
| Analog filter approximations, Butterworth and Chebyshev, design of IIR digital filters from analog filters, step and impulse invariant techniques, characteristics of FIR digital filters, frequency response; Design of FIR digital filters: Fourier method, digital filters using window techniques. | |
| **Text Books:** | |
| 1. A K ray and K M Bhurchandani, "Advanced microprocessors and peripherals", Tata McGraw-Hill, 2nd Edition 2006.<br>2. John G Proakis, Dimitris G Manolakis, "Digital signal processing, principles, Algorithms and applications", Pearson Education / PHI, 4th Edition. 2007. | |
| **Reference Books:** | |
| 1. Ajay V Deshmukh, "Microcontrollers and application", TMGH, 1st Edition, 2005.<br>2. Kenneth J Ayala, " The 8051 microcontroller", Cengage learning, 3rd Edition 2010.<br>3. Li tan Elsevier, "Digital signal processing: fundamentals and applications", 1st Edition, 2008. | |

## XVI. COURSE PLAN:

The course plan is meant as a guideline. Probably there may be changes.

| Lecture No | Topics to be covered | Course Learning Outcomes (CLOs) | Reference |
|---|---|---|---|
| 1-6 | Introduction of MDSP, Architecture of 8086, Functional diagram | CLO 1 | T1-2.1<br>R1-2.3 |
| 7-9 | Register organization of 8086, flag register structure, Memory segmentation, memory address and physical memory | CLO 2 | T1-20.1 |
| 10-12 | Differences between microprocessors and microcontrollers, Architecture of 8051 microcontroller, Pin diagram of 8051 | CLO 2 | T1-8.1<br>R2-2.1 |
| 13-16 | Register organization, I/O ports in 8051 and operation of each port | CLO 3 | T1–8.1<br>R2-2.7 |
| 17-20 | Memory organization of 8051, timers and counters | CLO 4 | T1-10.1 |
| 21-24 | Addressing modes in 8051 with examples | CLO 5 | T1-10.11<br>R2-3.1 |
| 25-32 | Instruction set of 8051with different addressing modes | CLO 6 | T1-11.1<br>R2-3.8 |
| 33-35 | Simple programs related to 8051 | CLO 6 | T1-11.12<br>R2-4.1.1 |
| 36-37 | 8051 Real time control, Interrupts used in 8051 | CLO 7 | T1-17.1 |
| 38-39 | Microcontroller design: External memory and memory space decoding | CLO 8 | T1-14.1<br>R2-21.1 |
| 40-41 | Clock circuits, memory mapped I/O | CLO 8<br>CLO 9 | T1-14.9<br>R2-17.1 |
| 42 | Keyboard Interface, Seven segment numeric display interface | CLO 10 | T1-19.1<br>R2-3.1 |
| 43-44 | D/A and A/D converter interface to 8051 | CLO 11 | T1-19.4<br>R2-41.1 |
| 45-46 | Discrete time signals and sequences, linear shift invariant systems, stability and causality | CLO 12 | T1-19.6<br>R2-23.1 |
| 47-48 | Frequency domain representation of discrete time signals and systems. | CLO 13 | R2-9.3 |
| 49 | Review of discrete Fourier transforms | CLO 14 | R2-9.1 |
| 50 | Fast Fourier transforms, radix2 decimation in time | CLO 15 | R2-9.7 |

| | | | |
|---|---|---|---|
| 51-53 | Decimation in frequency, FFT algorithms, inverse FFT and FFT with general radix-N | CLO 15 | T2-27.7 |
| 54 | Analog filter approximations Chebyshev | CLO 15 | T2-27.8 |
| 55-56 | Analog filter approximations, Butterworth, design of IIR digital filters from analog filters. | CLO 17 | T2-27.12 |
| 57 | Step and impulse invariant techniques, characteristics of FIR digital filters. | CLO 17 | T2-27.12<br>R1-11.8 |
| 58 | Frequency response, design of FIR digital filters | CLO 17 | R1-11.8 |
| 59-60 | Fourier method, digital filters using window techniques | CLO 17 | R1-11.9 |
| 54 | Analog filter approximations Chebyshev | CLO 15 | T2-27.8 |

## XVII. GAPS IN THE SYLLABUS-TO MEET INDUSTRY / PROFESSION REQUIREMENTS:

| S no | Description | Proposed actions | Relevance with pos | Relevance with psos |
|---|---|---|---|---|
| 1 | To introduce concepts of evolution o processor. | Guest Lectures | PO 1 | PSO 1 |
| 2 | Analyze and understand the assembl language apply to real time applications. | Seminars /NPTEL | PO 2 | PSO 1 |
| 3 | Encourage students to solve real tim applications and prepare toward competitive examinations. | NPTEL | PO 2 | PSO 1 |

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**HOD, EEE**