Hall Ticket No | | | | | | | | | | |  Question Paper Code: AECB05

# INSTITUTE OF AERONAUTICAL ENGINEERING

**(Autonomous)**

**Dundigal, Hyderabad - 500 043**

## MODEL QUESTION PAPER-II

**B.Tech III Semester End Examinations (Regular), November -2019**

**Regulations: IARE-R18**

**ANALOG AND DIGITAL ELECTRONICS**

(IT)

**Time: 3 hours** **Max. Marks: 70**

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the question must be answered in one place only

### MODULE – I

1. a) Explain the formation of depletion region in an open-circuited p-n junction diode and also the effect of forward and reverse biasing of p-n junction on the depletion region with neat sketches? **[7M]**

   b) A P-N junction germanium diode has a reverse saturation current of 0.10 µA at the room temperature of 270C.It is observed to be 30µA, when the room temperature is increased. Evaluate the room temperature? **[7M]**

2. a) Draw the circuit diagrams of a full wave rectifier and Bridge rectifier. Explain the operation of the circuit with relevant waveforms. **[7M]**

   b) A full wave bridge rectifier having load resistance of 100Ω is fed with 220V, Assuming the diodes are ideal, Find the following terms, **[7M]**

      i) DC output voltage
      ii) Peak inverse voltage
      iii) Rectifier efficiency.

### MODULE – II

3. a) Explain clearly the DC and AC load line and also explain how to obtain quiescent point graphically for a transistor amplifier of CE configuration. **[7M]**

   b) A Common emitter circuit has the following components. Rs=1kΩ, R1=110KΩ, R2=12KΩ Rc=6KΩ. H-parameters are hie=1.2K, hre=2.5*10-4 ,hfe=75,hoe=25uA/V. Draw the equivalent hybrid model and calculate Ai, Ri, Ro and Av? **[7M]**

4. a) Derive the equations of current gain Ai, voltage gain Av , input impedance Zi , output admittance Yo , voltage gain with Rs(Avs), current gain with Rs(Ais) using a general two port active network. **[7M]**

   b) Compute current gain, voltage gain, input and output impedance of the CB amplifier if it is driven by a voltage source of internal resistance Rs=1k.The load impedance is RL=1K. The transistor parameters are hib= 22, hfb= -0.98, hrb=2.9×10−4, hob= 0.5µA/V. **[7M]**

## MODULE – III

5. a) Explain in detail about the gray to binary and binary- to- gray conversion with neat sketches. **[7M]**

   b) Perform the subtraction using 1's complement and 2's Complement **[7M]**

      i) $(11010)_2 - (10000)_2$

      ii) $(1000100)_2 - (1010100)_2$

6. a) Give the Boolean expressions, symbols and truth tables for following gates, **[7M]**
   i) AND ii) NOR iii) EX-OR iv) OR v) EX-NOR.

   b) Obtain the canonical SOP form of the following functions, **[7M]**
   i) Y(A,B) = A+B. ii) Y(A,B,C,D) = AB+ACD

## MODULE – IV

7. a) Design a 64:1 MUX using 8:1 MUXs with suitable neat block diagram. **[7M]**

   b) Simplify the following Boolean expressions using K-map and implement it by using NOR gates. **[7M]**
   a) F(A,B,C,D)=AB'C' +AC+A'CD' b)F(W,X,Y,Z)=w' x'y'z' + wxy'z' + w'x'yz + wxyz

8. a) Implement the given function in 4:1 mux f= Σm(0,1,3,5,6) **[7M]**

   b) F(w,x,y,z) = ∑m (1,4,5,6,7,9,14,15) Realize using De-Multiplexer **[7M]**

## MODULE – V

9. a) Write short notes on shift register? Mention its application along with the Serial Transfer in 4-bit shift Registers? **[7M]**

   b) Describe the steps involved in design of asynchronous sequential circuit in detail with an example? **[7M]**

10. a) Design a 3 bit ring counter? Discuss how ring counters differ from twisted ring counter? **[7M]**

    b) Design and implement 4-bit binary counter (using D flip flops) which counts all possible odd numbers only? **[7M]**

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## COURSE OBJECTIVES:

**The course should enable the students to:**

| | |
|---|---|
| I | Introduce components such as diodes, BJTs and FETs. |
| II | Know the applications of components. |
| III | Understand common forms of number representation in logic circuits |
| IV | Learn basic techniques for the design of digital circuits and fundamental concepts used in the design of digital systems. |
| V | Understand the concepts of combinational logic circuits and sequential circuits. |

## COURSE OUTCOMES (COs):

| | |
|---|---|
| CO 1 | Acquire knowledge of electrical characteristics of ideal and practical diodes under forward and reverse bias to analyze and design diode application circuits such as rectifiers. |
| CO 2 | Utilize operational principles of bipolar to derive appropriate small-signal models and use them for the analysis of basic circuits. |
| CO 3 | Understand the basic concept of number systems, Boolean algebra principles and minimization techniques for Boolean algebra |
| CO 4 | Analyze Combination logic circuit such as multiplexers, adders, decoders. |
| CO 5 | Understand about synchronous and asynchronous sequential logic circuits. |

## COURSE LEARNING OUTCOMES (CLOs):

| | |
|---|---|
| AECB05.01 | Understand and analyze diodes operation and their characteristics in order to design basic form circuits |
| AECB05.02 | Explain half wave rectifier for the given specifications. |
| AECB05.03 | Design full wave rectifier for the given specifications |
| AECB05.04 | Design rectifier with capacitive filter for the given specifications |
| AECB05.05 | Understand the different parameters of transistors such as depletion width and channel width for understanding the functioning and design of this component. |
| AECB05.06 | Estimate the performance of BJT on the basis of their operation and working. |
| AECB05.07 | Explain the operation of Operating Point and Load Line Analysis |
| AECB05.08 | Explain the operation of CB,CE,CC I/O Characteristics |
| AECB05.09 | Understand the importance of h-parameter model |
| AECB05.10 | Understand the basic concept of number systems, Binary addition and subtraction for digital systems. |
| AECB05.11 | Explain the complements of Binary & Decimal number systems |

| | |
|---|---|
| AECB05.12 | Discuss about digital logic gates, error detecting and Correcting codes for digital systems. |
| AECB05.13 | Illustrate the switching algebra theorems and apply them for reduction of Boolean function. |
| AECB05.14 | Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits. |
| AECB05.15 | Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method. |
| AECB05.16 | Design Gate level minimization using KMaps and realize the Boolean function using logic gates. |
| AECB05.17 | Analyze the design procedures of Combinational logic circuits like adders,Subtractors. |
| AECB05.18 | Analyze the design of decoder, demultiplexer, and comparator using combinational logic circuit. |
| AECB05.19 | Understand bi-stable elements like latches flip-flop and Illustrate the excitation tables of different flip flops |
| AECB05.20 | Understand the concept of Shift Registers and implement the bidirectional and universal shift registers. |
| AECB05.21 | Implement the synchronous& asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops. |

## MAPPING OF SEMESTER END EXAMINATION - COURSE OUTCOMES:

| SEE Question No | | Course Learning Outcomes | | Course Outcomes | Blooms Taxonomy Level |
|---|---|---|---|---|---|
| 1 | a | AECB05.01 | Understand and analyze diodes operation and their characteristics in order to design basic form circuits | CO 1 | Understand |
| | b | AECB05.01 | Understand and analyze diodes operation and their characteristics in order to design basic form circuits | CO 1 | Understand |
| 2 | a | AECB05.03 | Design full wave rectifier for the given specifications | CO 1 | Understand |
| | b | AECB05.03 | Design full wave rectifier for the given specifications | CO 1 | Understand |
| 3 | a | AECB05.07 | Explain the operation of Operating Point and Load Line Analysis | CO 2 | Understand |
| | b | AECB05.09 | Understand the importance of h-parameter model | CO 2 | Remember |
| 4 | a | AECB05.09 | Understand the importance of h-parameter model | CO 2 | Understand |
| | b | AECB05.09 | Understand the importance of h-parameter model | CO 2 | Understand |
| 5 | a | AECB05.11 | Explain the complements of Binary & Decimal number systems | CO 3 | Understand |
| | b | AECB05.11 | Explain the complements of Binary & Decimal number systems | CO 3 | Understand |
| 6 | a | AECB05.12 | Discuss about digital logic gates, error detecting and Correcting codes for digital systems. | CO 3 | Understand |
| | b | AECB05.14 | Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits. | CO 3 | Understand |
| 7 | a | AECB05.18 | Analyze the design of decoder, demultiplexer, and comparator using combinational logic circuit. | CO 4 | Understand |
| | b | AECB05.16 | Design Gate level minimization using K-Maps and realize the Boolean function using logic gates. | CO 4 | Understand |
| 8 | a | AECB05.18 | Analyze the design of decoder, demultiplexer, and comparator using combinational logic circuit. | CO 4 | Understand |
| | b | AECB05.18 | Analyze the design of decoder, demultiplexer, and comparator using combinational logic circuit. | CO 4 | Understand |
| 9 | a | AECB05.20 | Understand the concept of Shift Registers and implement the bidirectional and universal shift registers. | CO 5 | Understand |

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|---|---|---|---|---|---|
| | b | AECB05.21 | Implement the synchronous& asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops. | CO 5 | Understand |
| 10 | a | AECB05.21 | Implement the synchronous& asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops. | CO 5 | Understand |
| | b | AECB05.21 | Implement the synchronous& asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops. | CO 5 | Understand |

**Signature of Course Coordinator** **HOD, IT**