INSTITUTE OF AERONAUTICAL ENGINEERING

(Autonomous)
Dundigal, Hyderabad - 500 043

| MODEL QUESTION PAPER - II |

B.Tech III Semester End Examinations, November - 2019
Regulation: IARE-R18
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours   **Max Marks: 70**

Answer any ONE question from each
MODULE
All questions carry equal marks
All parts of the question must be answered in one place only

MODULE – I

1   a)   Convert the octal numbers into binary numbers (47.5)8, (32.3)8.   [7M]
    b)   a) Convert 4510 to binary number   [7M]
         b) Convert 0.62510 to binary number?

2   a)   Explain Self complemented codes.   [7M]
    b)   Convert the following Hexadecimal number to their Decimal equivalent (EAF2)16.   [7M]

MODULE – II

3   a)   Design Full adder using Logic Gates.   [7M]
    b)   Convert (A+B) (A+B+C)(B+C) Expression into canonical POS.   [7M]

4   a)   A function having three data inputs to implement the logic for the function F = Σm (0, 1, 2, 3, 4, 7).   [7M]
    b)   Simplify the Boolean function F = Σm (0, 1, 2, 3, 4, 7, 9, 10, 14, 15) using tabular method.   [7M]

MODULE – III

5   a)   Differentiate the advantages and disadvantages of ripple counters?   [7M]
    b)   Describe about T – Flip-flop with the help of a logic diagram and characteristic table.   [7M]
         Derive a T-flip-flop from JK and D flip-flops.

6   a)   Define JK – Flip-flop with the help of a logic diagram and characteristic table?   [7M]
    b)   Explain with the help of a block diagram, the basic components of a Sequential Circuit?   [7M]

MODULE – IV

7	a)	Explain latch up and the circumstances under which it occurs.	[7M]
	b)	Explain about emitter coupled logic.	[7M]
8	a)	Write about CMOS circuits steady state electrical behavior.	[7M]
	b)	Realize the CMOS NAND gate in transistor level using NOR gate circuit.	[7M]

MODULE – V

9	a)	Explain the program structure of VHDL?	[7M]
	b)	Write about primary differences between the various programming styles of VHDL language.	[7M]
10	a)	Write about primary differences between the various programming styles of VHDL language.	[7M]
	b)	Write a VHDL code for a full subtractor using logic equation.	[7M]

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COURSE OBJECTIVES

I	Understand common forms of number representation in logic circuits.
II	Learn basic techniques for the design of digital circuits and fundamental concepts used in the design of digital systems.
III	Understand the concepts of combinational logic circuits and sequential circuits.
IV	Understand the Realization of Logic Gates Using Diodes & Transistors.

COURSE OUTCOMES (COs):

CO 1	Understand the logic simplification and combinational logic design.
CO 2	Explore the MSI devices like Comparators, Multiplexers, Encoder, Decoder, Driver & Multiplexed Display, Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder, Barrel shifter and ALU
CO 3	Understand the building blocks like FF, Ripple and Synchronous counters, Shift registers, Finite state machines, Design of synchronous FSM, Algorithmic State Machines charts
CO 4	Understand the Logic Families And Semiconductor Memories
CO 5	Explore the VHDL Design entry and Modeling, Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits

COURSE LEARNING OUTCOMES

AECB07.01	Understand number systems, binary addition and subtraction, 2's complement Representation and operations with this representation and understand the different binary codes.
AECB07.02	Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.
AECB07.03	Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method.
AECB07.04	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder
AECB07.05	Understand Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder.
AECB07.06	Analyze Barrel shifter and ALU
AECB07.07	Understand bi-stable elements like latches, flip-flop and illustrate the excitation tables of different flip flops.
AECB07.08	Analyze and apply the design procedures of small sequential circuits to build the gated latches.
AECB07.09	Understand the concept of Shift Registers and implement the bidirectional and universal shift registers.
AECB07.10	Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
AECB07.11	Implement the Asynchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.
AECB07.12	Analyze TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out.
AECB07.13	Implement Tristate TTL, ECL, CMOS families and their interfacing, Memory elements,
AECB07.14	Understand Concept of Programmable logic devices like FPGA. Logic implementation using Programmable Devices.
AECB07.15	Design entry: Schematic, FSM & HDL, different modeling styles in VHDL,
AECB07.16	Understand Data types and objects, Dataflow, Behavioral and Structural Modeling,

AECB07.17	Analyze Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits.

MAPPING OF SEMESTER END EXAMINATION TO COURSE LEARNING OUTCOMES:

SEE Question No.			Course Learning Outcomes	Blooms Taxonomy Level
1	a	AECB07.02	Identify the importance of SOP and POS canonical forms in the minimization or other optimization of Boolean formulas in general and digital circuits.	Understand
	b	AECB07.01	Understand number systems, binary addition and subtraction, 2's complement Representation and operations with this representation and understand the different binary codes.	Remember
2	a	AECB07.01	Understand number systems, binary addition and subtraction, 2's complement Representation and operations with this representation and understand the different binary codes.	Understand
	b	AECB07.03	Evaluate functions using various types of minimizing algorithms like Karnaugh map or tabulation method.	Remember
3	a	AECB07.04	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder	Remember
	b	AECB07.05	Understand Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder.	Apply
4	a	AECB07.04	Analyze the design procedures of Combinational logic circuits like adder, binary adder, carry look ahead adder.	Remember
	b	AECB07.06	Analyze Barrel shifter and ALU.	Apply
5	a	AECB07.07	Understand bi-stable elements like latches, flip-flop and illustrate the excitation tables of different flip flops.	Remember
	b	AECB07.08	Analyze and apply the design procedures of small sequential circuits to build the gated latches.	Apply
6	a	AECB07.09	Understand the concept of Shift Registers and implement the bidirectional and universal shift registers.	Understand
	b	AECB07.10	Implement the synchronous counters using design procedure of sequential circuit and excitation tables of flip – flops.	Apply
7	a	AECB07.12	Analyze TTL NAND gate, Specifications, Noise margin, Propagation delay, fan-in, fan-out.	Understand
	b	AECB07.13	Implement Tristate TTL, ECL, CMOS families and their interfacing, Memory elements.	Apply
8	a	AECB07.13	Implement Tristate TTL, ECL, CMOS families and their interfacing, Memory elements.	Remember
	b	AECB07.14	Understand Concept of Programmable logic devices like FPGA. Logic implementation using Programmable Devices.	Apply
9	a	AECB07.15	Design entry: Schematic, FSM & HDL, different modeling styles in VHDL.	Understand
	b	AECB07.16	Understand Data types and objects, Dataflow, Behavioral and Structural Modeling.	Understand
10	a	AECB07.15	Design entry: Schematic, FSM & HDL, different modeling styles in VHDL.	Apply
	b	AECB07.17	Analyze Synthesis and Simulation VHDL constructs and codes for combinational and sequential circuits.	Apply

Signature of Course Coordinator   **HOD, ECE**